

## Features

- Dual ADC with 8-bit Resolution
- 1 Gsps Sampling Rate per Channel, 2 Gsps in Interlaced Mode
- Single or 1:2 Demultiplexed Output
- LVDS Output Format (100Ω)
- 500 mVpp Analog Input (Differential Only)
- Differential or Single-ended 50Ω PECL/LVDS Compatible Clock Inputs
- Power Supply: 3.3V (Analog), 3.3V (Digital), 2.25V (Output)
- LQFP144 Package
- Temperature Range:
  - 0°C < TA < 70°C (Commercial Grade)
  - -40°C < TA < 85°C (Industrial Grade)
- 3-wire Serial Interface
  - 16-bit Data, 3-bit Address
  - 1:2 or 1:1 Output Demultiplexer Ratio Selection
  - Full or Partial Standby Mode
  - Analog Gain (±1.5 dB) Digital Control
  - Input Clock Selection
  - Analog Input Switch Selection
  - Binary or Gray Logical Outputs
  - Synchronous Data Ready Reset
  - Data Ready Delay Adjustable on Both Channels
  - Interlacing Functions:
    - Offset and Gain (Channel to Channel) Calibration
    - Digital Fine SDA (Fine Sampling Delay Adjust) on One Channel
  - Internal Static or Dynamic Built-In Test (BIT)

## Performance

- Low Power Consumption: 0.7W Per Channel
- Power Consumption in Standby Mode: 120 mW
- 1.5 GHz Full Power Input Bandwidth (-3 dB)
- SNR = 42 dB Typ (6.8 ENOB), THD = -51 dBc, SFDR = -54 dBc at Fs = 1 Gsps  
Fin = 500 MHz
- 2-tone IMD3: -54 dBc (499 MHz, 501 MHz) at 1 Gsps
- DNL = 0.25 LSB, INL = 0.5 LSB
- Channel to Channel Input Offset Error: 0.5 LSB Max (After Calibration)
- Gain Matching (Channel to Channel): 0.5 LSB Max (After Calibration)
- Low Bit Error Rate (10<sup>-13</sup>) at 1 Gsps

## Application

- Instrumentation
- Satellite Receivers
- Direct RF Down Conversion
- WLAN



**Dual 8-bit  
1 Gsps ADC**

**AT84AD001B  
Smart ADC™**



## Description

The AT84AD001B is a monolithic dual 8-bit analog-to-digital converter, offering low 1.4W power consumption and excellent digitizing accuracy. It integrates dual on-chip track/holds that provide an enhanced dynamic performance with a sampling rate of up to 1 Gsps and an input frequency bandwidth of over 1.5 GHz. The dual concept, the integrated demultiplexer and the easy interleaving mode make this device user-friendly for all dual channel applications, such as direct RF conversion or data acquisition. The *smart* function of the 3-wire serial interface eliminates the need for external components, which are usually necessary for gain and offset tuning and setting of other parameters, leading to space and power reduction as well as system flexibility.

## Functional Description

The AT84AD001B is a dual 8-bit 1 Gsps ADC based on advanced high-speed BiCMOS technology.

Each ADC includes a front-end analog multiplexer followed by a Sample and Hold (S/H), and an 8-bit flash-like architecture core analog-to-digital converter. The output data is followed by a switchable 1:1 or 1:2 demultiplexer and LVDS output buffers (100Ω).

Two over-range bits are provided for adjustment of the external gain control on each channel.

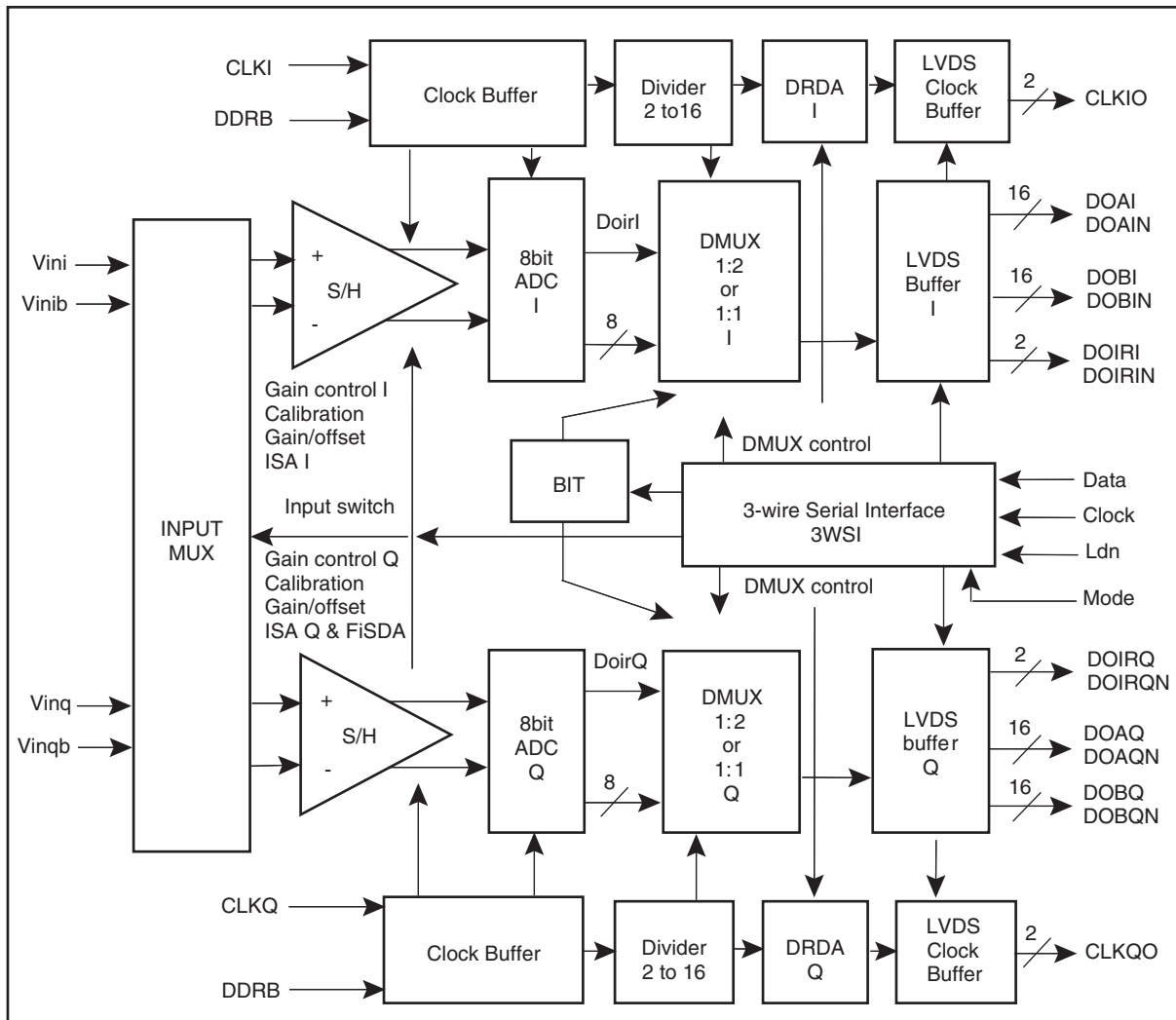
A 3-wire serial interface (3-bit address and 16-bit data) is included to provide several adjustments:

- Analog input range adjustment ( $\pm 1.5$  dB) with 8-bit data control using a 3-wire bus interface (steps of 0.18 dB)
- Analog input switch: both ADCs can convert the same analog input signal I or Q
- Gray or binary encoder output. Output format: DMUX 1:1 or 1:2 with control of the output frequency on the data ready output signal
- Partial or full standby on channel I or channel Q
- Clock selection:
  - Two independent clocks: CLKI and CLKQ
  - One master clock (CLKI) with the same phase for channel I and channel Q
  - One master clock but with two phases (CLKI for channel I and CLKIB for channel Q)
- ISA: Internal Settling Adjustment on channel I and channel Q
- FiSDA: Fine Sampling Delay Adjustment on channel Q
- Adjustable Data Ready Output Delay on both channels
- Test mode: decimation mode (by 16), Built-In Test.

A calibration phase is provided to set the two DC offsets of channel I and channel Q close to code 127.5 and calibrate the two gains to achieve a maximum difference of 0.5 LSB. The offset and gain error can also be set externally via the 3-wire serial interface.

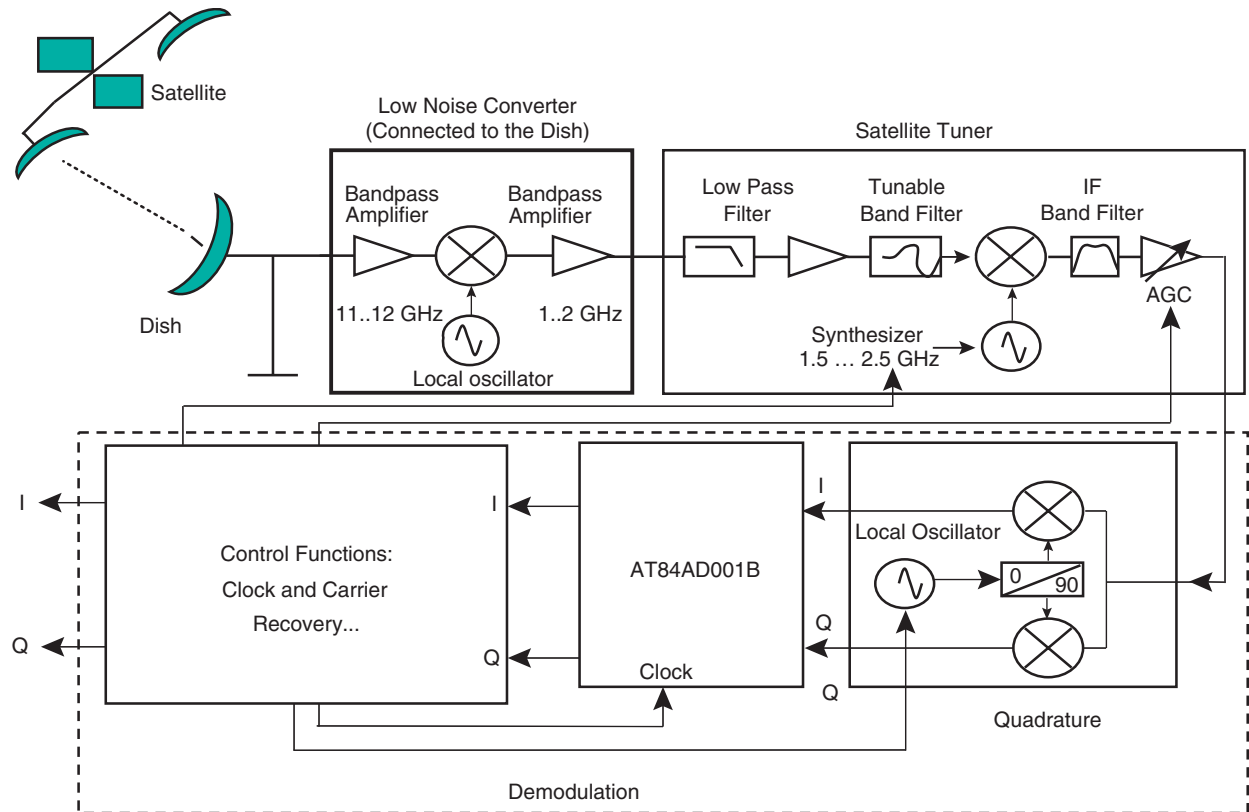
The AD84AD001B operates in fully differential mode from the analog inputs up to the digital outputs. The AD84AD001B features a full-power input bandwidth of 1.5 GHz.

Figure 1. Simplified Block Diagram

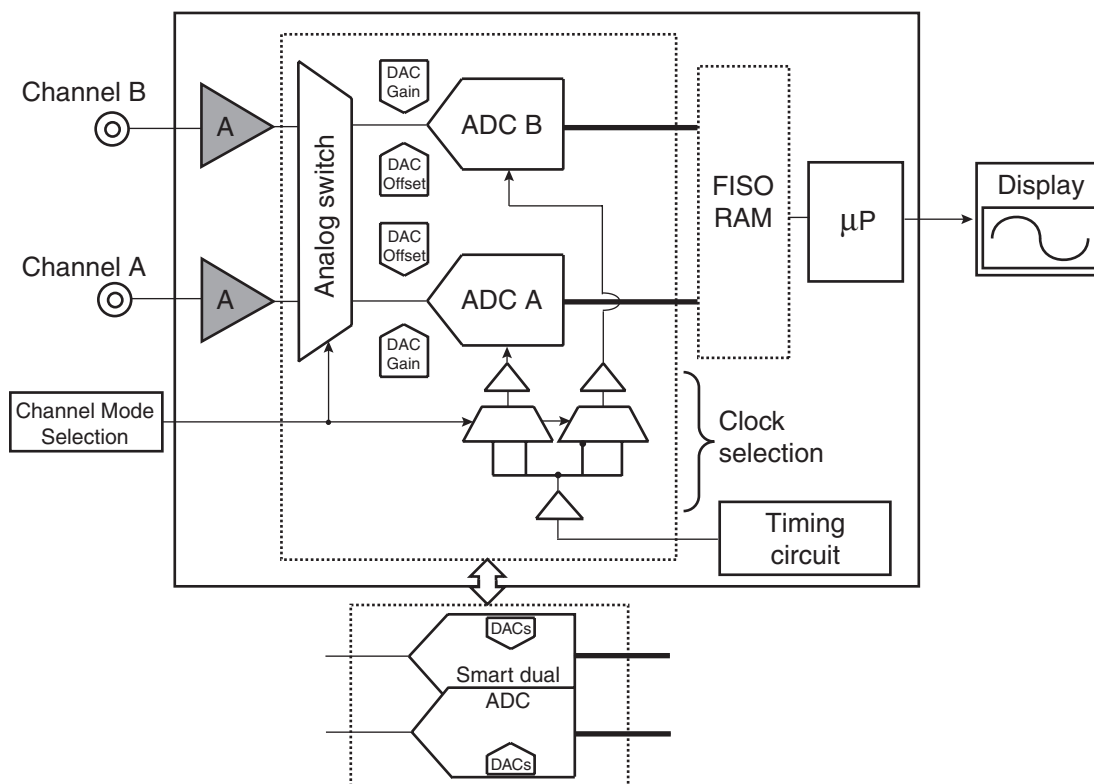


## Typical Applications

**Figure 2.** Satellite Receiver Application



**Figure 3.** Dual Channel Digital Oscilloscope Application



**Table 1.** Absolute Maximum Ratings

| Parameter                                           | Symbol                                             | Value                   | Unit |
|-----------------------------------------------------|----------------------------------------------------|-------------------------|------|
| Analog positive supply voltage                      | $V_{CCA}$                                          | 3.6                     | V    |
| Digital positive supply voltage                     | $V_{CCD}$                                          | 3.6                     | V    |
| Output supply voltage                               | $V_{CCO}$                                          | 3.6                     | V    |
| Maximum difference between $V_{CCA}$ and $V_{CCD}$  | $V_{CCA}$ to $V_{CCD}$                             | $\pm 0.8$               | V    |
| Minimum $V_{CCO}$                                   | $V_{CCO}$                                          | 1.6                     | V    |
| Analog input voltage                                | $V_{INI}$ or $V_{INIB}$<br>$V_{INQ}$ or $V_{INQB}$ | 1/-1                    | V    |
| Digital input voltage                               | $V_D$                                              | -0.3 to $V_{CCD} + 0.3$ | V    |
| Clock input voltage                                 | $V_{CLK}$ or $V_{CLKB}$                            | -0.3 to $V_{CCD} + 0.3$ | V    |
| Maximum difference between $V_{CLK}$ and $V_{CLKB}$ | $V_{CLK} - V_{CLKB}$                               | -2 to 2                 | V    |
| Maximum junction temperature                        | $T_J$                                              | 125                     | °C   |
| Storage temperature                                 | $T_{stg}$                                          | -65 to 150              | °C   |
| Lead temperature (soldering 10s)                    | $T_{leads}$                                        | 300                     | °C   |

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

**Table 2.** Recommended Conditions of Use

| Parameter                                                                                     | Symbol                                          | Comments                             | Recommended Value                  | Unit |
|-----------------------------------------------------------------------------------------------|-------------------------------------------------|--------------------------------------|------------------------------------|------|
| Analog supply voltage                                                                         | $V_{CCA}$                                       |                                      | 3.3                                | V    |
| Digital supply voltage                                                                        | $V_{CCD}$                                       |                                      | 3.3                                | V    |
| Output supply voltage                                                                         | $V_{CCO}$                                       |                                      | 2.25                               | V    |
| Differential analog input voltage (full-scale)                                                | $V_{INi} - V_{INiB}$ or<br>$V_{INQ} - V_{INQB}$ |                                      | 500                                | mVpp |
| Differential clock input level                                                                | $V_{inclk}$                                     |                                      | 600                                | mVpp |
| Internal Settling Adjustment (ISA) with a 3-wire serial interface for channel I and channel Q | ISA                                             |                                      | -50                                | ps   |
| Operating temperature range                                                                   | $T_{Ambient}$                                   | Commercial grade<br>Industrial grade | $0 < T_A < 70$<br>$-40 < T_A < 85$ | °C   |

## Electrical Operating Characteristics

Unless otherwise specified:

- $V_{CCA} = 3.3V$ ;  $V_{CCD} = 3.3V$ ;  $V_{CCO} = 2.25V$
- $V_{INi} - V_{INiB}$  or  $V_{INQ} - V_{INQB} = 500$  mVpp full-scale differential input
- LVDS digital outputs (100Ω)
- $T_A$  (typical) = 25° C
- Full temperature range: 0° C <  $T_A$  < 70° C (commercial grade) or -40° C <  $T_A$  < 85° C (industrial grade)

**Table 3.** Electrical Operating Characteristics in Nominal Conditions

| Parameter                                  | Symbol    | Min  | Typ  | Max  | Unit |
|--------------------------------------------|-----------|------|------|------|------|
| <b>Resolution</b>                          |           |      | 8    |      | Bits |
| <b>Power Requirements</b>                  |           |      |      |      |      |
| Positive supply voltage                    |           |      |      |      |      |
| - Analog                                   | $V_{CCA}$ | 3.15 | 3.3  | 3.45 | V    |
| - Digital                                  | $V_{CCD}$ | 3.15 | 3.3  | 3.45 | V    |
| Output digital (LVDS) and serial interface | $V_{CCO}$ | 2.0  | 2.25 | 2.5  | V    |
| Supply current (typical conditions)        |           |      |      |      |      |
| - Analog                                   | $I_{CCA}$ |      | 150  | 180  | mA   |
| - Digital                                  | $I_{CCD}$ |      | 230  | 275  | mA   |
| - Output                                   | $I_{CCO}$ |      | 100  | 120  | mA   |
| Supply current (1:2 DMUX mode)             |           |      |      |      |      |
| - Analog                                   | $I_{CCA}$ |      | 150  | 180  | mA   |
| - Digital                                  | $I_{CCD}$ |      | 260  | 310  | mA   |
| - Output                                   | $I_{CCO}$ |      | 175  | 210  | mA   |

**Table 3.** Electrical Operating Characteristics in Nominal Conditions (Continued)

| Parameter                                                                                           | Symbol                                             | Min           | Typ               | Max               | Unit           |
|-----------------------------------------------------------------------------------------------------|----------------------------------------------------|---------------|-------------------|-------------------|----------------|
| Supply current (2 input clocks, 1:2 DMUX mode)<br>- Analog<br>- Digital<br>- Output                 | $I_{CCA}$<br>$I_{CCD}$<br>$I_{CCO}$                |               | 150<br>290<br>180 | 180<br>350<br>215 | mA             |
| Supply current<br>(1 channel only, 1:1 DMUX mode)<br>- Analog<br>- Digital<br>- Output              | $I_{CCA}$<br>$I_{CCD}$<br>$I_{CCO}$                |               | 80<br>160<br>55   | 95<br>190<br>65   | mA<br>mA<br>mA |
| Supply current<br>(1 channel only, 1:2 DMUX mode)<br>- Analog<br>- Digital<br>- Output              | $I_{CCA}$<br>$I_{CCD}$<br>$I_{CCO}$                |               | 80<br>170<br>90   | 95<br>205<br>110  | mA<br>mA<br>mA |
| Supply current (full standby mode)<br>- Analog<br>- Digital<br>- Output                             | $I_{CCA}$<br>$I_{CCD}$<br>$I_{CCO}$                |               | 12<br>24<br>3     | 17<br>34<br>5     | mA<br>mA<br>mA |
| Nominal dissipation<br>(1 clock, 1:1 DMUX mode, 2 channels)                                         | $P_D$                                              |               | 1.4               | 1.7               | W              |
| Nominal dissipation (full standby mode)                                                             | stbpd                                              |               | 120               |                   | mW             |
| <b>Analog Inputs</b>                                                                                |                                                    |               |                   |                   |                |
| Full-scale differential analog input voltage                                                        | $V_{INi} - V_{INiB}$<br>or<br>$V_{INQ} - V_{INQB}$ | 450           | 500               | 550               | mV<br>mV       |
| Analog input capacitance I and Q                                                                    | $C_{IN}$                                           |               |                   | 2                 | pF             |
| Full power input bandwidth (-3 dB)                                                                  | FPBW                                               |               | 1.5               |                   | GHz            |
| Gain flatness (-0.5 dB)                                                                             |                                                    |               | 500               |                   | MHz            |
| <b>Clock Input</b>                                                                                  |                                                    |               |                   |                   |                |
| Logic compatibility for clock inputs and DDRB Reset (pins 124,125,126,127,128,129)                  |                                                    | PECL/ECL/LVDS |                   |                   |                |
| PECL/LVDS clock inputs voltages<br>( $V_{CLKI/IN}$ or $V_{CLKQ/QN}$ )<br>Differential logical level | $V_{IL} - V_{IH}$                                  |               | 600               |                   | mV             |
| Clock input power level                                                                             |                                                    | -9            | 0                 | 6                 | dBm            |
| Clock input capacitance                                                                             |                                                    |               | 2                 |                   | pF             |
| <b>Digital Outputs</b>                                                                              |                                                    |               |                   |                   |                |
| Logic compatibility for digital outputs<br>(depending on the value of $V_{CCO}$ )                   |                                                    | LVDS          |                   |                   |                |
| Differential output voltage swings<br>(assuming $V_{CCO} = 2.25V$ )                                 | $V_{OD}$                                           | 220           | 270               | 350               | mV             |

**Table 3.** Electrical Operating Characteristics in Nominal Conditions (Continued)

| Parameter                                                                                                                   | Symbol               | Min             | Typ             | Max             | Unit            |
|-----------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------|-----------------|-----------------|-----------------|
| Output levels (assuming $V_{CCO} = 2.25V$ )<br>100 $\Omega$ differentially terminated<br>Logic 0 voltage<br>Logic 1 voltage | $V_{OL}$<br>$V_{OH}$ | 1.0<br>1.25     | 1.1<br>1.35     | 1.2<br>1.45     | V<br>V          |
| Output offset voltage (assuming $V_{CCO} = 2.25V$ )<br>100 $\Omega$ differentially terminated                               | $V_{OS}$             | 1125            | 1250            | 1325            | mV              |
| Output impedance                                                                                                            | $R_O$                |                 | 50              |                 | $\Omega$        |
| Output current (shorted output)                                                                                             |                      |                 |                 | 12              | mA              |
| Output current (grounded output)                                                                                            |                      |                 | 30              |                 | mA              |
| Output level drift with temperature                                                                                         |                      |                 | 1.3             |                 | mV/ $^{\circ}C$ |
| <b>Digital Input (Serial Interface)</b>                                                                                     |                      |                 |                 |                 |                 |
| Maximum clock frequency (input clk)                                                                                         | Fclk                 |                 |                 | 50              | MHz             |
| Input logical level 0 (clk, mode, data, ldn)                                                                                |                      | -0.4            | 0               | 0.4             | V               |
| Input logical level 1 (clk, mode, data, ldn)                                                                                |                      | $V_{CCO} - 0.4$ | $V_{CCO} - 0.4$ | $V_{CCO} + 0.4$ | V               |
| Output logical level 0 (cal)                                                                                                |                      | -0.4            | 0               | 0.4             | V               |
| Output logical level 1 (cal)                                                                                                |                      | $V_{CCO} - 0.4$ | $V_{CCO}$       | $V_{CCO} + 0.4$ | V               |
| Maximum output load (cal)                                                                                                   |                      |                 |                 | 15              | pF              |

Note: The gain setting is 0 dB, one clock input, no standby mode [full power mode], 1:1 DMUX, calibration off.

**Table 4.** Electrical Operating Characteristics

| Parameter                                                                                                     | Symbol | Min                                         | Typ            | Max        | Unit                       |
|---------------------------------------------------------------------------------------------------------------|--------|---------------------------------------------|----------------|------------|----------------------------|
| <b>DC Accuracy</b>                                                                                            |        |                                             |                |            |                            |
| No missing code                                                                                               |        | Guaranteed over specified temperature range |                |            |                            |
| Differential non-linearity                                                                                    | DNL    |                                             | 0.25           | 0.6        | LSB                        |
| Integral non-linearity                                                                                        | INL    |                                             | 0.5            | 1          | LSB                        |
| Gain error (single channel I or Q) with calibration                                                           |        | -0.5                                        | 0              | 0.5        | LSB                        |
| Input offset matching (single channel I or Q) with calibration                                                |        | -0.5                                        | 0              | 0.5        | LSB                        |
| Gain error drift against temperature<br>Gain error drift against $V_{CCA}$                                    |        |                                             | 0.062<br>0.064 |            | LSB/ $^{\circ}C$<br>LSB/mV |
| Mean output offset code with calibration                                                                      |        | 127                                         | 127.5          | 128        | LSB                        |
| <b>Transient Performance</b>                                                                                  |        |                                             |                |            |                            |
| Bit Error Rate<br>$F_s = 1$ Gsps<br>$F_{in} = 250$ MHz                                                        | BER    |                                             | $10^{-13}$     | $10^{-10}$ | Error/<br>sample           |
| ADC settling time channel I or Q<br>(between 10% - 90% of output response)<br>$V_{inI} - V_{inIB} = 500$ mVpp | TS     |                                             | 170            |            | ps                         |

Note: Gain setting is 0 dB, two clock inputs, no standby mode [full power mode], 1:2 DMUX, calibration on.

**Table 5. AC Performances**

| Parameter                                                                                                           | Symbol | Min  | Typ  | Max | Unit |
|---------------------------------------------------------------------------------------------------------------------|--------|------|------|-----|------|
| AC Performance                                                                                                      |        |      |      |     |      |
| Signal-to-noise Ratio                                                                                               |        |      |      |     |      |
| Fs = 1 Gsps      Fin = 20 MHz                                                                                       | SNR    | 42   | 44   |     | dBc  |
| Fs = 1 Gsps      Fin = 500 MHz                                                                                      |        | 40   | 42   |     | dBc  |
| Fs = 1 Gsps      Fin = 1 GHz                                                                                        |        |      | 41   |     | dBc  |
| Effective Number of Bits                                                                                            |        |      |      |     |      |
| Fs = 1 Gsps      Fin = 20 MHz                                                                                       | ENOB   | 7    | 7.2  |     | Bits |
| Fs = 1 Gsps      Fin = 500 MHz                                                                                      |        | 6.5  | 6.8  |     | Bits |
| Fs = 1 Gsps      Fin = 1 GHz                                                                                        |        |      | 6.2  |     | Bits |
| Total Harmonic Distortion (First 9 Harmonics)                                                                       |        |      |      |     |      |
| Fs = 1 Gsps      Fin = 20 MHz                                                                                       | ITHDI  | 48   | 54   |     | dBc  |
| Fs = 1 Gsps      Fin = 500 MHz                                                                                      |        | 45   | 51   |     | dBc  |
| Fs = 1 Gsps      Fin = 1 GHz                                                                                        |        |      | 42   |     | dBc  |
| Spurious Free Dynamic Range                                                                                         |        |      |      |     |      |
| Fs = 1 Gsps      Fin = 20 MHz                                                                                       | ISFDRI | 50   | 56   |     | dBc  |
| Fs = 1 Gsps      Fin = 500 MHz                                                                                      |        | 48   | 54   |     | dBc  |
| Fs = 1 Gsps      Fin = 1 GHz                                                                                        |        |      | 43   |     | dBc  |
| Two-tone Inter-modulation Distortion (Single Channel)                                                               |        |      |      |     |      |
| F <sub>IN1</sub> = 499 MHz , F <sub>IN2</sub> = 501 MHz at Fs = 1 Gsps                                              | IMD    |      | -54  |     | dBc  |
| Band flatness from DC up to 600 MHz                                                                                 |        |      | ±0.5 |     | dB   |
| Phase matching using auto-calibration and FiSDA in interlace mode (channel I and Q)<br>Fin = 250 MHz<br>Fs = 1 Gsps | dφ     | -0.7 | 0    | 0.7 | °    |
| Crosstalk channel I versus channel Q<br>Fin = 250 MHz, Fs = 1 Gsps <sup>(2)</sup>                                   | Cr     |      | -55  |     | dB   |

Notes: 1. Differential input [-1 dBFS analog input level], gain setting is 0 dB, two input clock signals, no standby mode, 1:1 DMUX, ISA = -50 ps.  
2. Measured on the AT84AD001TD-EB Evaluation Board.

**Table 6. AC Performances in Interlace Mode**

| Parameter                                                                                             | Symbol    | Min | Typ  | Max | Unit |
|-------------------------------------------------------------------------------------------------------|-----------|-----|------|-----|------|
| Interlace Mode                                                                                        |           |     |      |     |      |
| Maximum equivalent clock frequency $F_{int} = 2 \times F_s$<br>Where $F_s$ = external clock frequency | $F_{int}$ | 2   |      |     | Gsps |
| Minimum clock frequency                                                                               | $F_{int}$ |     | 20   |     | Msps |
| Differential non-linearity in interlace mode                                                          | intDNL    |     | 0.25 |     | LSB  |
| Integral non-linearity in interlace mode                                                              | intINL    |     | 0.5  |     | LSB  |
| Signal-to-noise Ratio in Interlace Mode                                                               |           |     |      |     |      |
| $F_{int} = 2$ Gsps $F_{in} = 20$ MHz                                                                  | iSNR      |     | 42   |     | dBc  |
| $F_{int} = 2$ Gsps $F_{in} = 250$ MHz                                                                 |           |     | 40   |     | dBc  |
| Effective Number of Bits in Interlace Mode                                                            |           |     |      |     |      |
| $F_{int} = 2$ Gsps $F_{in} = 20$ MHz                                                                  | iENOB     |     | 7.1  |     | Bits |
| $F_{int} = 2$ Gsps $F_{in} = 250$ MHz                                                                 |           |     | 6.8  |     | Bits |
| Total Harmonic Distortion in Interlace Mode                                                           |           |     |      |     |      |
| $F_{int} = 2$ Gsps $F_{in} = 20$ MHz                                                                  | liTHDI    |     | 52   |     | dBc  |
| $F_{int} = 2$ Gsps $F_{in} = 250$ MHz                                                                 |           |     | 49   |     | dBc  |
| Spurious Free Dynamic Range in Interlace Mode                                                         |           |     |      |     |      |
| $F_{int} = 2$ Gsps $F_{in} = 20$ MHz                                                                  | liSFDRl   |     | 54   |     | dBc  |
| $F_{int} = 2$ Gsps $F_{in} = 250$ MHz                                                                 |           |     | 52   |     | dBc  |
| Two-tone Inter-modulation Distortion (Single Channel) in Interlace Mode                               |           |     |      |     |      |
| $F_{IN1} = 249$ MHz , $F_{IN2} = 251$ MHz at $F_{int} = 2$ Gsps                                       | iIMD      |     | -54  |     | dBc  |

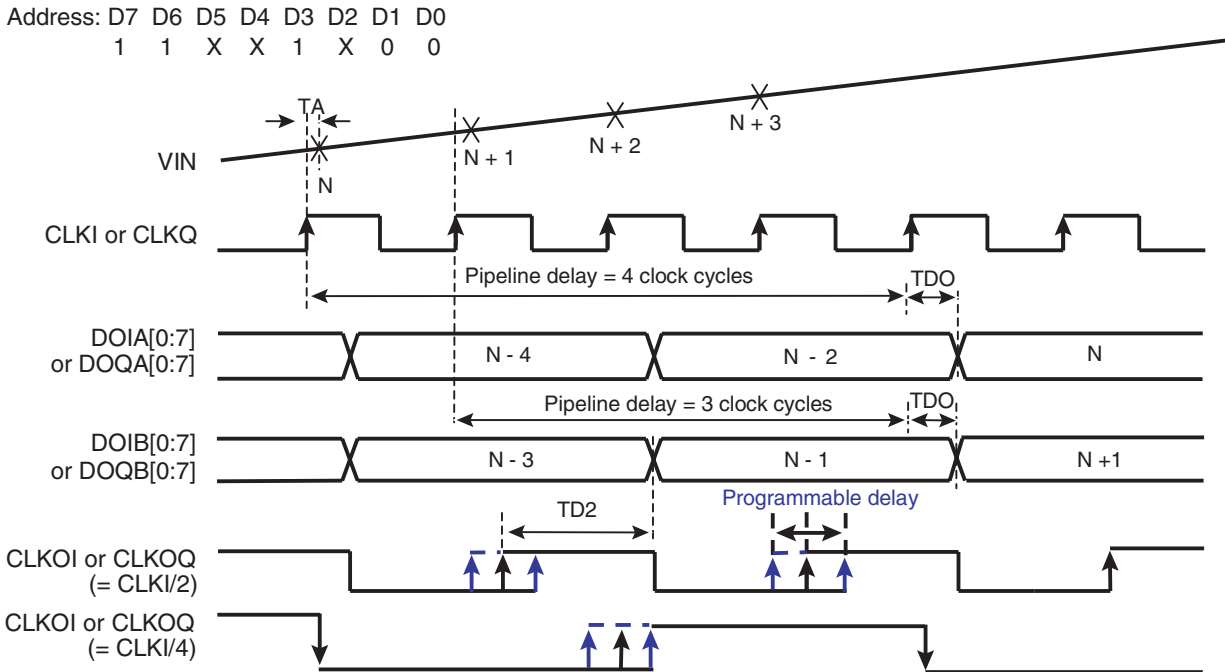
Note: One analog input on both cores, clock I samples the analog input on the rising and falling edges. The calibration phase is necessary. The gain setting is 0 dB, one input clock I, no standby mode, 1:1 DMUX, FiSDA adjustment.

**Table 7. Switching Performances**

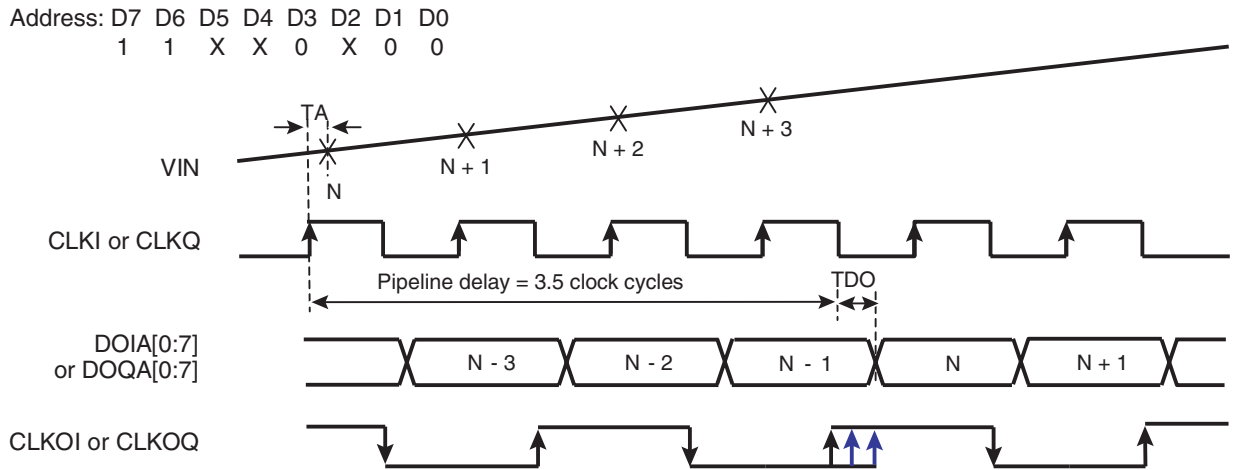
| Parameter                                                                     | Symbol                       | Min                                                                      | Typ                          | Max | Unit         |
|-------------------------------------------------------------------------------|------------------------------|--------------------------------------------------------------------------|------------------------------|-----|--------------|
| Switching Performance and Characteristics - See “Timing Diagrams” on page 12. |                              |                                                                          |                              |     |              |
| Maximum operating clock frequency                                             | F <sub>S</sub>               | 1                                                                        |                              |     | Gsps         |
| Maximum operating clock frequency in BIT and decimation modes                 | F <sub>S</sub><br>(BIT, DEC) |                                                                          |                              | 750 | Msps         |
| Minimum clock frequency (no transparent mode)                                 | F <sub>S</sub>               |                                                                          | 10                           |     | Msps         |
| Minimum clock frequency (with transparent mode)                               |                              |                                                                          | 1                            |     | Ksps         |
| Minimum clock pulse width [high]<br>(No transparent mode)                     | TC1                          | 0.4                                                                      | 0.5                          | 50  | ns           |
| Minimum clock pulse width [low]<br>(No transparent mode)                      | TC2                          | 0.4                                                                      | 0.5                          | 50  | ns           |
| Aperture delay: nominal mode with ISA & FiSDA                                 | TA                           |                                                                          | 1                            |     | ns           |
| Aperture uncertainty                                                          | Jitter                       |                                                                          | 0.4                          |     | ps (rms)     |
| Data output delay between input clock and data                                | TDO                          |                                                                          | 3.8                          |     | ns           |
| Data Ready Output Delay                                                       | TDR                          |                                                                          | 3                            |     | ns           |
| Data Ready Reset to Data Ready                                                | TRDR                         |                                                                          | 2                            |     | ns           |
| Data Output Delay with Data Ready                                             | TD2                          |                                                                          | 1/2 F <sub>s</sub><br>+Tdrda |     | ps           |
| Data Ready (CLKO) Delay Adjust (140 ps steps)                                 | Tdrda range                  |                                                                          | -560 to 420                  |     | ps           |
| Output skew                                                                   |                              | 50                                                                       |                              | 100 | ps           |
| Output rise/fall time for DATA (20% - 80%)                                    | TR/TF                        | 300                                                                      | 350                          | 500 | ps           |
| Output rise/fall time for DATA READY (20% - 80%)                              | TR/TF                        | 300                                                                      | 350                          | 500 | ps           |
| Data pipeline delay (nominal mode)                                            | TPD                          | 3 (port B)<br>3.5 (port A, 1:1 DMUX mode)<br>4 (port A, 1:2 DMUX mode)   |                              |     | Clock cycles |
| Data pipeline delay (nominal mode) in S/H transparent mode                    |                              | 2.5 (port B)<br>3 (port A, 1:1 DMUX mode)<br>3.5 (port A, 1:2 DMUX mode) |                              |     |              |
| DDRB recommended pulse width                                                  |                              | 1                                                                        |                              |     | ns           |

## Timing Diagrams

**Figure 4.** Timing Diagram, ADC I or ADC Q, 1:2 DMUX Mode, Clock I for ADC I, Clock Q for ADC Q

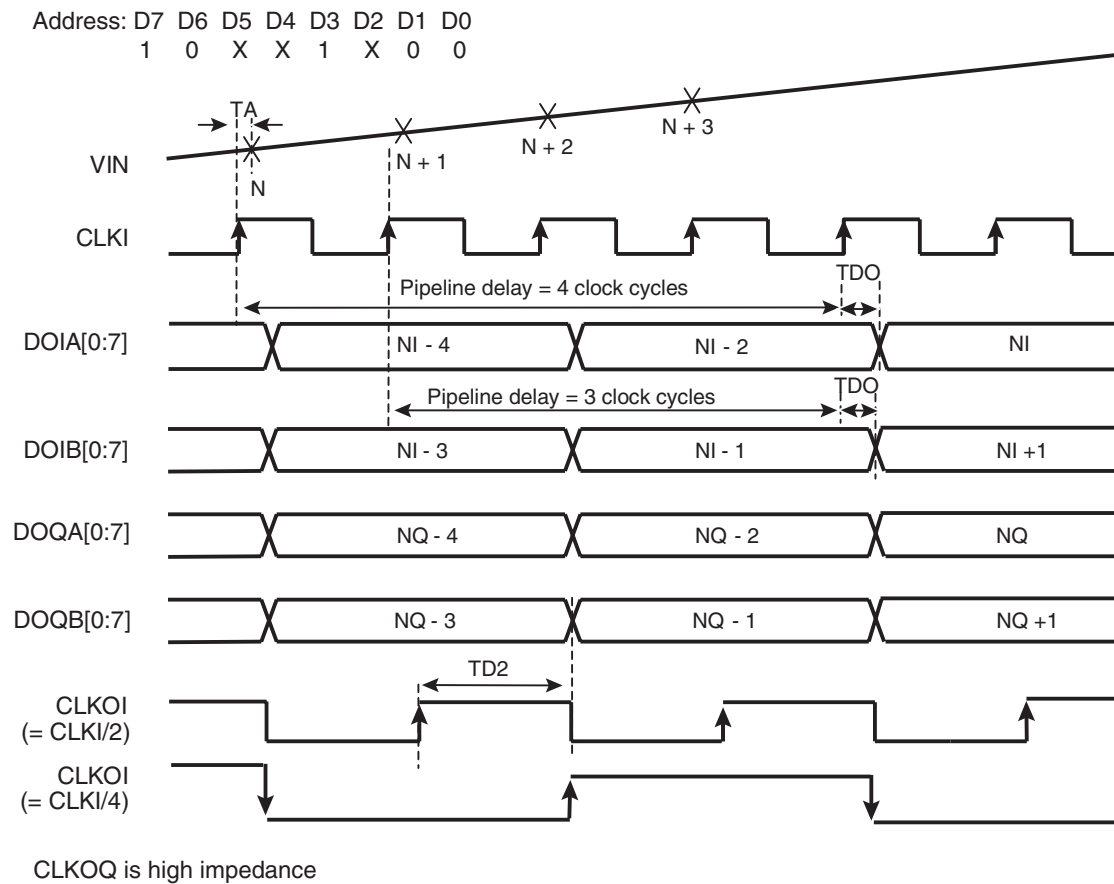


**Figure 5.** 1:1 DMUX Mode, Clock I = ADC I, Clock Q = ADC Q



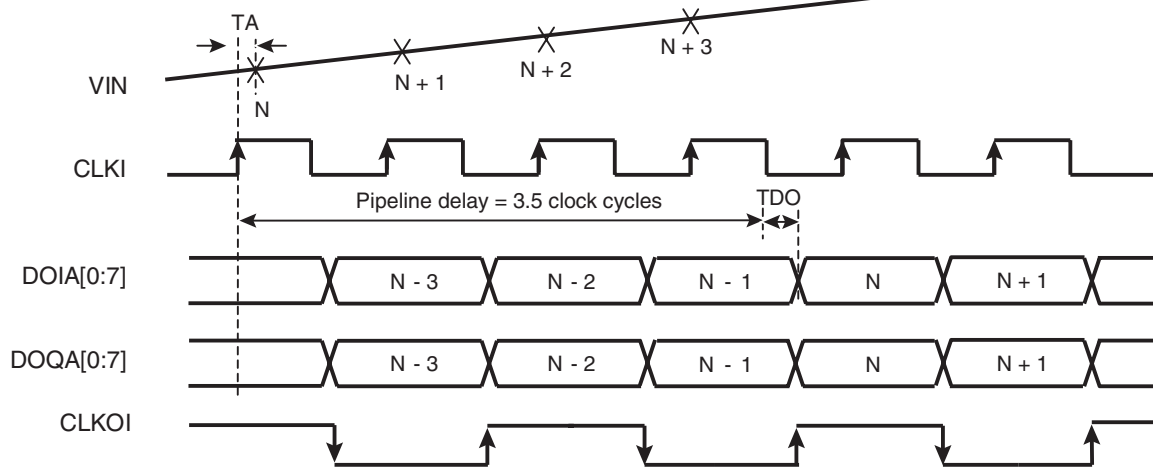
DOIB[0:7] and DOQB[0:7] are high impedance

**Figure 6.** 1:2 DMUX Mode, Clock I = ADC I, Clock I = ADC Q



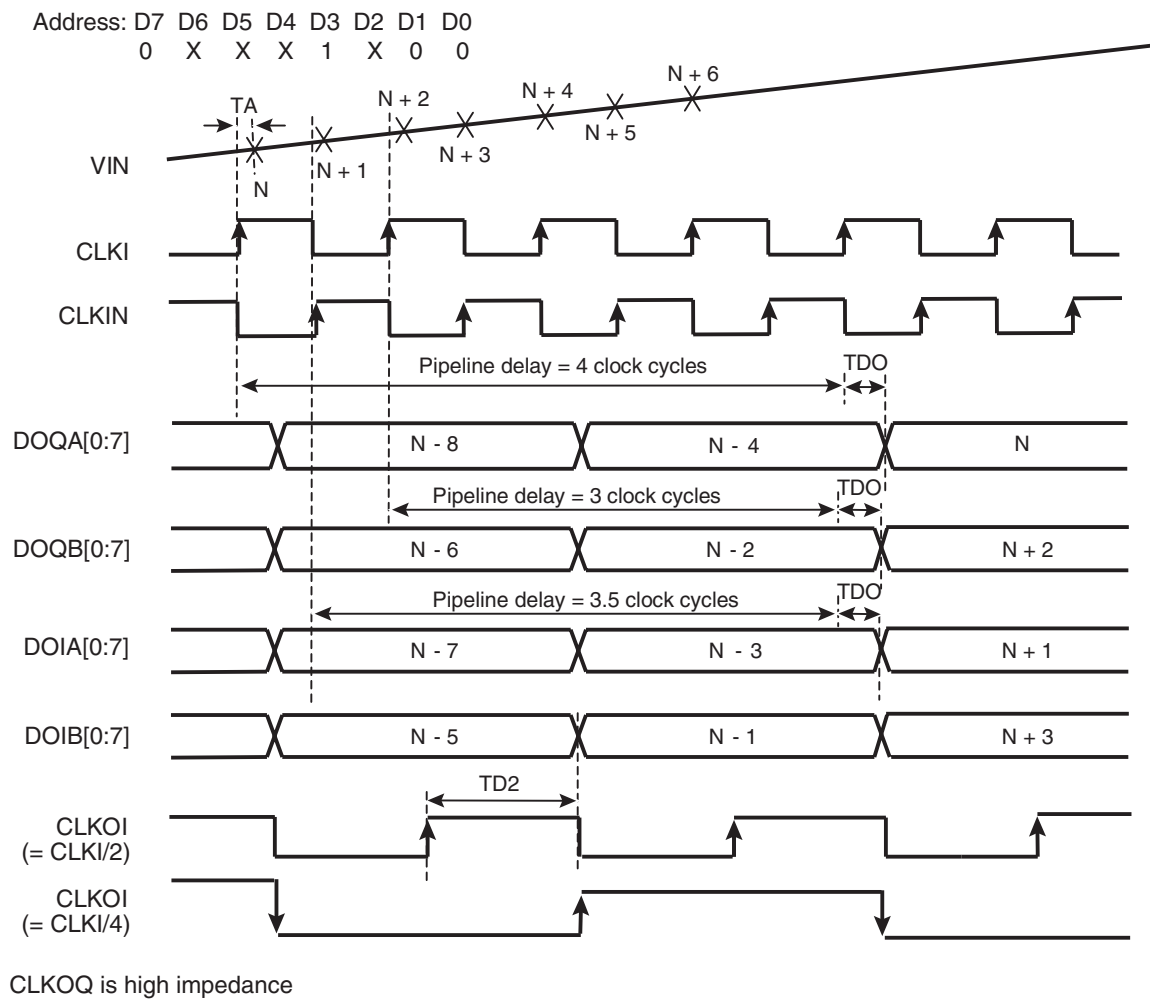
**Figure 7.** 1:1 DMUX Mode, Clock I = ADC I, Clock I = ADC Q

Address: D7 D6 D5 D4 D3 D2 D1 D0  
 1 0 X X 0 X 0 0

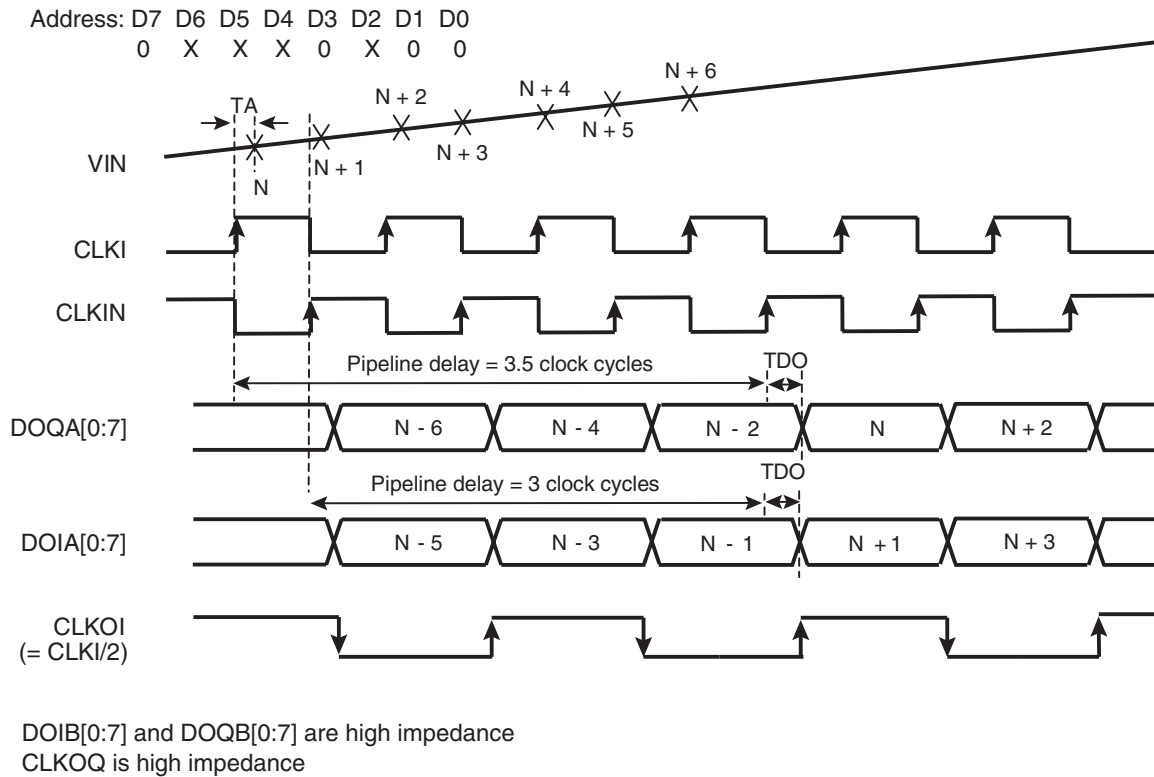


$DOIB[0:7]$  and  $DOQB[0:7]$  are high impedance  
 $CLKOQ$  is high impedance

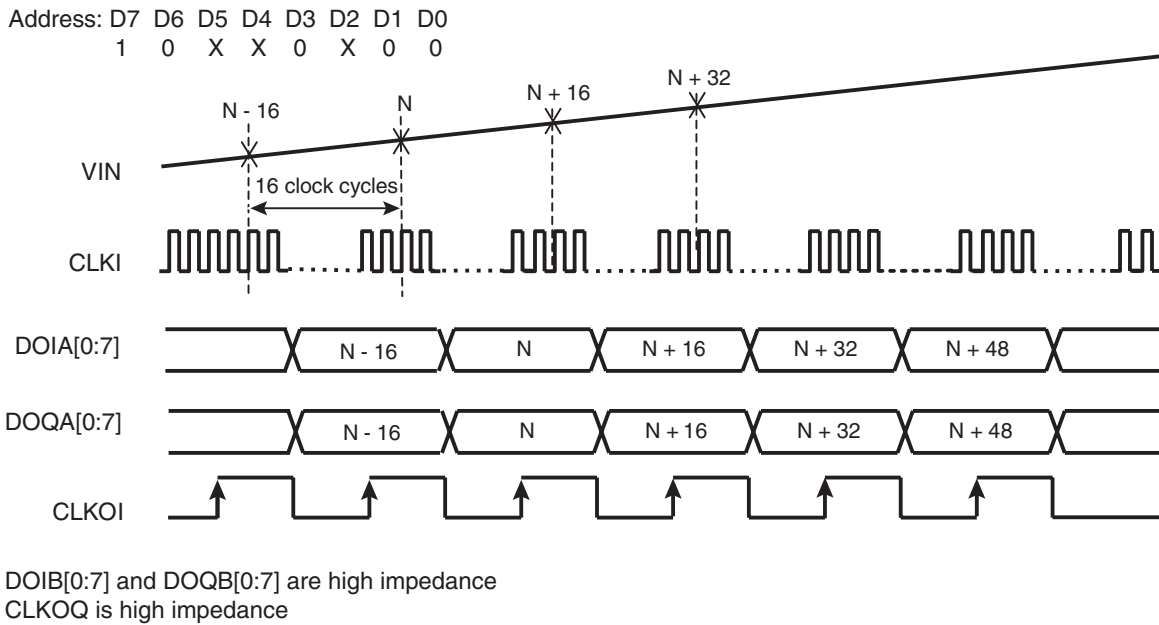
**Figure 8.** 1:2 DMUX Mode, Clock I = ADC I, Clock IN = ADC Q



**Figure 9.** 1:1 DMUX Mode, Clock I = ADC I, Clock IN = ADC Q

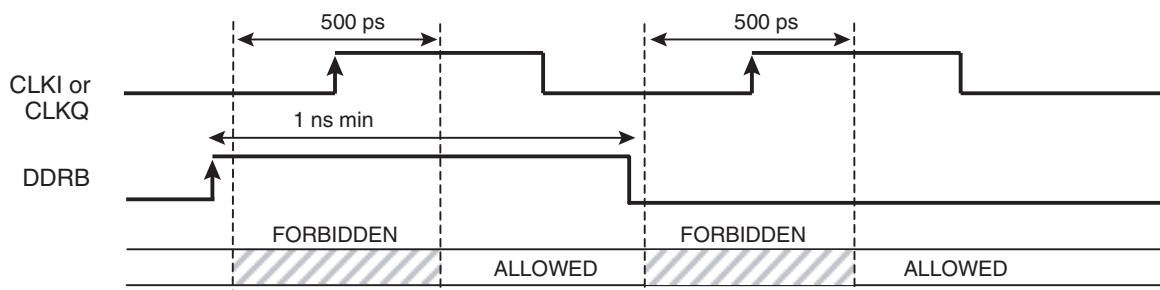


**Figure 10.** 1:1 DMUX Mode, Decimation Mode Test (1:16 Factor)

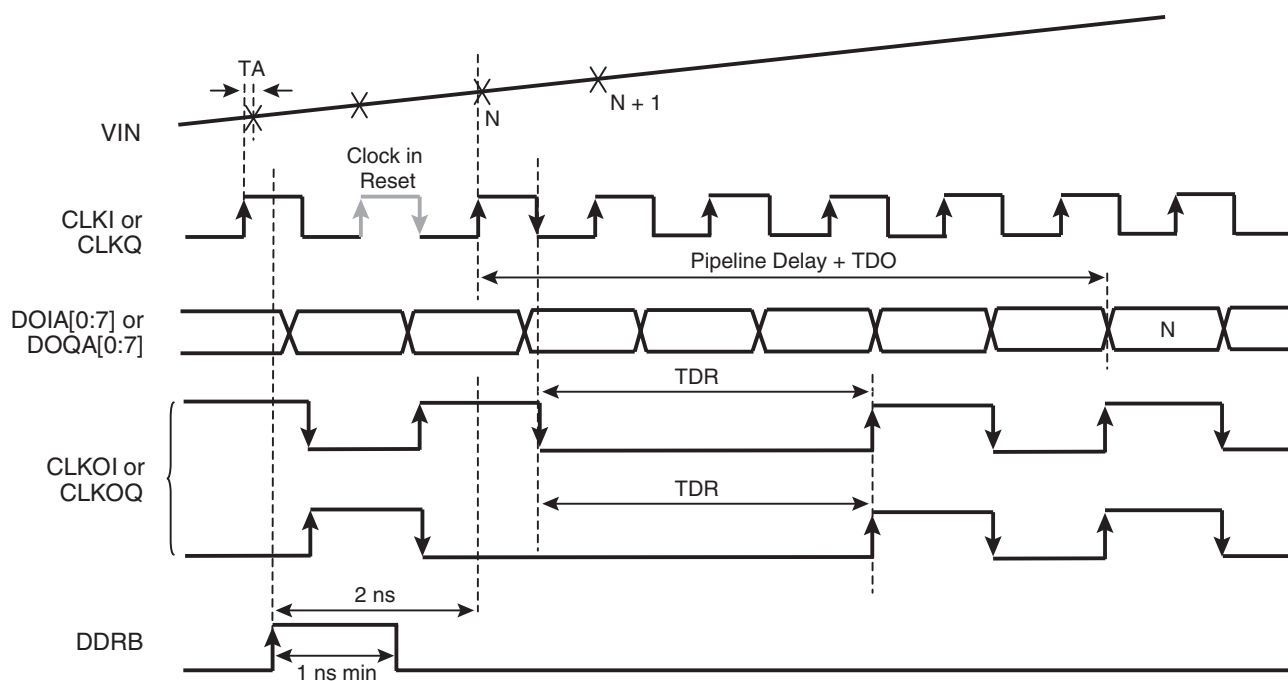


- Notes:
1. The maximum clock input frequency in decimation mode is 750 Msps.
  2. Frequency(CLKOI) = Frequency(Data) = Frequency(CLKI)/16.

**Figure 11. Data Ready Reset**

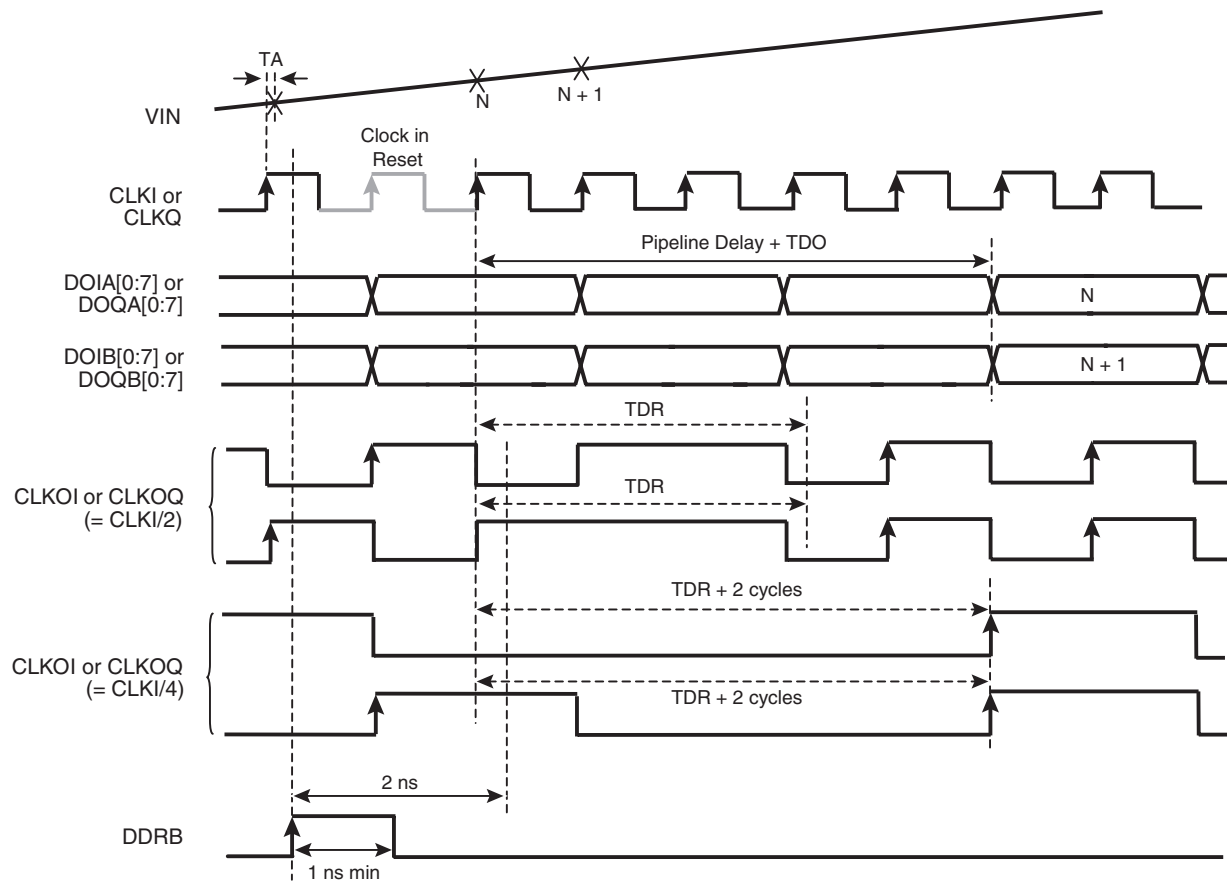


**Figure 12. Data Ready Reset 1:1 DMUX Mode**



**Note:** The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:1 DMUX mode). The next falling edge of the input clock after reset makes the output clock return to normal mode (after TDR).

**Figure 13. Data Ready Reset 1:2 DMUX Mode**



Notes: 1. In 1:2 DMUX, Fs/2 mode:

The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is low, it goes high only when its half cycle is complete; if the reset occurs when it is high, it remains high) and then only, remains in reset state (frozen to a high level in 1:2 DMUX Fs/2 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

2. In 1:2 DMUX, Fs/4 mode:

The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:2 DMUX Fs/4 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

## Functions Description

**Table 8.** Description of Functions

| Name                                                                 | Function                                                    |                             |                                                   |
|----------------------------------------------------------------------|-------------------------------------------------------------|-----------------------------|---------------------------------------------------|
| V <sub>CCA</sub>                                                     | Positive analog power supply                                |                             |                                                   |
| V <sub>CCD</sub>                                                     | Positive digital power supply                               |                             |                                                   |
| V <sub>CCO</sub>                                                     | Positive output power supply                                |                             |                                                   |
| GNDA                                                                 | Analog ground                                               |                             |                                                   |
| GNDD                                                                 | Digital ground                                              |                             |                                                   |
| GNDO                                                                 | Output ground                                               |                             |                                                   |
| V <sub>INI</sub> , V <sub>INIB</sub>                                 | Differential analog inputs I                                |                             |                                                   |
| V <sub>INQ</sub> , V <sub>INQB</sub>                                 | Differential analog inputs Q                                |                             |                                                   |
| CLKOI, CLKOIN, CLKOQ, CLKOQN                                         | Differential output data ready I and Q                      |                             |                                                   |
| CLKI, CLKIN, CLKQ, CLKQN                                             | Differential clock inputs I and Q                           |                             |                                                   |
| DDRB, DDRBN                                                          | Synchronous data ready reset I and Q                        |                             |                                                   |
| Mode                                                                 | Bit selection for 3-wire bus or nominal setting             |                             |                                                   |
| Clk                                                                  | Input clock for 3-wire bus interface                        |                             |                                                   |
| Data                                                                 | Input data for 3-wire bus                                   |                             |                                                   |
| Ldn                                                                  | Beginning and end of register line for 3-wire bus interface | DOIRI, DOIRIN DOIRQ, DOIRQN | Differential output IN range data I and Q         |
| <DOAI0:DOAI7><br><DOAI0N:DOAI7N><br><DOBI0:DOBI7><br><DOBI0N:DOBI7N> | Differential output data port channel I                     | VtestQ                      | Test voltage output for ADC Q (to be left open)   |
|                                                                      |                                                             | VtestI                      | Test voltage output for ADC I (to be left open)   |
| <DOAQ0:DOAQ7><br><DOAQ0N:DOAQ7N><br><DOBQ0:DOBQ7><br><DOBQ0N:DOBQ7N> | Differential output data port channel Q                     | Cal                         | Output bit status internal calibration            |
|                                                                      |                                                             | Vdiode                      | Test diode voltage for T <sub>j</sub> measurement |

## Digital Output Coding (Nominal Settings)

**Table 9.** Digital Output Coding (Nominal Setting)

| Differential Analog Input | Voltage Level                   | Digital Output I or Q (Binary Coding) | Out-of-range Bit |
|---------------------------|---------------------------------|---------------------------------------|------------------|
| > 250 mV                  | > Positive full-scale + 1/2 LSB | 1 1 1 1 1 1 1 1                       | 1                |
| 250 mV                    | Positive full-scale + 1/2 LSB   | 1 1 1 1 1 1 1 1                       | 0                |
| 248 mV                    | Positive full-scale - 1/2 LSB   | 1 1 1 1 1 1 1 0                       | 0                |
| 1 mV                      | Bipolar zero + 1/2 LSB          | 1 0 0 0 0 0 0 0                       | 0                |
| -1 mV                     | Bipolar zero - 1/2 LSB          | 0 1 1 1 1 1 1 1                       | 0                |
| -248 mV                   | Negative full-scale + 1/2 LSB   | 0 0 0 0 0 0 0 1                       | 0                |
| -250 mV                   | Negative full-scale - 1/2 LSB   | 0 0 0 0 0 0 0 0                       | 0                |
| < -250 mV                 | < Negative full-scale - 1/2 LSB | 0 0 0 0 0 0 0 0                       | 1                |

## Pin Description

**Table 10.** AT84AD001B LQFP 144 Pin Description

| Symbol            | Pin number                                                                                                      | Function                                                                                  |
|-------------------|-----------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| GNDA, GNDD, GNDO  | 10, 12, 22, 24, 36, 38, 40, 42, 44, 46, 51, 54, 59, 61, 63, 65, 67, 69, 85, 87, 97, 99, 109, 111, 130, 142, 144 | Ground pins. To be connected to external ground plane                                     |
| V <sub>CCA</sub>  | 41, 43, 45, 60, 62, 64                                                                                          | Analog positive supply: 3.3V typical                                                      |
| V <sub>CCD</sub>  | 9, 21, 37, 39, 66, 68, 88, 100, 112, 123, 141                                                                   | 3.3V digital supply                                                                       |
| V <sub>CCO</sub>  | 11, 23, 86, 98, 110, 143                                                                                        | 2.25V output and 3-wire serial interface supply                                           |
| V <sub>INI</sub>  | 57, 58                                                                                                          | In-phase (+) analog input signal of the sample & hold differential preamplifier channel I |
| V <sub>INIB</sub> | 55, 56                                                                                                          | Inverted phase (-) of analog input signal (V <sub>INI</sub> )                             |
| V <sub>INQ</sub>  | 47, 48                                                                                                          | In-phase (+) analog input signal of the sample & hold differential preamplifier channel Q |
| V <sub>INQB</sub> | 49, 50                                                                                                          | Inverted phase (-) of analog input signal (V <sub>INQ</sub> )                             |
| CLKI              | 124                                                                                                             | In-phase (+) clock input signal                                                           |
| CLKIN             | 125                                                                                                             | Inverted phase (-) clock input signal (CLKI)                                              |
| CLKQ              | 129                                                                                                             | In-phase (+) clock input signal                                                           |

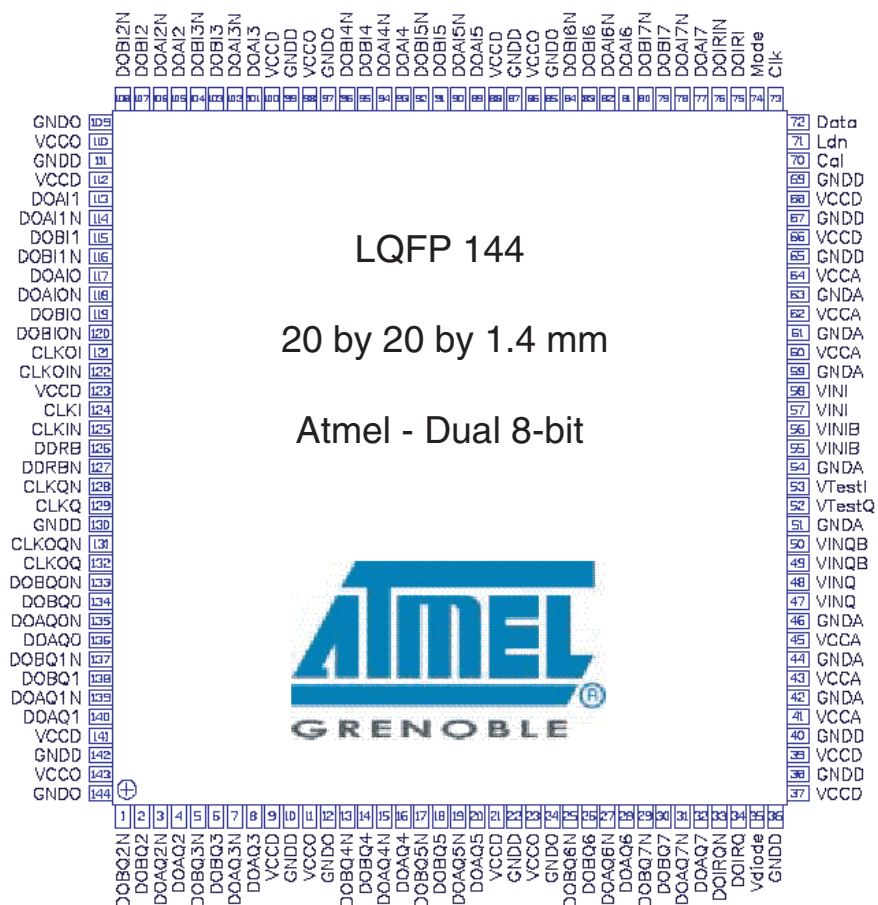
**Table 10.** AT84AD001B LQFP 144 Pin Description (Continued)

| Symbol                                                         | Pin number                         | Function                                                                                                                             |
|----------------------------------------------------------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| CLKQN                                                          | 128                                | Inverted phase (-) clock input signal (CLKQ)                                                                                         |
| DDRB                                                           | 126                                | Synchronous data ready reset I and Q                                                                                                 |
| DDRBN                                                          | 127                                | Inverted phase (-) of input signal (DDRB)                                                                                            |
| DOAI0, DOAI1, DOAI2, DOAI3, DOAI4, DOAI5, DOAI6, DOAI7         | 117, 113, 105, 101, 93, 89, 81, 77 | In-phase (+) digital outputs first phase demultiplexer (channel I) DOAI0 is the LSB. DOAI7 is the MSB                                |
| DOAI0N, DOAI1N, DOAI2N, DOAI3N, DOAI4N, DOAI5N, DOAI6N, DOAI7N | 118, 114, 106, 102, 94, 90, 82, 78 | Inverted phase (-) digital outputs first phase demultiplexer (channel I) DOAI0N is the LSB. DOAI7N is the MSB                        |
| DOBI0, DOBI1, DOBI2, DOBI3, DOBI4, DOBI5, DOBI6, DOBI7         | 119, 115, 107, 103, 95, 91, 83, 79 | In-phase (+) digital outputs second phase demultiplexer (channel I) DOBI0 is the LSB. DOBI7 is the MSB                               |
| DOBI0N, DOBI1N, DOBI2N, DOBI3N, DOBI4N, DOBI5N, DOBI6N, DOBI7N | 120, 116, 108, 104, 96, 92, 84, 80 | Inverted phase (-) digital outputs second phase demultiplexer (channel I) DOBI0N is the LSB. DOBI7N is the MSB                       |
| DOAQ0, DOAQ1, DOAQ2, DOAQ3, DOAQ4, DOAQ5, DOAQ6, DOAQ7         | 136, 140, 4, 8, 16, 20, 28, 32     | In-phase (+) digital outputs first phase demultiplexer (channel Q) DOAI0 is the LSB. DOAQ7 is the MSB                                |
| DOAQ0N, DOAQ1N, DOAQ2N, DOAQ3N, DOAQ4N, DOAQ5N, DOAQ6N, DOAQ7N | 135, 139, 3, 7, 15, 19, 27, 31     | Inverted phase (-) digital outputs first phase demultiplexer (channel Q) DOAI0N is the LSB. DOAQ7N is the MSB                        |
| DOBQ0, DOBQ1, DOBQ2, DOBQ3, DOBQ4, DOBQ5, DOBQ6, DOBQ7         | 134, 138, 2, 6, 14, 18, 26, 30     | In-phase (+) digital outputs second phase demultiplexer (channel Q) DOBQ0 is the LSB. DOBQ7 is the MSB                               |
| DOBQ0N, DOBQ1N, DOBQ2N, DOBQ3N, DOBQ4N, DOBQ5N, DOBQ6N, DOBQ7N | 133, 137, 1, 5, 13, 17, 25, 29     | Inverted phase (-) digital outputs second phase demultiplexer (channel Q) DOBQ0N is the LSB. DOBQ7N is the MSB                       |
| DOIRI                                                          | 75                                 | In-phase (+) out-of-range bit input (I phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256 |
| DOIRIN                                                         | 76                                 | Inverted phase of output signal DOIRI                                                                                                |
| DOIRQ                                                          | 34                                 | In-phase (+) out-of-range bit input (Q phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256 |
| DOIRQN                                                         | 33                                 | Inverted phase of output signal DOIRQ                                                                                                |
| MODE                                                           | 74                                 | Bit selection for 3-wire bus interface or nominal setting                                                                            |
| CLK                                                            | 73                                 | Input clock for 3-wire bus interface                                                                                                 |
| DATA                                                           | 72                                 | Input data for 3-wire bus                                                                                                            |
| LND                                                            | 71                                 | Beginning and end of register line for 3-wire bus interface                                                                          |
| CLKOI                                                          | 121                                | Output clock in-phase (+) channel I                                                                                                  |

**Table 10. AT84AD001B LQFP 144 Pin Description (Continued)**

| Symbol         | Pin number | Function                                                                 |
|----------------|------------|--------------------------------------------------------------------------|
| CLKOIN         | 122        | Inverted phase (-) output clock channel I                                |
| CLKOQ          | 132        | Output clock in-phase (+) channel Q,<br>1/2 input clock frequency        |
| CLKOQN         | 131        | Inverted phase (-) output clock channel Q                                |
| VtestQ, VtestI | 52, 53     | Pins for internal test (to be left open)                                 |
| Cal            | 70         | Calibration output bit status                                            |
| Vdiode         | 35         | Positive node of diode used for die<br>junction temperature measurements |

**Figure 14. AT84AD001B Pinout (Top View)**



## Typical Characterization Results

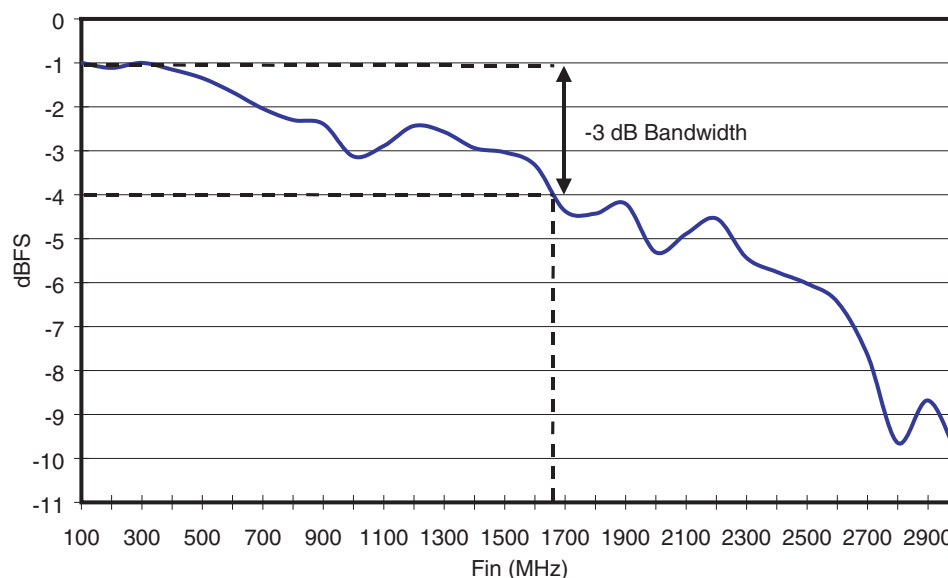
Nominal conditions (unless otherwise specified):

- $V_{CCA} = 3.3V$ ;  $V_{CCD} = 3.3V$ ;  $V_{CCO} = 2.25V$
- $V_{INI} - V_{INB}$  or  $V_{INQ}$  to  $V_{INQB} = 500$  mVpp full-scale differential input
- LVDS digital outputs ( $100\Omega$ )
- $T_A$  (typical) =  $25^\circ C$
- Full temperature range:  $0^\circ C < T_A < 70^\circ C$  (commercial grade) or  $-40^\circ C < T_A < 85^\circ C$  (industrial grade)

### Typical Full Power Input Bandwidth

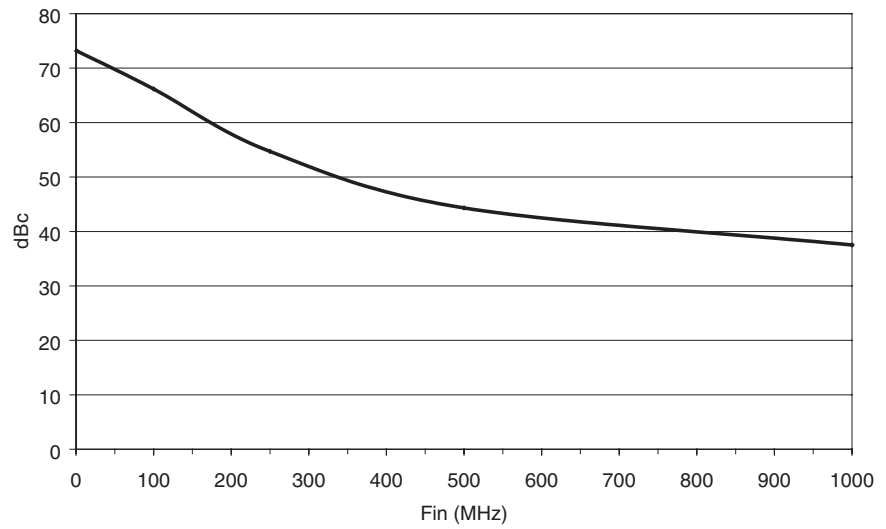
- $F_s = 500$  Msps
- $P_{clock} = 0$  dBm
- $P_{in} = -1$  dBFS
- Gain flatness ( $\pm 0.5$  dB) from DC to  $> 500$  MHz
- Full power input bandwidth at  $-3$  dB  $> 1.5$  GHz

**Figure 15.** Full Power Input Bandwidth



## Typical Crosstalk

**Figure 16.** Crosstalk ( $F_s = 500$  Msps)

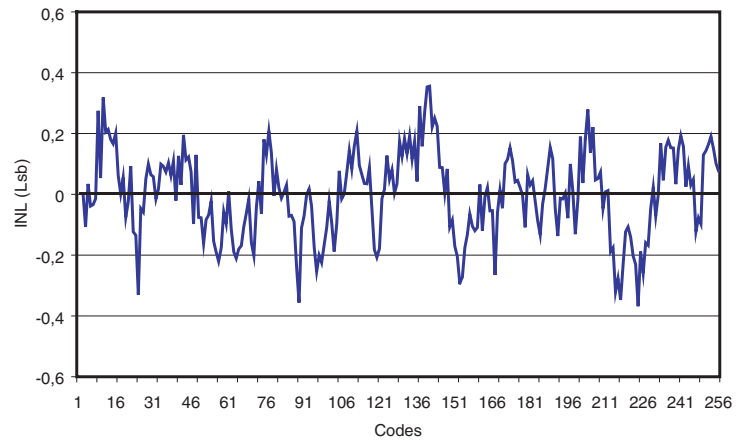


Note: Measured on the AT84AD001TD-EB Evaluation Board.

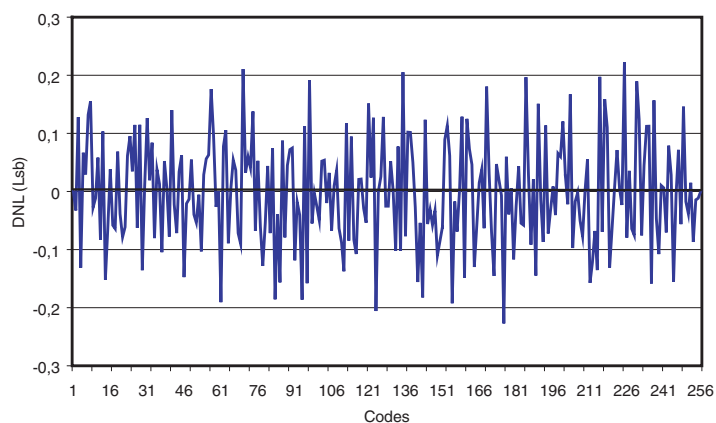
## Typical DC, INL and DNL Patterns

1:2 DMUX mode,  $F_s/4$  DR type

**Figure 17.** Typical INL ( $F_s = 50$  Msps,  $F_{in} = 1$  MHz, Saturated Input)

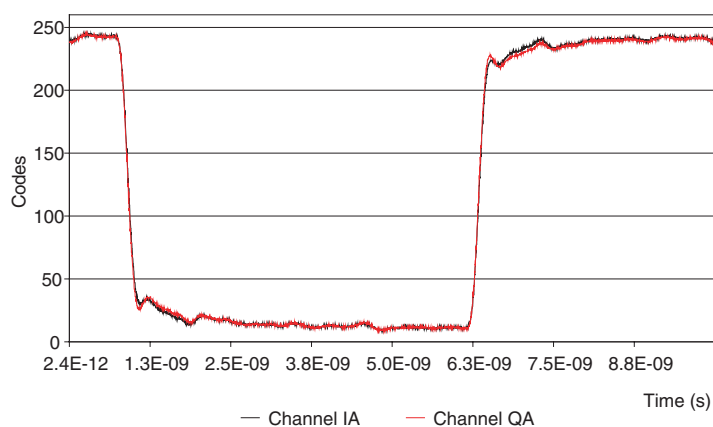


**Figure 18.** Typical DNL ( $F_s = 50$  Msps,  $F_{in} = 1$  MHz, Saturated Input)



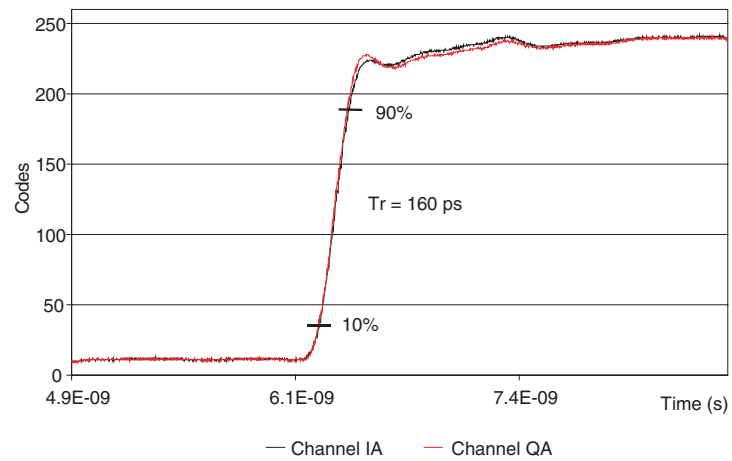
## Typical Step Response

**Figure 19.** Step Response



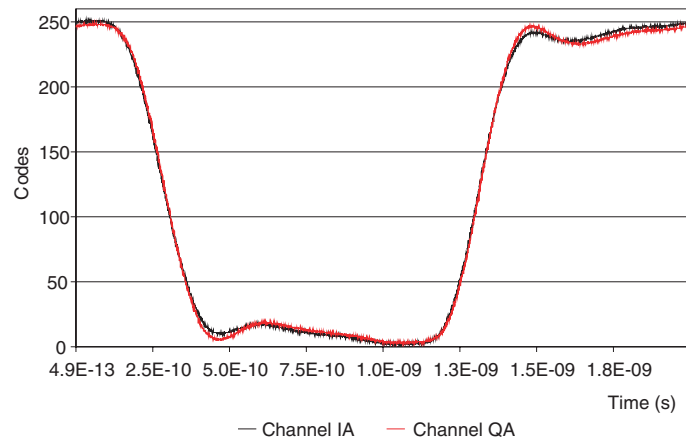
- $F_s = 1$  Gsps
- $P_{clock} = 0$  dBm
- $F_{in} = 100$  MHz
- $P_{in} = -1$  dBFS

**Figure 20. Step Response (Zoom)**

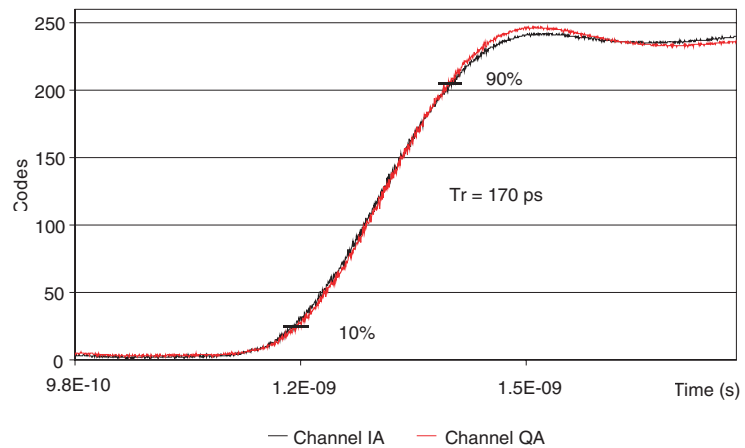


- $F_s = 1$  Gsps
- $P_{\text{clock}} = 0$  dBm
- $F_{\text{in}} = 500$  MHz
- $P_{\text{in}} = -1$  dBFS

**Figure 21. Step Response**

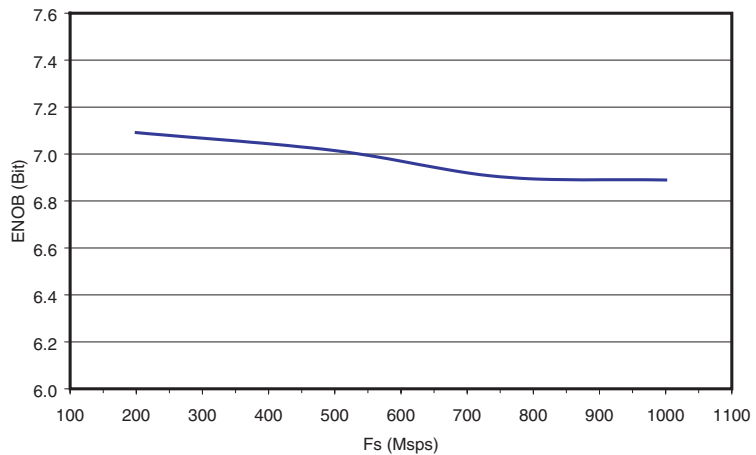


**Figure 22. Step Response (Zoom)**

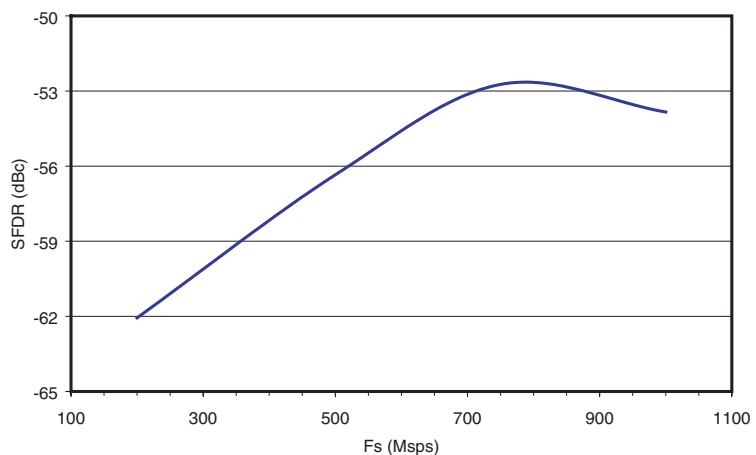


### Typical Dynamic Performances Versus Sampling Frequency

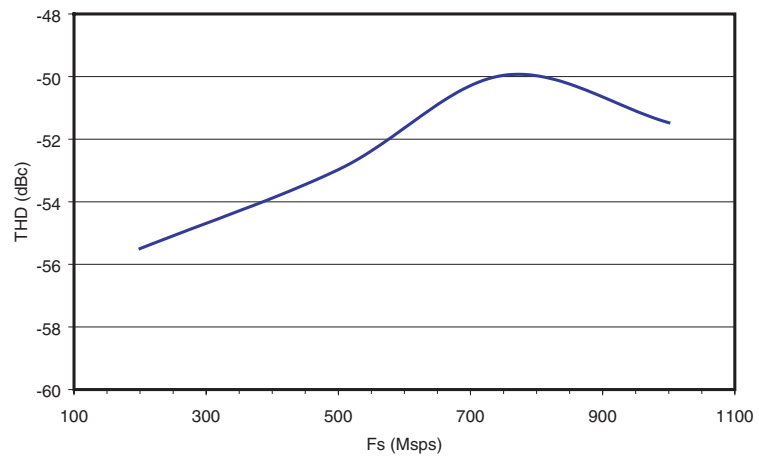
**Figure 23. ENOB Versus Sampling Frequency in Nyquist Conditions ( $F_{in} = F_s/2$ )**



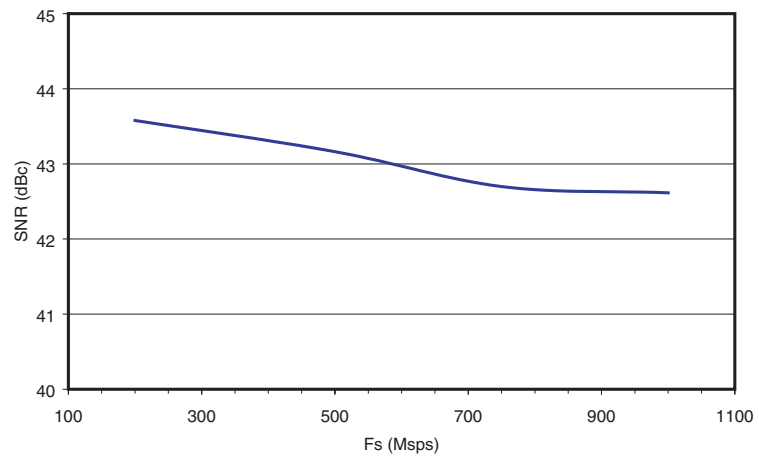
**Figure 24. SFDR Versus Sampling Frequency in Nyquist Conditions ( $F_{in} = F_s/2$ )**



**Figure 25.** THD Versus Sampling Frequency in Nyquist Conditions ( $F_{in} = F_s/2$ )

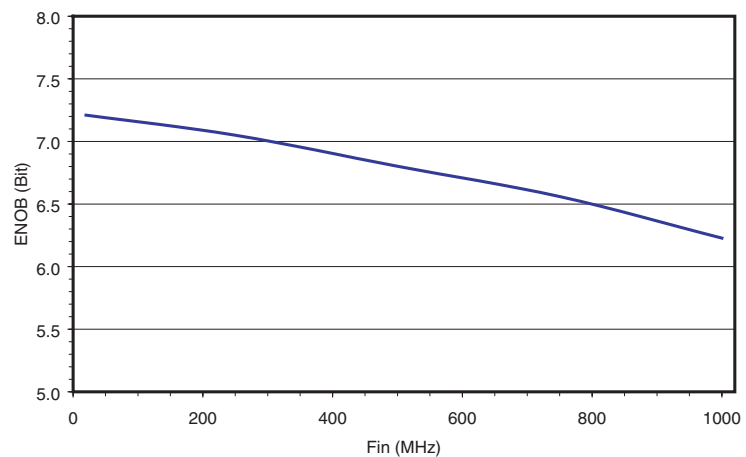


**Figure 26.** SNR Versus Sampling Frequency in Nyquist Conditions ( $F_{in} = F_s/2$ )

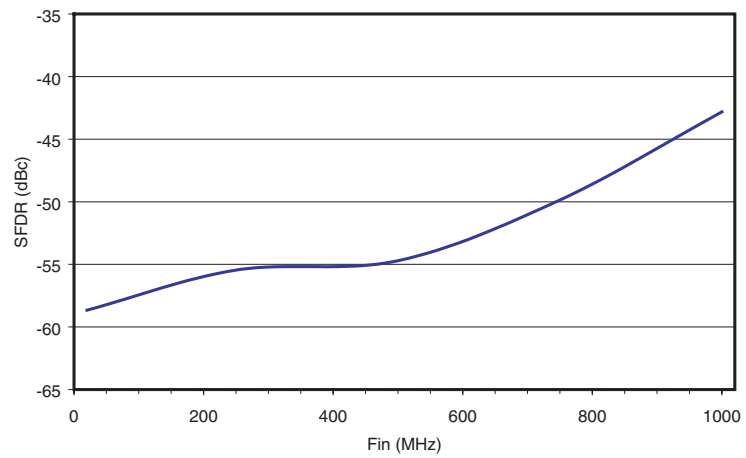


## Typical Dynamic Performances Versus Input Frequency

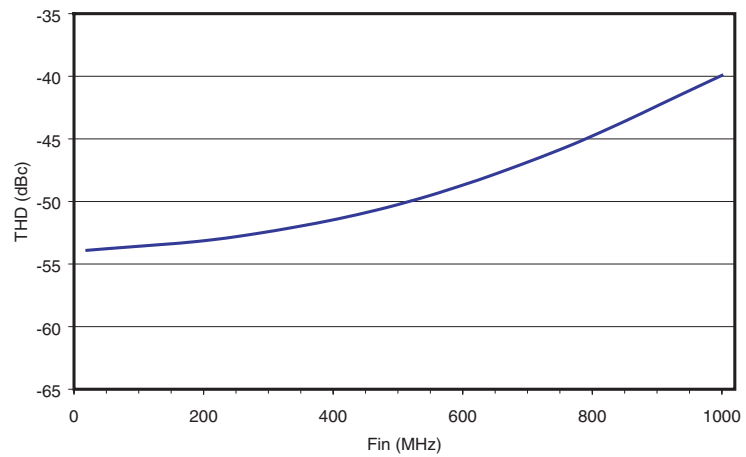
**Figure 27.** ENOB Versus Input Frequency ( $F_s = 1$  GSPS)



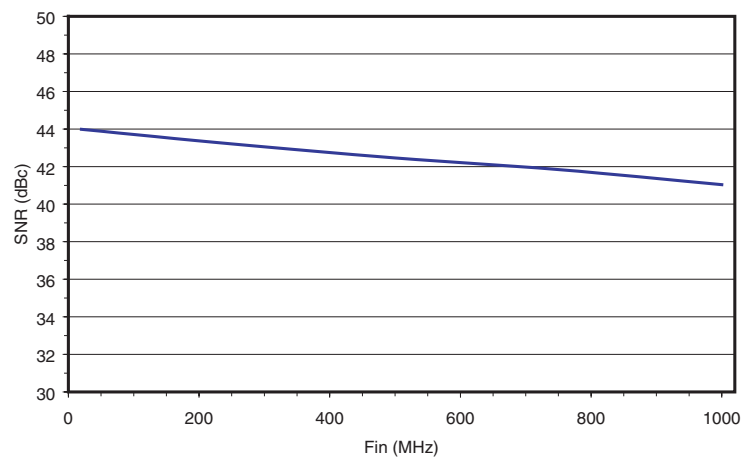
**Figure 28.** SFDR Versus Input Frequency ( $F_s = 1$  Gsps)



**Figure 29.** THD Versus Input Frequency ( $F_s = 1$  Gsps)

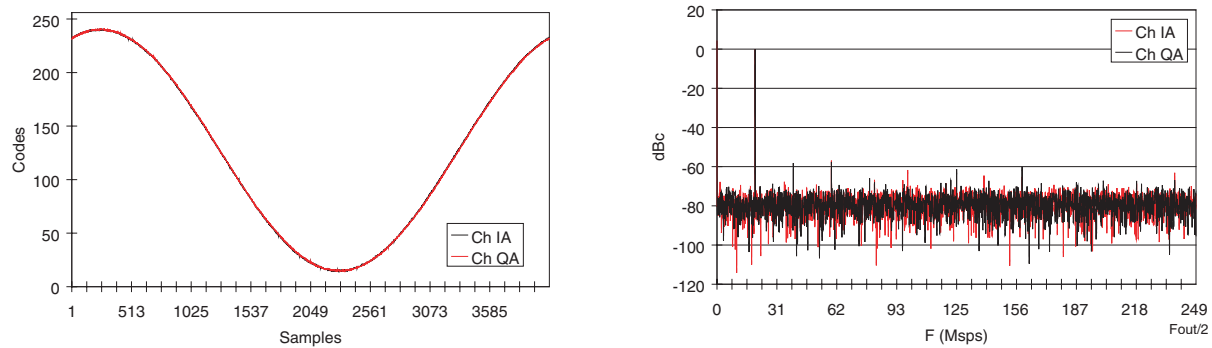


**Figure 30.** SNR Versus Input Frequency ( $F_s = 1$  Gsps)

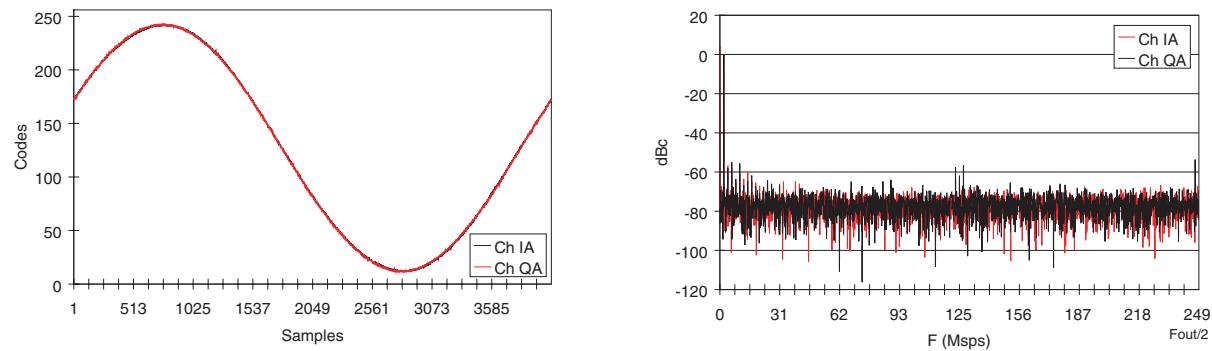


## Typical Reconstructed Signals and Signal Spectrum

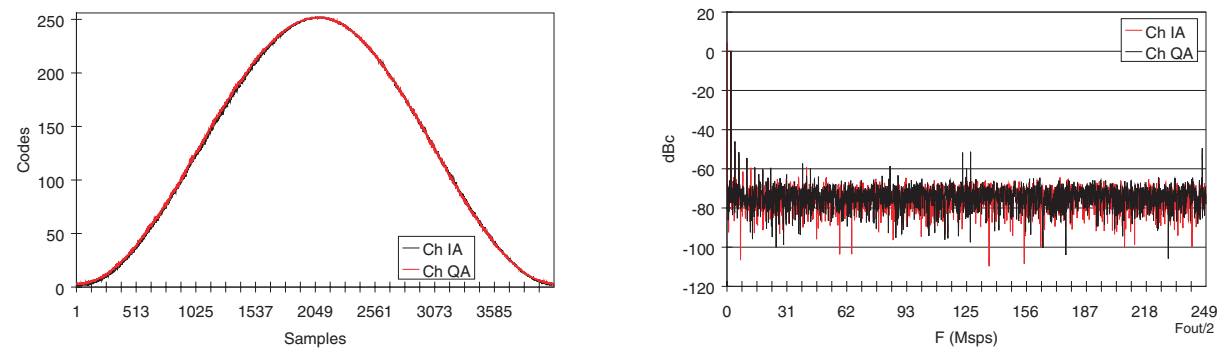
**Figure 31.**  $F_s = 1$  Gsps and  $F_{in} = 20$  MHz (1:2 DMUX,  $F_s/2$  DR Type,  $F_iSDA = -15$  ps,  $ISA = -50$  ps)



**Figure 32.**  $F_s = 1$  Gsps and  $F_{in} = 500$  MHz (1:2 DMUX,  $F_s/2$  DR Type,  $F_iSDA = -15$  ps,  $ISA = -50$  ps)

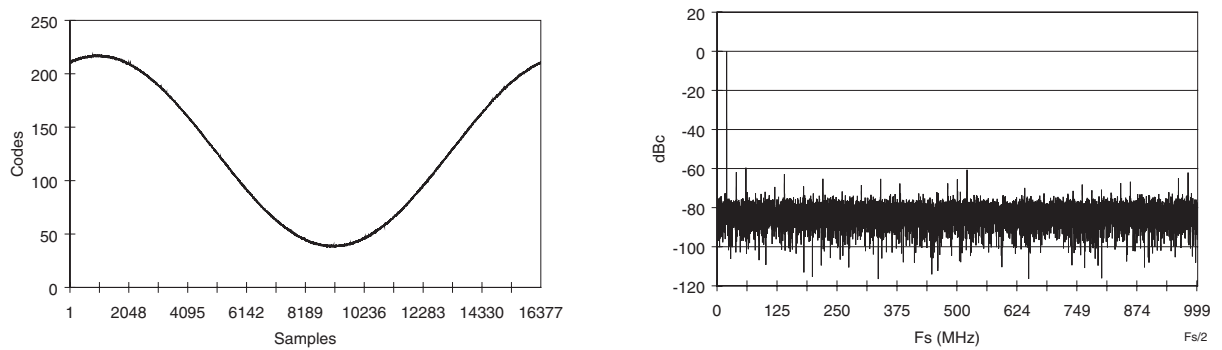


**Figure 33.**  $F_s = 1$  Gsps and  $F_{in} = 1$  GHz (1:2 DMUX,  $F_s/2$  DR Type,  $F_iSDA = -15$  ps,  $ISA = -50$  ps)

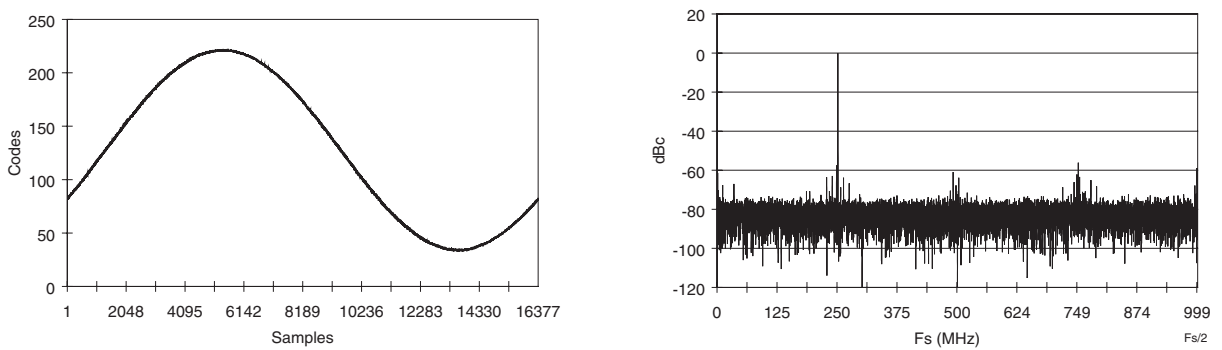


Note: The spectra are given with respect to the output clock frequency observed by the acquisition system (Figures 31 to 33).

**Figure 34.**  $F_s = 1$  Gsps and  $F_{in} = 20$  MHz (Interleaving Mode  $F_{int} = 2$  Gsps,  $F_s/4$  DR Type,  $F_iSDA = -15$  ps,  $ISA = -50$  ps)

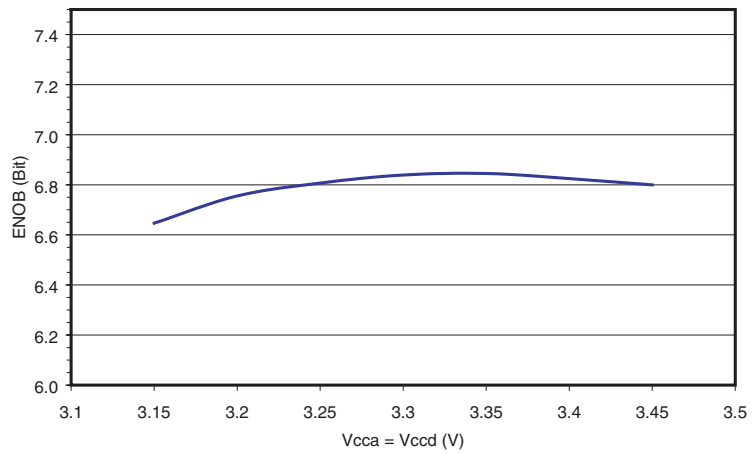


**Figure 35.**  $F_s = 1$  Gsps and  $F_{in} = 250$  MHz (Interleaving Mode  $F_{int} = 2$  Gsps,  $F_s/4$  DR Type,  $F_iSDA = -15$  ps,  $ISA = -50$  ps)

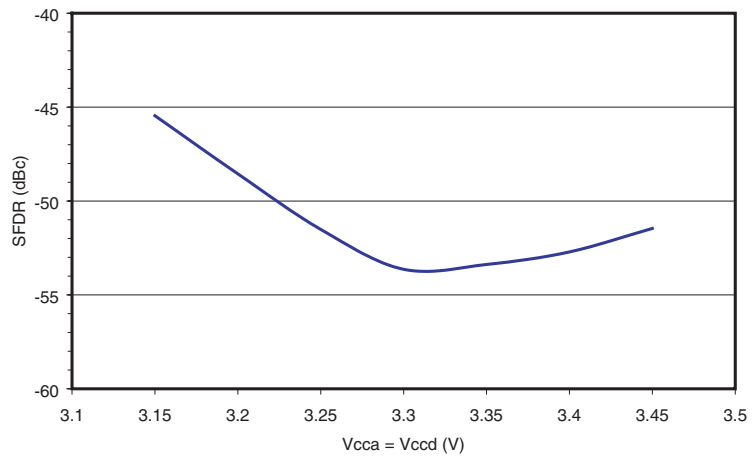


## Typical Performance Sensitivity Versus Power Supplies and Temperature

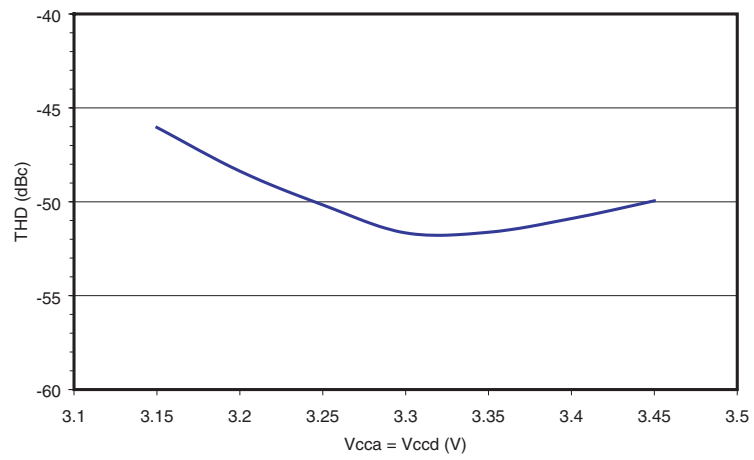
**Figure 36.** ENOB Versus  $V_{CCA} = V_{CCD}$  ( $F_s = 1$  Gsps,  $F_{in} = 500$  MHz, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



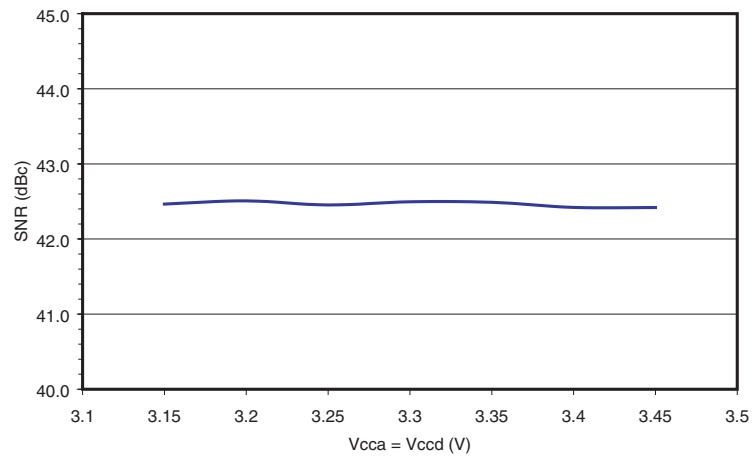
**Figure 37.** SFDR Versus  $V_{CCA} = V_{CCD}$  ( $F_s = 1$  Gsps,  $F_{in} = 500$  MHz, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



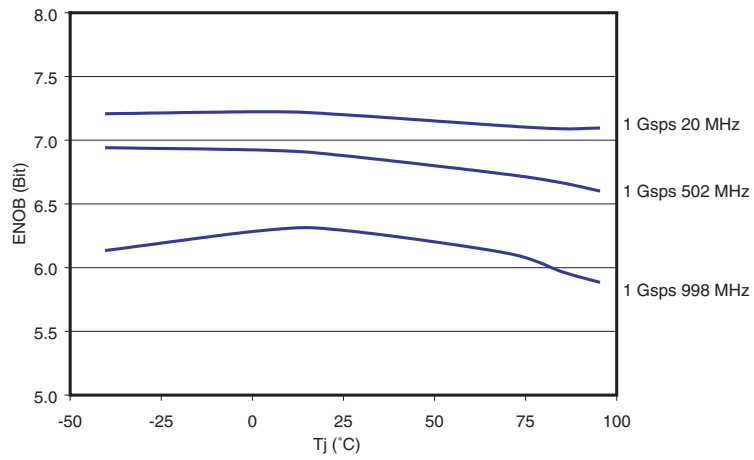
**Figure 38.** THD Versus  $V_{CCA} = V_{CCD}$  ( $F_s = 1$  Gsps,  $F_{in} = 500$  MHz, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



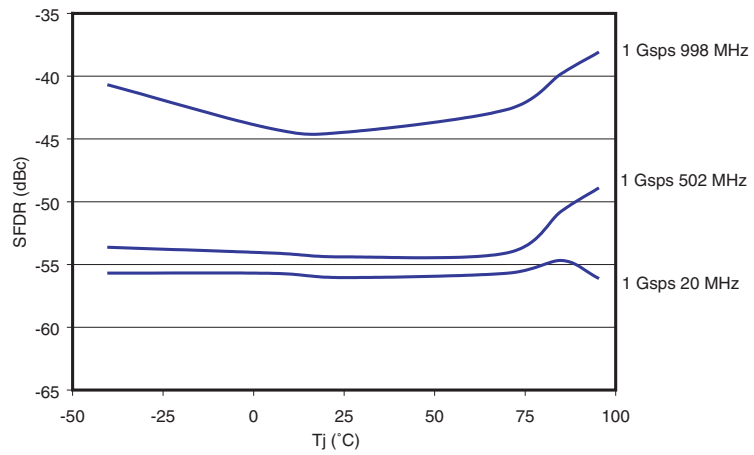
**Figure 39.** SNR Versus  $V_{CCA} = V_{CCD}$  ( $F_s = 1$  Gsps,  $F_{in} = 500$  MHz, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



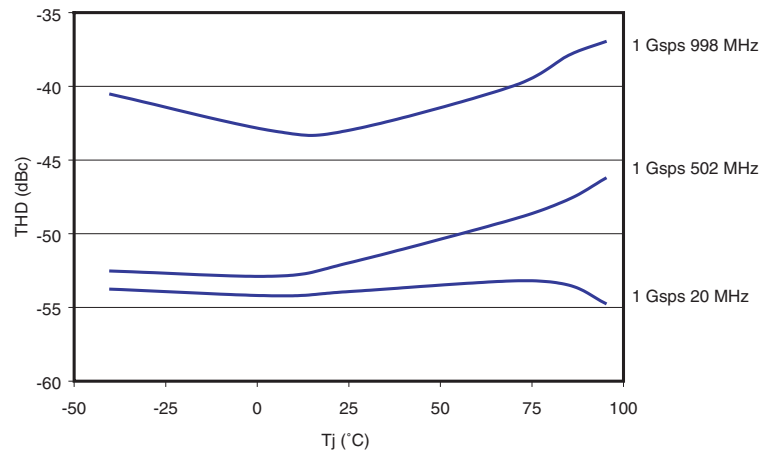
**Figure 40.** ENOB Versus Junction Temperature ( $F_s = 1$  Gsps, 1:2 DMUX,  $F_s/4$  DR Type, ISA = -50 ps)



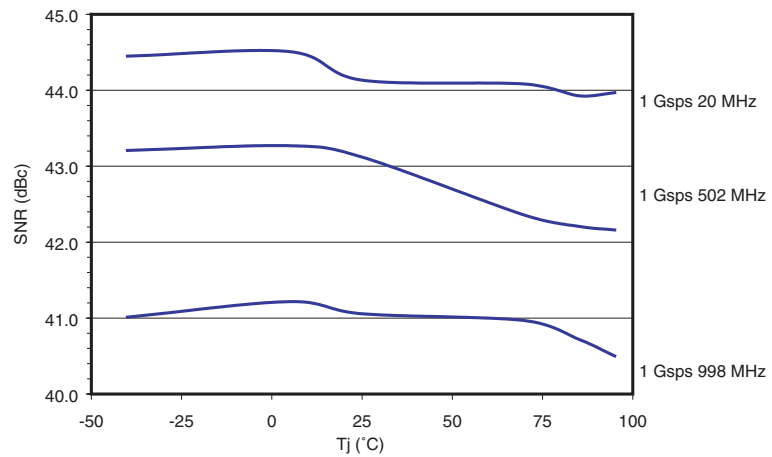
**Figure 41.** SFDR Versus Junction Temperature ( $F_s = 1$  Gsps, 1:2 DMUX,  $F_s/4$  DR Type, ISA = -50 ps)



**Figure 42.** THD Versus Junction Temperature ( $F_s = 1$  Gsps, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



**Figure 43.** SNR Versus Junction Temperature ( $F_s = 1$  Gsps, 1:2 DMUX,  $F_s/4$  DR Type,  $ISA = -50$  ps)



## Test and Control Features

### 3-wire Serial Interface Control Setting

**Table 11.** 3-wire Serial Interface Control Settings

| Mode             | Characteristics                                                                                                                                                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Mode = 1 (2.25V) | 3-wire serial bus interface activated                                                                                                                                                                                                                                                                   |
| Mode = 0 (0V)    | 3-wire serial bus interface deactivated<br>Nominal setting:<br>Dual channel I and Q activated<br>One clock I<br>0 dB gain<br>DMUX mode 1:1<br>DRDA I & Q = 0 ps<br>ISA I & Q = 0 ps<br>FiSDA Q = 0 ps<br>Binary output<br>Decimation test mode OFF<br>Calibration setting OFF<br>Data Ready = $F_s / 2$ |

## 3-wire Serial Interface and Data Description

The 3-wire bus is activated with the control bit mode set to 1. The length of the word is 19 bits: 16 for the data and 3 for the address. The maximum clock frequency is 50 MHz.

**Table 12.** 3-wire Serial Interface Address Setting Description

| Address | Setting                                                                                                                                                                                                                                                                                                   |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 000     | <b>Standby</b><br>Gray/binary mode<br>1:1 or 1:2 DMUX mode<br>Analog input MUX<br>Clock selection<br>Auto-calibration<br>Decimation test mode<br>Data Ready Delay Adjust                                                                                                                                  |
| 001     | <b>Analog gain adjustment</b><br>Data7 to Data0: gain channel I<br>Data15 to Data8: gain channel Q<br>Code 00000000: -1.5 dB<br>Code 10000000: 0 dB<br>Code 11111111: 1.5 dB<br>Steps: 0.011 dB                                                                                                           |
| 010     | <b>Offset compensation</b><br>Data7 to Data0: offset channel I<br>Data15 to Data8: offset channel Q<br>Data7 and Data15: sign bits<br>Code 11111111b: 31.75 LSB<br>Code 10000000b: 0 LSB<br>Code 00000000b: 0 LSB<br>Code 01111111b: -31.75 LSB<br>Steps: 0.25 LSB<br>Maximum correction: $\pm 31.75$ LSB |
| 011     | <b>Gain compensation</b><br>Data6 to Data0: channel I/Q (Q is matched to I)<br>Code 11111111b: -0.315 dB<br>Code 10000000b: 0 dB<br>Code 00000000b: 0 dB<br>Code 01111111b: 0.315 dB<br>Steps: 0.005 dB<br>Data6: sign bit                                                                                |
| 100     | <b>Internal Settling Adjustment (ISA)</b><br>Data2 to Data0: channel I<br>Data5 to Data3: channel Q<br>Data15 to Data6: 1000010000                                                                                                                                                                        |



| Address | Setting                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 101     | <b>Testability</b><br>Data3 to Data0 = 0000<br>Mode S/H transparent                      OFF: Data4 = 0                      ON: Data4 = 1<br>Data7 = 0<br>Data8 = 0                                                                                                                                                                                                                                                                                            |
| 110     | <b>Built-In Test (BIT)</b><br>Data0 = 0              BIT Inactive                      Data0 = 1                      BIT Active<br>Data1 = 0              Static BIT                      Data1 = 1                      Dynamic BIT<br>If Data1 = 1, then Ports BI & BQ = Rising Ramp<br>Ports AI & AQ = Decreasing Ramp<br>If Data1 = 0, then Data2 to Data9 = Static Data for BIT<br>Ports BI & BQ = Data2 to Data9<br>Ports AI & AQ = NOT (Data2 to Data9) |
| 111     | <b>Data Ready Delay Adjust (DRDA)</b><br>Data2 to Data0: clock I<br>Data5 to Data3: clock Q<br>Steps: 140 ps<br>000: -560 ps<br>100: 0 ps<br>111: 420 ps<br><br><b>Fine Sampling Delay Adjustment (FiSDA) on channel Q</b><br>Data10 to Data6: channel Q<br>Steps: 5 ps<br>Data4: sign bit<br>Code 11111: -75 ps<br>Code 10000: 0 ps<br>Code 00000: 0 ps<br>Code 01111: 75 ps                                                                                   |

Notes:

1. The Internal Settling Delay Adjustment could change independently of the two analog sampling times (TA channels I and Q) of the sample/hold (with a fixed digital sampling time) with steps of  $\pm 50$  ps:  
Nominal mode will be given by Data2...Data0 = 100 or Data5...Data3 = 100.  
Data5...Data3 = 000 or Data2...Data0 = 000: sampling time is -200 ps compared to nominal.  
Data2...Data0 = 111 or Data5...Data3 = 111: sampling time is 150 ps compared to nominal.  
We recommend setting the ISA to -50 ps to optimize the ADC's dynamic performances.
2. The Fine Sampling Delay Adjustment enables you to change the sampling time (steps of  $\pm 5$  ps) on channel Q more precisely, particularly in the interleaved mode.
3. A Built-In Test (BIT) function is available to rapidly test the device's I/O by either applying a defined static pattern to the dual ADC or by generating a dynamic ramp at the output of the dual ADC. This function is controlled via the 3-wire bus interface at the address 110. The maximum clock frequency in dynamic BIT mode is 750 Msps.  
Please refer to "Built-In Test (BIT)" on page 43 for more information about this function.
4. The decimation mode enables you to lower the output bit rate (including the output clock rate) by a factor of 16, while the internal clock frequency remains unchanged. The maximum clock frequency in decimation mode is 750 Msps.
5. The "S/H transparent" mode (address 101, Data4) enables bypassing of the ADC's track/hold. This function optimizes the ADC's performances at very low input frequencies ( $F_{in} < 50$  MHz).
6. In the Gray mode, when the input signal is overflow (that is, the differential analog input is greater than 250 mV), the output data must be corrected using the output DOIR:  
If DOIR = 1: Data7 unchanged  
Data6 = 0, Data5 = 0, Data4 = 0, Data3 = 0, Data2 = 0, Data1 = 0, Data0 = 0.  
In 1:2 DMUX mode, only one out-of-range bit is provided for both A and B ports.

**Table 13. 3-wire Serial Interface Data Setting Description**

| Setting for Address:<br>000                                                      | D15 | D14 | D13 | D12 | D11 | D10 | D9 <sup>(1)</sup> | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-------------------|----|----|----|----|----|----|----|----|----|
| Full standby mode                                                                | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | 1  | 1  |
| Standby channel I <sup>(2)</sup>                                                 | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | 0  | 1  |
| Standby channel Q <sup>(3)</sup>                                                 | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | 1  | 0  |
| No standby mode                                                                  | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | 0  | 0  |
| Binary output mode                                                               | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | 1  | X  | X  |
| Gray output mode                                                                 | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | 0  | X  | X  |
| DMUX 1:2 mode                                                                    | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | 1  | X  | X  | X  |
| DMUX 1:1 mode                                                                    | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | 0  | X  | X  | X  |
| Analog selection mode<br>Input I →ADC I<br>Input Q →ADC Q                        | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | 1  | 1  | X  | X  | X  | X  |
| Analog selection mode<br>Input I →ADC I<br>Input I →ADC Q                        | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | 1  | 0  | X  | X  | X  | X  |
| Analog selection mode<br>Input Q →ADC I<br>Input Q →ADC Q                        | X   | X   | X   | X   | X   | X   | 0                 | X  | X  | X  | 0  | X  | X  | X  | X  | X  |
| Clock Selection mode<br>CLKI →ADC I<br>CLKQ →ADC Q                               | X   | X   | X   | X   | X   | X   | 0                 | X  | 1  | 1  | X  | X  | X  | X  | X  | X  |
| Clock selection mode<br>CLKI →ADC I<br>CLKI →ADC Q                               | X   | X   | X   | X   | X   | X   | 0                 | X  | 1  | 0  | X  | X  | X  | X  | X  | X  |
| Clock selection mode<br>CLKI →ADC I<br>CLKIN →ADC Q                              | X   | X   | X   | X   | X   | X   | 0                 | X  | 0  | X  | X  | X  | X  | X  | X  | X  |
| Decimation OFF mode                                                              | X   | X   | X   | X   | X   | X   | 0                 | 0  | X  | X  | X  | X  | X  | X  | X  | X  |
| Decimation ON mode                                                               | X   | X   | X   | X   | X   | X   | 0                 | 1  | X  | X  | X  | X  | X  | X  | X  | X  |
| Keep last calibration<br>calculated value <sup>(4)</sup><br>No calibration phase | X   | X   | X   | X   | 0   | 1   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |
| No calibration phase <sup>(5)</sup><br>No calibration value                      | X   | X   | X   | X   | 0   | 0   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |
| Start a new calibration<br>phase                                                 | X   | X   | X   | X   | 1   | 1   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |

**Table 13. 3-wire Serial Interface Data Setting Description (Continued)**

| Setting for Address:<br>000                    | D15 | D14 | D13 | D12 | D11 | D10 | D9 <sup>(1)</sup> | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------------------------------|-----|-----|-----|-----|-----|-----|-------------------|----|----|----|----|----|----|----|----|----|
| Control wait bit<br>calibration <sup>(6)</sup> | X   | X   | a   | b   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |
| In 1:2 DMUX<br>FDataReady<br>I & Q = Fs/2      | X   | 0   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |
| In 1:2 DMUX<br>FDataReady<br>I & Q = Fs/4      | X   | 1   | X   | X   | X   | X   | 0                 | X  | X  | X  | X  | X  | X  | X  | X  | X  |

- Notes:
1. D9 must be set to "0"
  2. Mode standby channel I: use analog input I Vini, Vinib and Clocki.
  3. Mode standby channel Q: use analog input Q Vinq, Vinqb and Clockq.
  4. Keep last calibration calculated value - no calibration phase: D11 = 0 and D10 = 1. No new calibration is required. The values taken into account for the gain and offset are either from the last calibration phase or are default values (reset values).
  5. No calibration phase - no calibration value: D11 = 0 and D10 = 0. No new calibration phase is required. The gain and offset compensation functions can be accessed externally by writing in the registers at address 010 for the offset compensation and at address 011 for the gain compensation.
  6. The control wait bit gives the possibility to change the internal setting for the auto-calibration phase:  
For high clock rates (> 500 Msps) use a = b = 1.  
For clock rates > 250 Msps and < 500 Msps use a = 1 and b = 0.  
For clock rates > 125 Msps and < 250 Msps use a = 0 and b = 1.  
For low clock rates < 125 Msps use a = 0 and b = 0.

### 3-wire Serial Interface Timing Description

The 3-wire serial interface is a synchronous write-only serial interface made of three wires:

- sclk: serial clock input
- sldn: serial load enable input
- sdata: serial data input

The 3-wire serial interface gives write-only access to as many as 8 different internal registers of up to 16 bits each. The input format is always fixed with 3 bits of register address followed by 16 bits of data. The data and address are entered with the Most Significant Bit (MSB) first.

The write procedure is fully synchronous with the rising clock edge of "sclk" and described in the write chronogram (Figure 44 on page 41).

- "sldn" and "sdata" are sampled on each rising clock edge of "sclk" (clock cycle).
- "sldn" must be set to 1 when no write procedure is performed.
- A minimum of one rising clock edge (clock cycle) with "sldn" at 1 is required for a correct start of the write procedure.
- A write starts on the first clock cycle with "sldn" at 0. "sldn" must stay at 0 during the complete write procedure.
- During the first 3 clock cycles with "sldn" at 0, 3 bits of the register address from MSB (a[2]) to LSB (a[0]) are entered.
- During the next 16 clock cycles with "sldn" at 0, 16 bits of data from MSB (d[15]) to LSB (d[0]) are entered.
- An additional clock cycle with "sldn" at 0 is required for parallel transfer of the serial data d[15:0] into the addressed register with address a[2:0]. This yields 20 clock cycles with "sldn" at 0 for a normal write procedure.

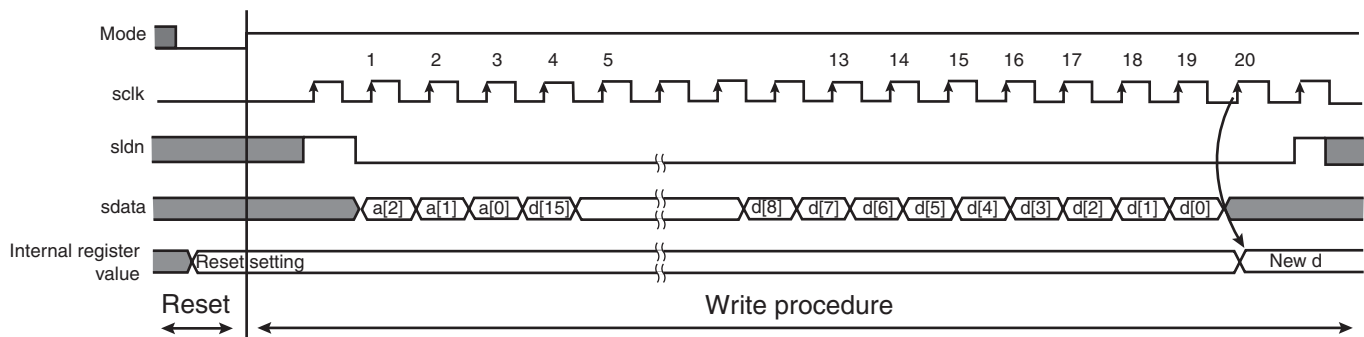
- A minimum of one clock cycle with “sldn” returned at 1 is requested to close the write procedure and make the interface ready for a new write procedure. Any clock cycle where “sldn” is at 1 *before* the write procedure is completed interrupts this procedure and no further data transfer to the internal registers is performed.
- Additional clock cycles with “sldn” at 0 *after* the parallel data transfer to the register (done at the 20th consecutive clock cycle with “sldn” at 0) do not affect the write procedure and are ignored.

It is possible to have only one clock cycle with “sldn” at 1 between two following write procedures.

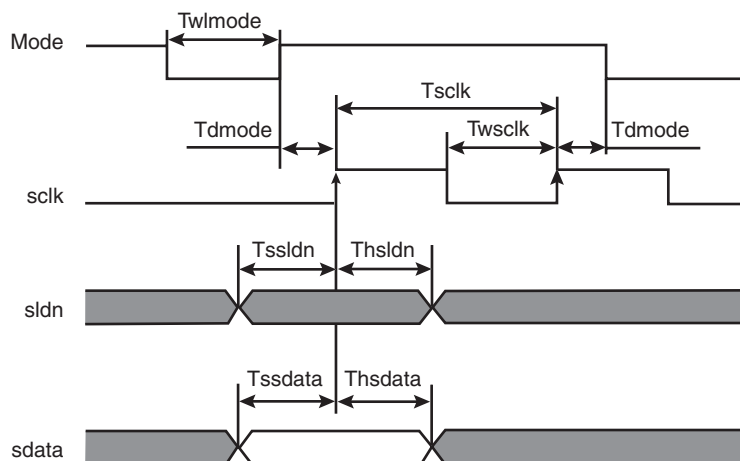
- 16 bits of data must always be entered even if the internal addressed register has less than 16 bits. Unused bits (usually MSBs) are ignored. Bit signification and bit positions for the internal registers are detailed in Table 12 on page 37.

To reset the registers, the Pin mode can be used as a reset pin for chip initialization, even when the 3-wire serial interface is used.

**Figure 44. Write Chronogram**



**Figure 45. Timing Definition**



**Table 14.** Timing Description

| Name    | Parameter                                                         | Value |     |     | Unit |
|---------|-------------------------------------------------------------------|-------|-----|-----|------|
|         |                                                                   | Min   | Typ | Max |      |
| Tsclk   | Sclk period                                                       | 20    |     |     | ns   |
| Twsclk  | High or low time of sclk                                          | 5     |     |     | ns   |
| Tssldn  | Setup time of sldn before rising edge of sclk                     | 4     |     |     | ns   |
| Thsldn  | Hold time of sldn after rising edge of sclk                       | 2     |     |     | ns   |
| Tssdata | Setup time of sdata before rising edge of sclk                    | 4     |     |     | ns   |
| Thsdata | Hold time of sdata after rising edge of sclk                      | 2     |     |     | ns   |
| Twlmode | Minimum low pulse width of mode                                   | 5     |     |     | ns   |
| Tdmode  | Minimum delay between an edge of mode and the rising edge of sclk | 10    |     |     | ns   |

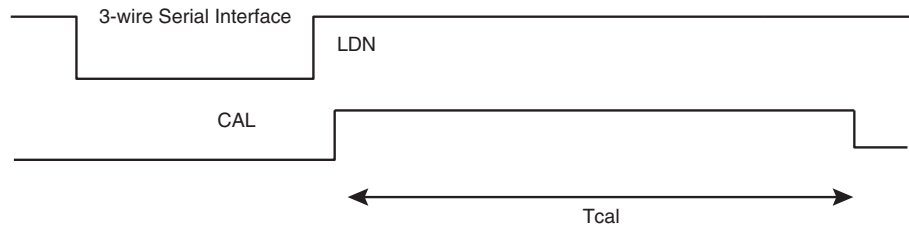
### Calibration Description

The AT84AD001B offers the possibility of reducing offset and gain matching between the two ADC cores. An internal digital calibration may start right after the 3-wire serial interface has been loaded (using data D12 of the 3-wire serial interface with address 000).

The beginning of calibration disables the two ADCs and a standard data acquisition is performed. The output bit CAL goes to a high level during the entire calibration phase. When this bit returns to a low level, the two ADCs are calibrated with offset and gain and can be used again for a standard data acquisition.

If only one channel is selected (I or Q) the offset calibration duration is divided by two and no gain calibration between the two channels is necessary.

**Figure 46.** Internal Timing Calibration



The Tcal duration is a multiple of the clock frequency ClockI (master clock). Even if a dual clock scheme is used during calibration, ClockQ will not be used.

The control wait bits (D13 and D14) give the possibility of changing the calibration's setting depending on the clock's frequency:

- For high clock rates (> 500 Msps) use a = b = 1, Tcal = 10112 clock I periods.
- For clock rates > 250 Msps and < 500 Msps use a = 1, b = 0, Tcal = 6016 clock I periods.
- For clock rates > 125 Msps and < 250 Msps use a = 0, b = 1, Tcal = 3968 clock I periods.
- For low clock rates (< 125 Msps) use a = 0, b = 0, Tcal = 2944 clock I periods.

The calibration phase is necessary when using the AT84AD001B in interlace mode, where one analog input is sampled at both ADC cores on the common input clock's rising and falling edges. This operation is equivalent to converting the analog signal at twice the clock frequency

**Table 15.** Matching Between Channels

| Parameter                                                    | Value |       |     | Unit |
|--------------------------------------------------------------|-------|-------|-----|------|
|                                                              | Min   | Typ   | Max |      |
| Gain error (single channel I or Q) without calibration       |       | 0     |     | LSB  |
| Gain error (single channel I or Q) with calibration          | -0.5  | 0     | 0.5 | LSB  |
| Offset error (single channel I or Q) without calibration     |       | 0     |     | LSB  |
| Offset error (single channel I or Q) with calibration        | -0.5  | 0     | 0.5 | LSB  |
| Mean offset code without calibration (single channel I or Q) |       | 127.5 |     |      |
| Mean offset code with calibration (single channel I or Q)    | 127   | 127.5 | 128 |      |

During the ADC's auto-calibration phase, the dual ADC is set with the following:

- Decimation mode ON
- 1:1 DMUX mode
- Binary mode

Any external action applied to any signal of the ADC's registers is inhibited during the calibration phase.

#### Gain and Offset Compensation Functions

It is also possible for the user to have external access to the ADC's gain and offset compensation functions:

- Offset compensation between I and Q channels (at address 010)
- Gain compensation between I and Q channels (at address 011)

To obtain manual access to these two functions, which are used to set the offset to middle code 127.5 and to match the gain of channel Q with that of channel I (if only one channel is used, the gain compensation does not apply), it is necessary to set the ADC to "manual" mode by writing 0 at bits D11 and D10 of address 000.

#### Built-In Test (BIT)

A Built-In Test (BIT) function is available to allow rapid testing of the device's I/O by either applying a defined static pattern to the ADC or by generating a dynamic ramp at the ADC's output. The dynamic ramp can be used with a clock frequency of up to 750 Msps. This function is controlled via the 3-wire bus interface at address 101.

- The BIT is active when Data0 = 1 at address 110.
- The BIT is inactive when Data0 = 0 at address 110.
- The Data1 bit allows choosing between static mode (Data1 = 0) and dynamic mode (Data1 = 1).

When the static BIT is selected (Data1 = 0), it is possible to write any 8-bit pattern by defining the Data9 to Data2 bits. Port B then outputs an 8-bit pattern equal to Data9 ... Data2, and Port A outputs an 8-bit pattern equal to NOT (Data9 ... Data2).

### Example:

Address = 110

Data =

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| X   | X   | X   | X   | X   | X   | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  |

One should then obtain 01010101 on Port B and 10101010 on Port A.

When the dynamic mode is chosen (Data1 = 1) port B outputs a rising ramp while Port A outputs a decreasing one.

Note: In dynamic mode, use the DRDA function to align the edges of CLK0 with the middle of the data.

### Decimation Mode

The decimation mode is provided to enable rapid testing of the ADC at a maximum clock frequency of 750 Msp. In decimation mode, one data out of 16 is output, thus leading to a maximum output rate of 46.875 Msp.

Note: Frequency (CLK0) = frequency (Data) = Frequency (CLKI)/16.

### Die Junction Temperature Monitoring Function

A die junction temperature measurement setting is included on the board for junction temperature monitoring.

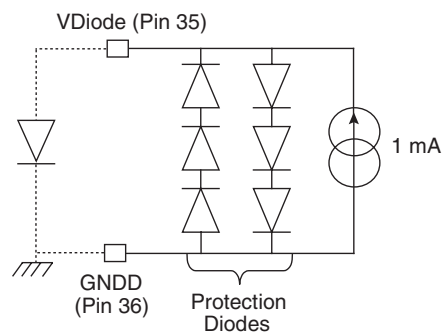
The measurement method forces a 1 mA current into a diode-mounted transistor.

Caution should be given to respecting the polarity of the current.

In any case, one should make sure the maximum voltage compliance of the current source is limited to a maximum of 1V or use a resistor serial-mounted with the current source to avoid damaging the transistor device (this may occur if the current source is reverse-connected).

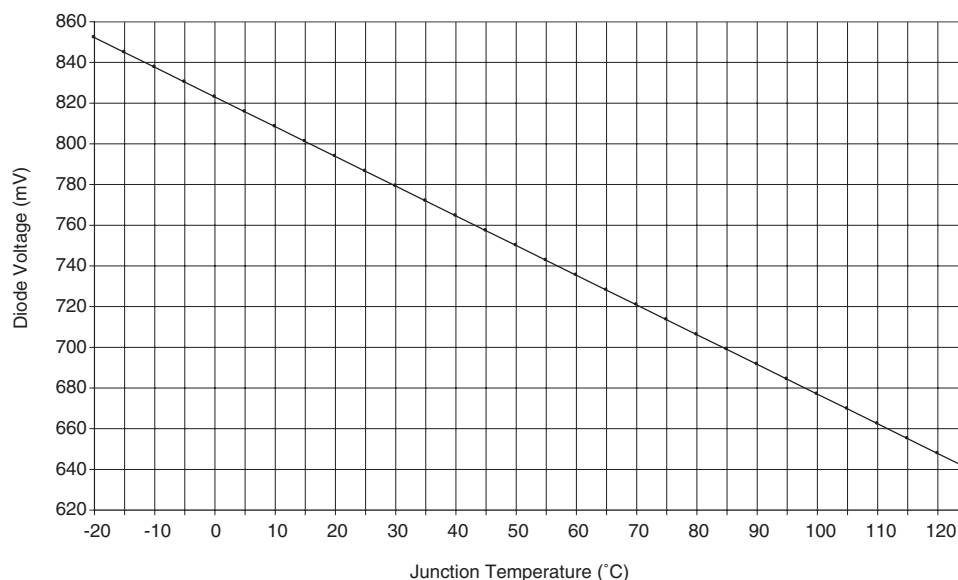
The measurement setup is illustrated in Figure 47.

**Figure 47.** Die Junction Temperature Monitoring Setup



The VBE diode's forward voltage in relation to the junction temperature (in steady-state conditions) is shown in Figure 48.

**Figure 48.** Diode Characteristics Versus  $T_J$

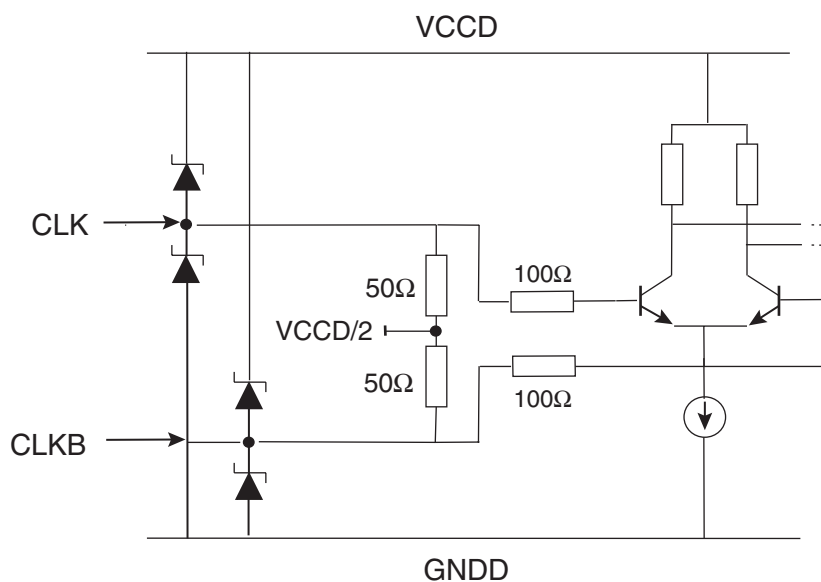


## VtestI, VtestQ

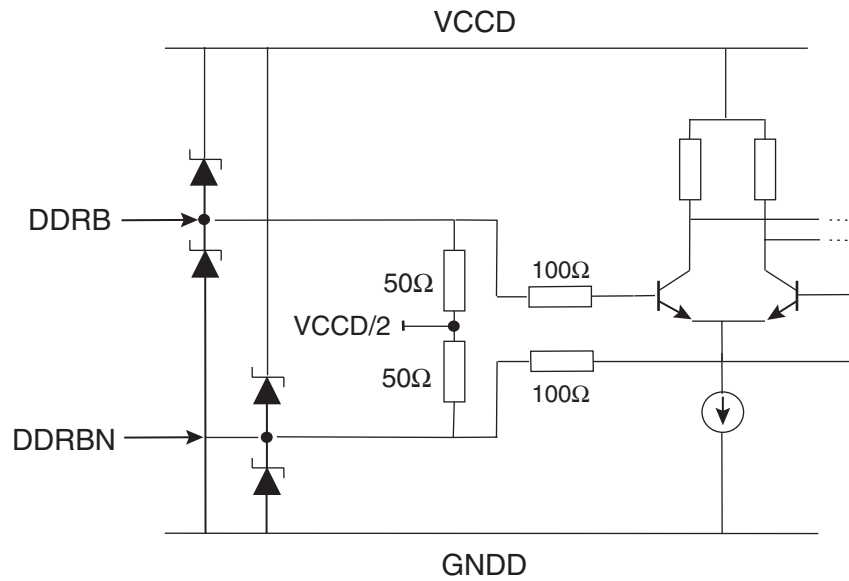
VtestI and VtestQ pins are for internal test use only. These two signals must be left open.

## Equivalent Input/Output Schematics

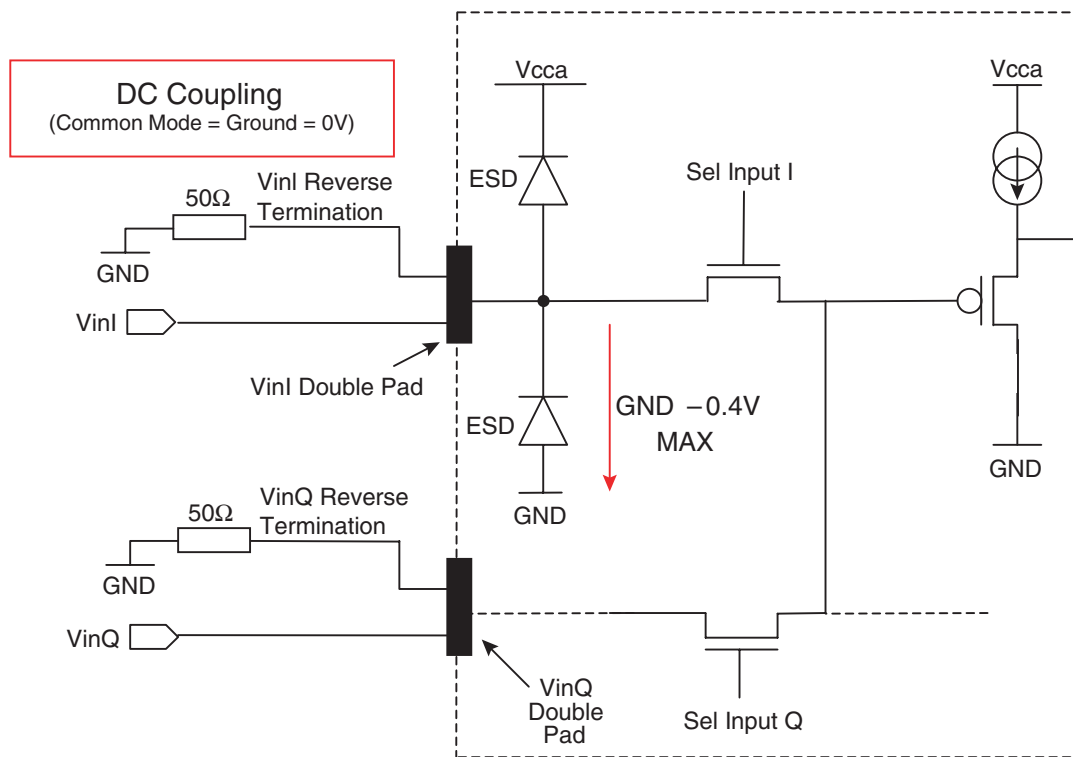
**Figure 49.** Simplified Input Clock Model



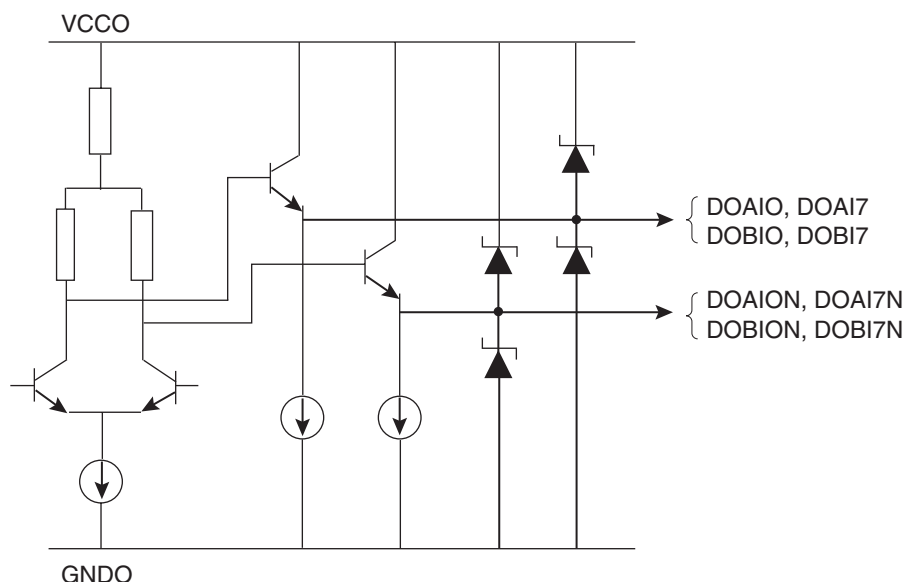
**Figure 50.** Simplified Data Ready Reset Buffer Model



**Figure 51.** Analog Input Model



**Figure 52.** Data Output Buffer Model



## Definitions of Terms

**Table 16.** Definitions of Terms

| Abbreviation | Definition                  | Description                                                                                                                                                                                                                                                                                                                                                                              |
|--------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BER          | Bit Error Rate              | The probability to exceed a specified error threshold for a sample at a maximum specified sampling rate. An error code is a code that differs by more than $\pm 4$ LSB from the correct code                                                                                                                                                                                             |
| DNL          | Differential Non-Linearity  | The differential non-linearity for an output code $i$ is the difference between the measured step size of code $i$ and the ideal LSB step size. DNL ( $i$ ) is expressed in LSBs. DNL is the maximum value of all DNL ( $i$ ). A DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic                |
| ENOB         | Effective Number of Bits    | $ENOB = \frac{SINAD - 1.76 + 20 \log \left[ \frac{A}{F_s/2} \right]}{6.02}$ Where A is the actual input amplitude and $F_s$ is the full scale range of the ADC under test                                                                                                                                                                                                                |
| FPBW         | Full Power Input Bandwidth  | The analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale -1 dB (-1 dBFS)                                                                                                                                             |
| IMD          | Inter-Modulation Distortion | The two tones intermodulation distortion (IMD) rejection is the ratio of either of the two input tones to the worst third order intermodulation products                                                                                                                                                                                                                                 |
| INL          | Integral Non-Linearity      | The integral non-linearity for an output code $i$ is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL ( $i$ ) is expressed in LSBs and is the maximum value of all INL ( $i$ )                                                                                                                               |
| JITTER       | Aperture uncertainty        | The sample-to-sample variation in aperture delay. The voltage error due to jitters depends on the slew rate of the signal at the sampling point                                                                                                                                                                                                                                          |
| NPR          | Noise Power Ratio           | The NPR is measured to characterize the ADC's performance in response to broad bandwidth signals. When applying a notch-filtered broadband white noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test |

**Table 16.** Definitions of Terms (Continued)

| Abbreviation | Definition                                    | Description                                                                                                                                                                                                                                                                                                                                              |
|--------------|-----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ORT          | Overvoltage Recovery Time                     | The time to recover a 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale                                                                                                                                                                                                                              |
| PSRR         | Power Supply Rejection Ratio                  | The ratio of input offset variation to a change in power supply voltage                                                                                                                                                                                                                                                                                  |
| SFDR         | Spurious Free Dynamic Range                   | The ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (related to the converter -1 dB full-scale) or in dBc (related to the input signal level) |
| SINAD        | Signal to Noise and Distortion Ratio          | The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale (-1 dBFS) to the RMS sum of all other spectral components including the harmonics, except DC                                                                                                                                                                         |
| SNR          | Signal to Noise Ratio                         | The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the first 9 harmonics                                                                                                                                                                                     |
| SSBW         | Small Signal Input Bandwidth                  | The analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale -10 dB (-10 dBFS)                                                                                                           |
| TA           | Aperture delay                                | The delay between the rising edge of the differential clock inputs (CLK, CLKB) [zero crossing point] and the time at which VIN and VINB are sampled                                                                                                                                                                                                      |
| TC           | Encoding Clock period                         | TC1 = minimum clock pulse width (high)<br>TC = TC1 + TC2<br>TC2 = minimum clock pulse width (low)                                                                                                                                                                                                                                                        |
| TD1          | Time Delay from Data Transition to Data Ready | The general expression is $TD1 = TC1 + TDR - TDO$ with $TC = TC1 + TC2 = 1$ encoding clock period                                                                                                                                                                                                                                                        |
| TD2          | Time Delay from Data Ready to Data            | The general expression is $TD2 = TC2 + TDR - TDO$ with $TC = TC1 + TC2 = 1$ encoding clock period                                                                                                                                                                                                                                                        |
| TDO          | Digital Data Output Delay                     | The delay from the rising edge of the differential clock inputs (CLK, CLKB) [zero crossing point] to the next point of change in the differential output data (zero crossing) with a specified load                                                                                                                                                      |
| TDR          | Data Ready Output Delay                       | The delay from the falling edge of the differential clock inputs (CLK, CLKB) [zero crossing point] to the next point of change in the differential output data (zero crossing) with a specified load                                                                                                                                                     |
| TF           | Fall Time                                     | The time delay for the output data signals to fall from 20% to 80% of delta between the low and high levels                                                                                                                                                                                                                                              |
| THD          | Total Harmonic Distortion                     | The ratio expressed in dB of the RMS sum of the first 9 harmonic components to the RMS input signal amplitude, set at 1 dB below full-scale. It may be reported in dB (related to the converter -1 dB full-scale) or in dBc (related to the input signal level)                                                                                          |
| TPD          | Pipeline Delay                                | The number of clock cycles between the sampling edge of an input data and the associated output data made available (not taking into account the TDO)                                                                                                                                                                                                    |
| TR           | Rise Time                                     | The time delay for the output data signals to rise from 20% to 80% of delta between the low and high levels                                                                                                                                                                                                                                              |

**Table 16.** Definitions of Terms (Continued)

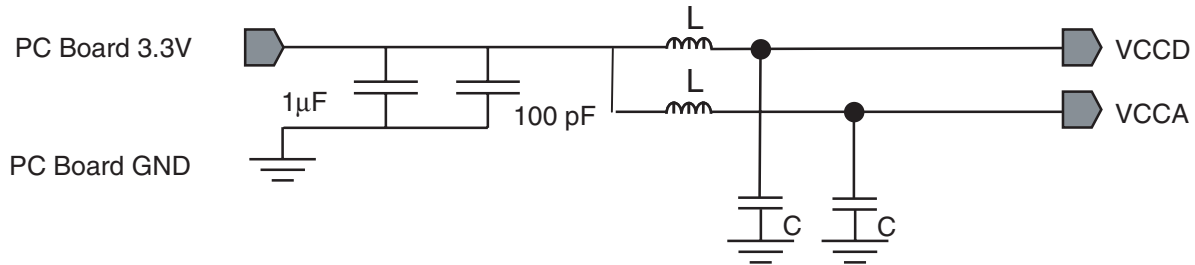
| Abbreviation | Definition                  | Description                                                                                                                                                                                |
|--------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TRDR         | Data Ready Reset Delay      | The delay between the falling edge of the Data Ready output asynchronous reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR)                 |
| TS           | Settling Time               | The time delay to rise from 10% to 90% of the converter output when a full-scale step function is applied to the differential analog input                                                 |
| VSWR         | Voltage Standing Wave Ratio | The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example, a VSWR of 1.2 corresponds to a 20 dB return loss (99% power transmitted and 1% reflected) |

## Using the AT84AD001B Dual 8-bit 1 Gsps ADC

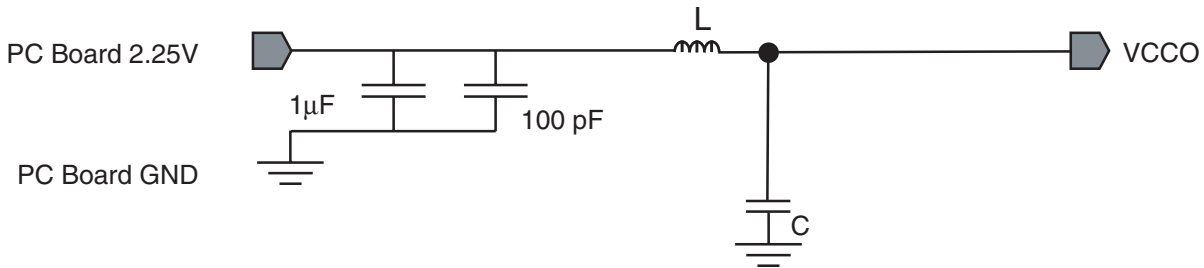
### Decoupling, Bypassing and Grounding of Power Supplies

The following figures show the recommended bypassing, decoupling and grounding schemes for the dual 8-bit 1 Gsps ADC power supplies.

**Figure 53.**  $V_{CCD}$  and  $V_{CCA}$  Bypassing and Grounding Scheme

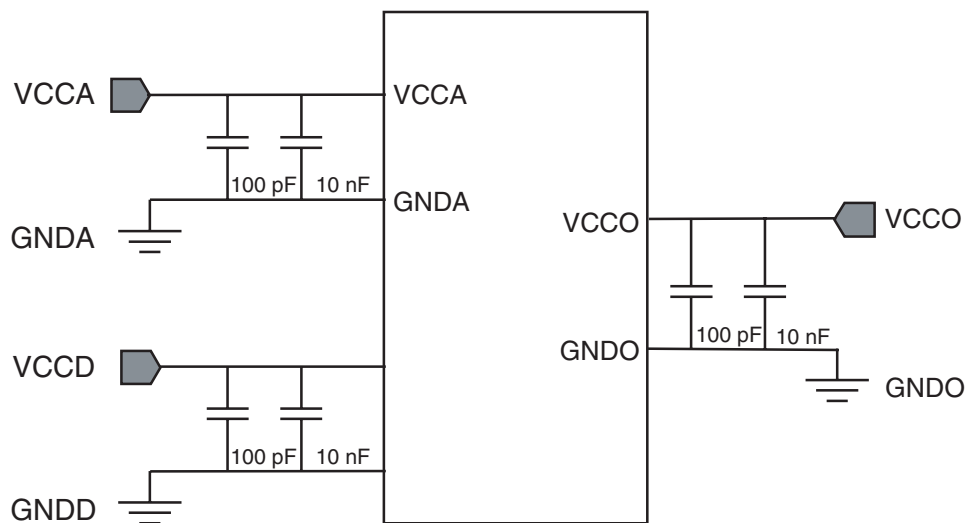


**Figure 54.**  $V_{CCO}$  Bypassing and Grounding Scheme



Note: L and C values must be chosen in accordance with the operation frequency of the application.

**Figure 55.** Power Supplies Decoupling Scheme



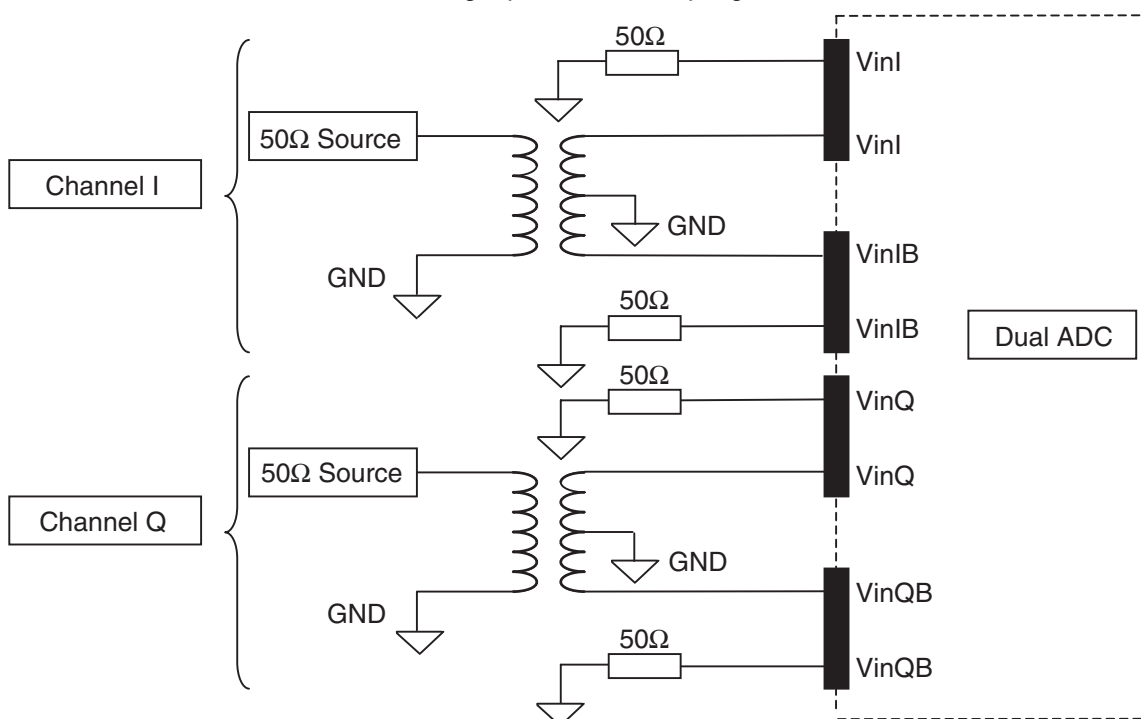
Note: The bypassing capacitors (1 µF and 100 pF) should be placed as close as possible to the board connectors, whereas the decoupling capacitors (100 pF and 10 nF) should be placed as close as possible to the device.

## Analog Input Implementation

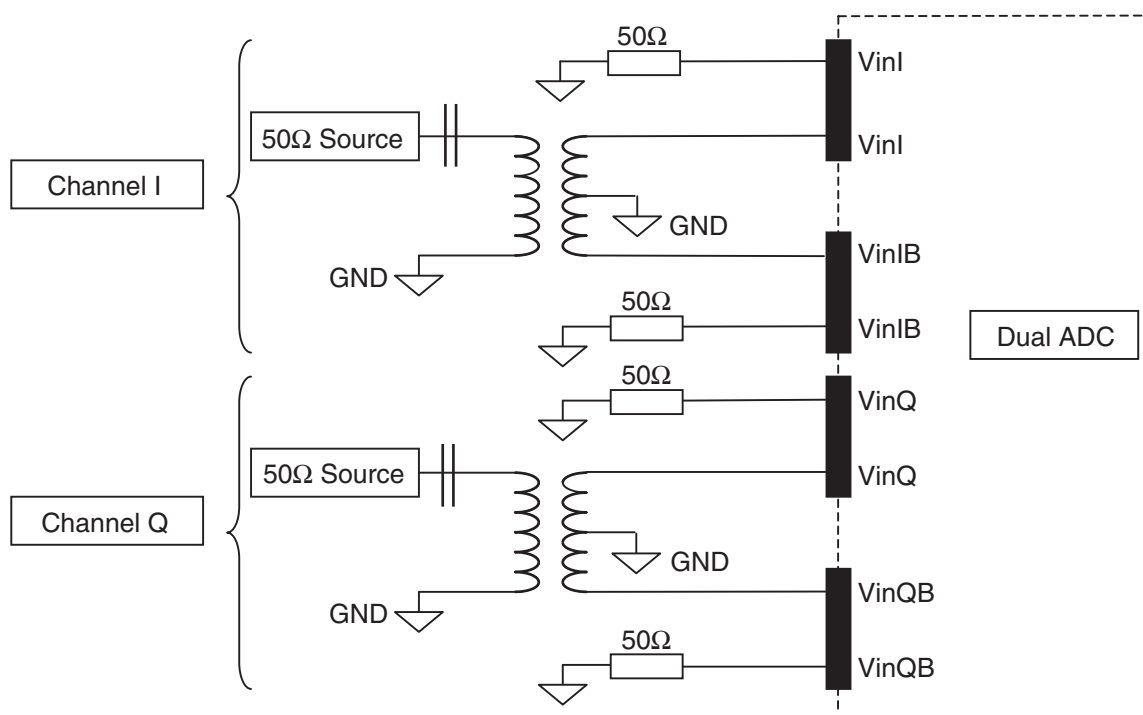
The analog inputs of the dual ADC have been designed with a double pad implementation as illustrated in Figure 56. The reverse pad for each input should be tied to ground via a  $50\Omega$  resistor.

The analog inputs must be used in differential mode only.

**Figure 56.** Termination Method for the ADC Analog Inputs in DC Coupling Mode



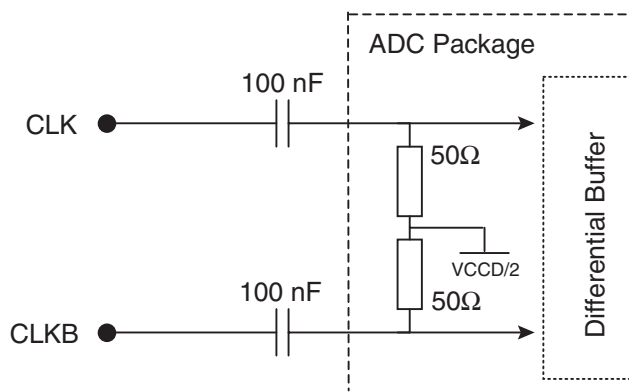
**Figure 57.** Termination Method for the ADC Analog Inputs in AC Coupling Mode



## Clock Implementation

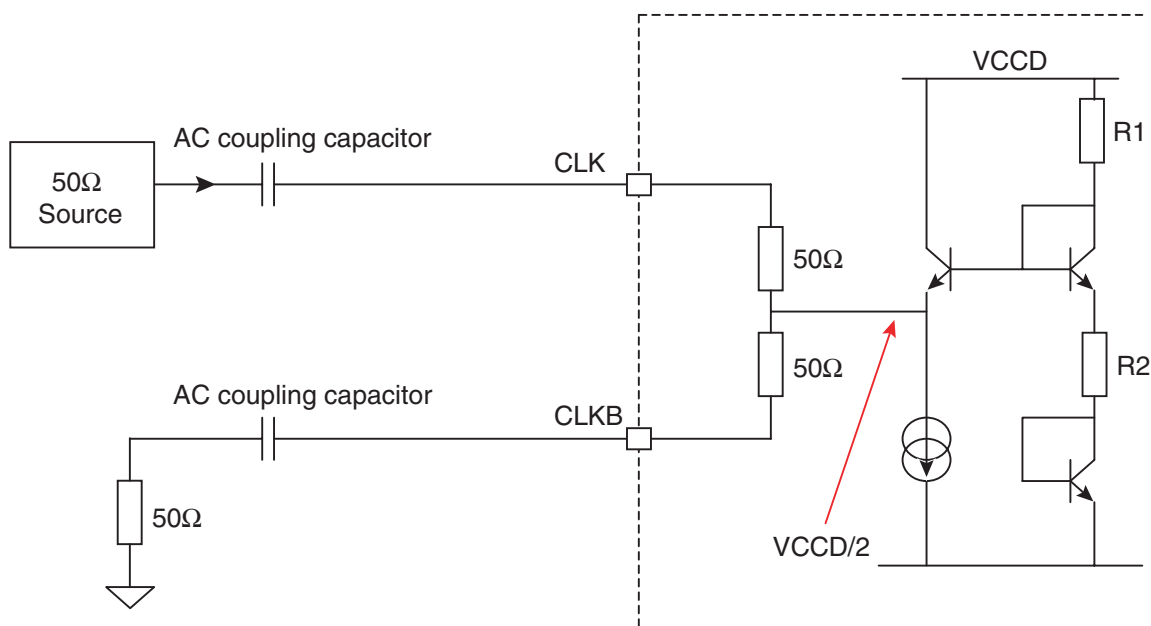
The ADC features two different clocks (I or Q) that must be implemented as shown in Figure 58. Each path must be AC coupled with a 100 nF capacitor.

**Figure 58.** Differential Termination Method for Clock I or Clock Q



Note: When only clock I is used, it is not necessary to add the capacitors on the CLKQ and CLKQN signal paths; they may be left floating.

**Figure 59.** Single-ended Termination Method for Clock I or Clock Q



### Output Termination in 1:1 Ratio

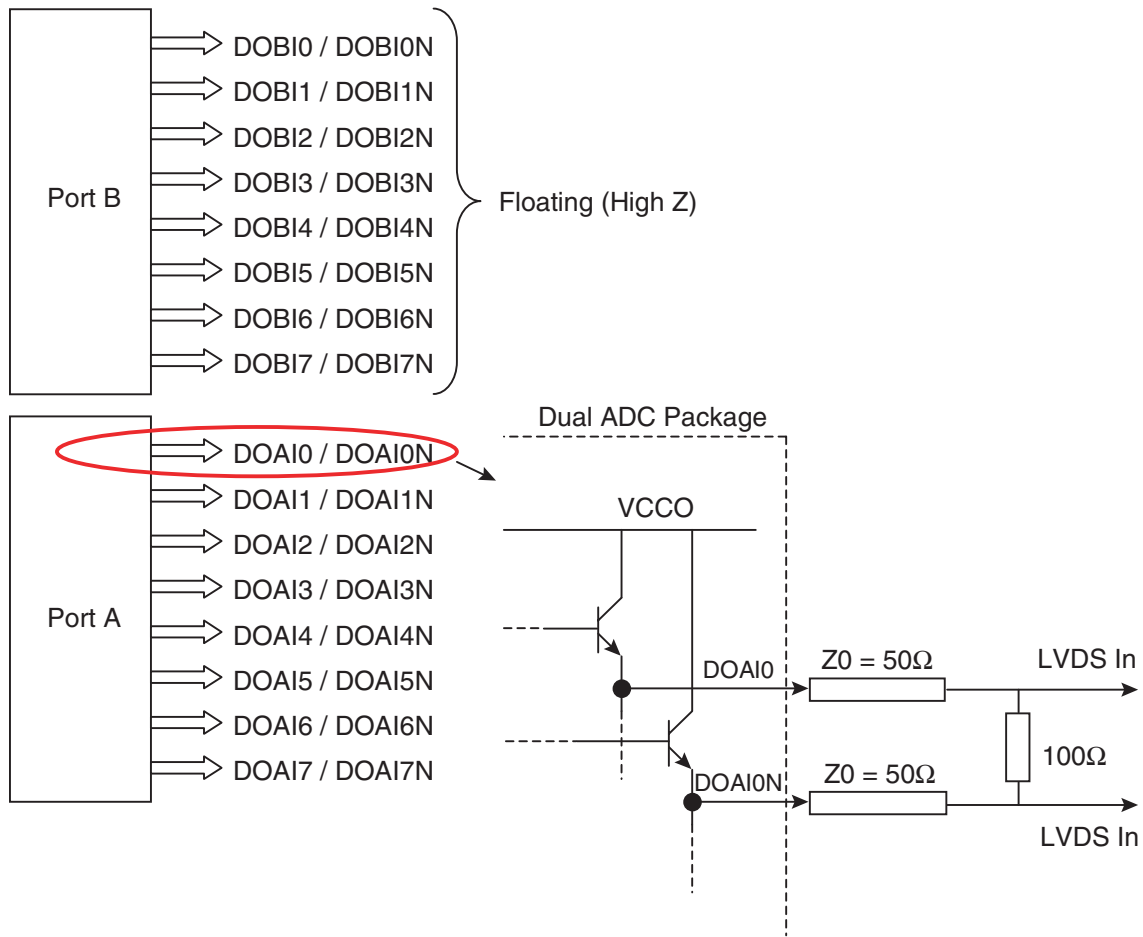
When using the integrated DMUX in 1:1 ratio, the valid port is port A. Port B remains unused.

Port A functions in LVDS mode and the corresponding outputs (DOAI or DOAQ) have to be  $100\Omega$  differentially terminated as shown in Figure 60 on page 54.

The pins corresponding to Port B (DOBI or DOBQ pins) must be left floating (in high impedance state).

Figure 60 shows the example of a 1:1 ratio of the integrated DMUX for channel I (the same applies to channel Q).

**Figure 60.** Example of Termination for Channel I Used in DMUX 1:1 Ratio (Port B Unused)

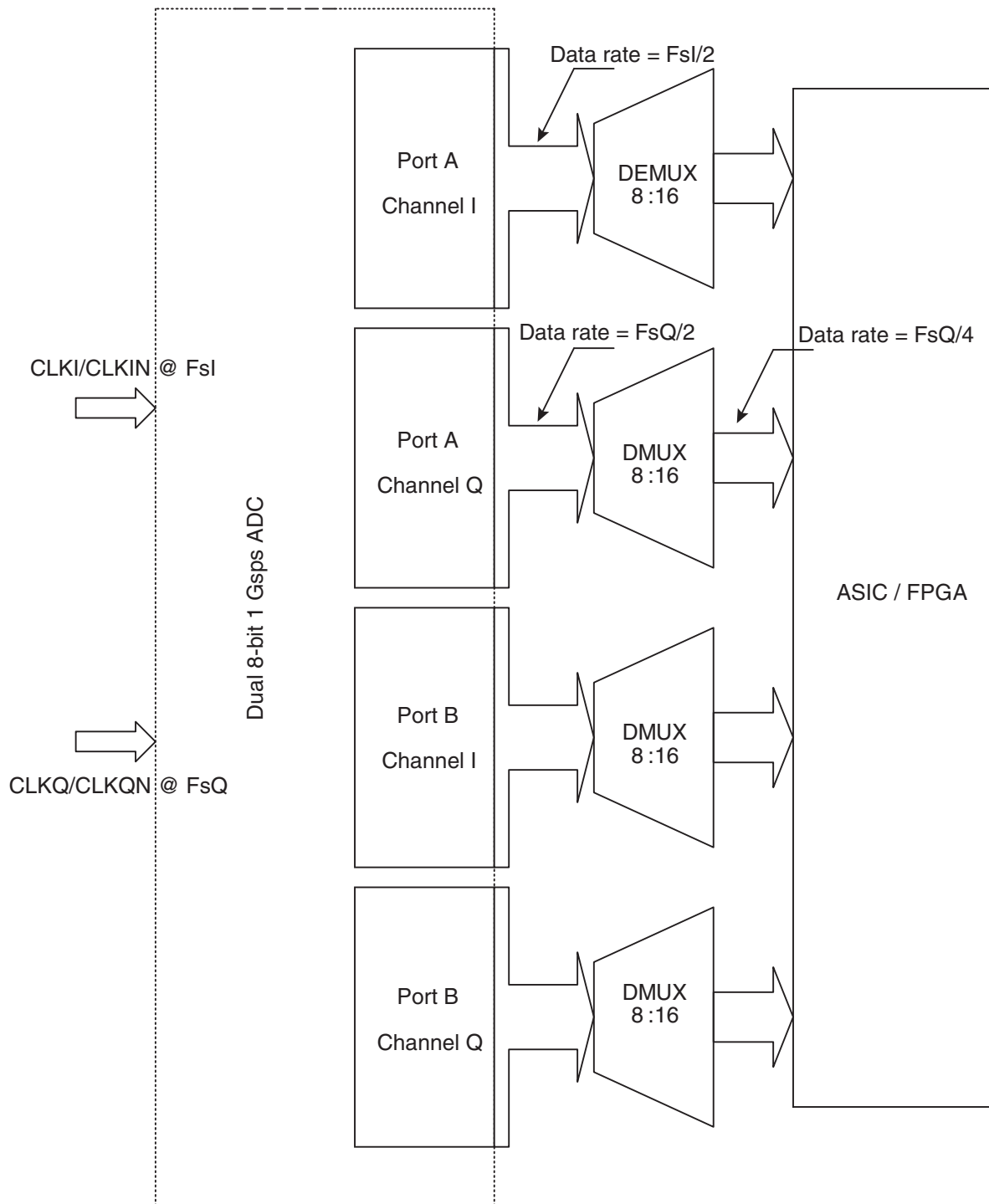


**Note:** If the outputs are to be used in single-ended mode, it is recommended that the true and false signals be terminated with a 50Ω resistor.

### Using the Dual ADC With and ASIC/FPGA Load

Figure 61 on page 55 illustrates the configuration of the dual ADC (1:2 DMUX mode, independent I and Q clocks) driving an LVDS system (ASIC/FPGA) with potential additional DMUXes used to halve the speed of the dual ADC outputs.

**Figure 61.** Dual ADC and ASIC/FPGA Load Block Diagram



Note: The demultiplexers may be internal to the ASIC/FPGA system.



*Thermal Resistance from  
Junction to Ambient*

The thermal resistance from the junction to ambient is 25.2° C/W typical.

Note: In order to keep the ambient temperature of the die within the specified limits of the device grade (that is  $T_A$  max = 70°C in commercial grade and 85°C in industrial grade) and the die junction temperature below the maximum allowed junction temperature of 105°C, it is necessary to operate the dual ADC in air flow conditions (1m/s recommended).

In still air conditions, the junction temperature is indeed greater than the maximum allowed  $T_J$ .

- $T_J = 25.2^{\circ}\text{C/W} \times 1.4\text{W} + T_A = 35.28 + 70 = 105.28^{\circ}\text{C}$  for commercial grade devices
- $T_J = 25.2^{\circ}\text{C/W} \times 1.4\text{W} + T_A = 35.28 + 85 = 125.28^{\circ}\text{C}$  for industrial grade devices

*Thermal Resistance from  
Junction to Board*

The thermal resistance from the junction to the board is 13° C/W typical.

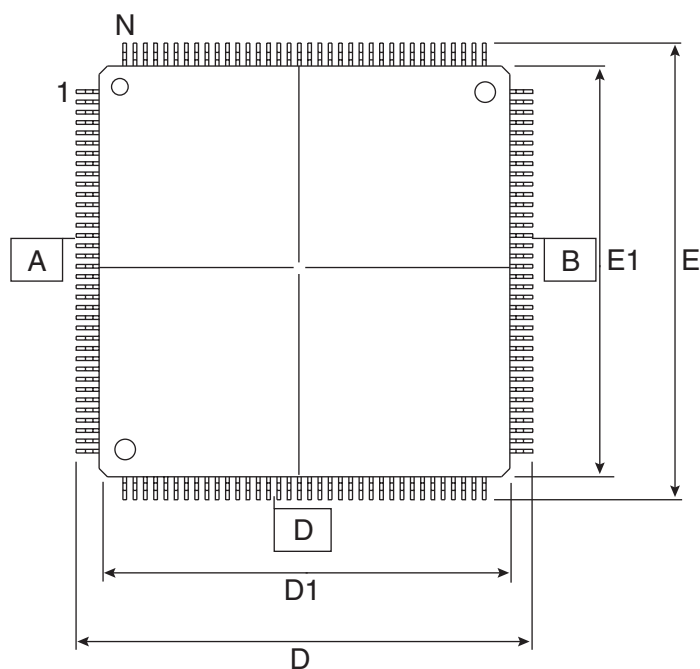


## Ordering Information

| Part Number    | Package  | Temperature Range                                           | Screening | Comments                                                          |
|----------------|----------|-------------------------------------------------------------|-----------|-------------------------------------------------------------------|
| AT84XAD001BTD  | LQFP 144 | Ambient                                                     | Prototype | Prototype version<br>Please contact your local Atmel sales office |
| AT84AD001BCTD  | LQFP 144 | C grade<br>$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$   | Standard  |                                                                   |
| AT84AD001BITD  | LQFP 144 | I grade<br>$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ | Standard  |                                                                   |
| AT84AD001TD-EB | LQFP 144 | Ambient                                                     | Prototype | Evaluation Kit                                                    |

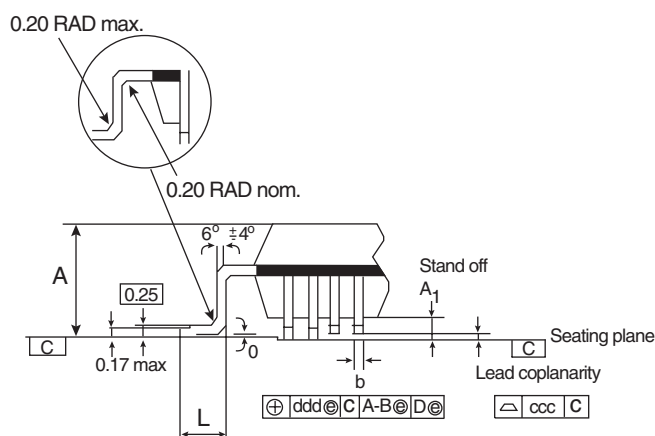
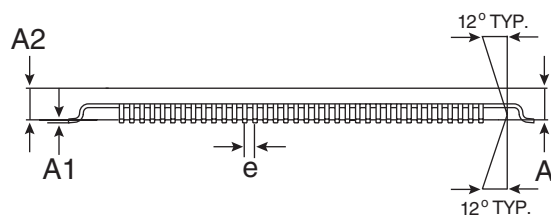
## Packaging Information

**Figure 63.** Type of Package



| Body +2.00 mm footprint |             |       |                     |
|-------------------------|-------------|-------|---------------------|
| Dims.                   | Tols.       | Leads | 144L                |
| A                       | max.        |       | 1.60                |
| A1                      |             |       | 0.05 min./0.15 max. |
| A2                      | +/- 0.05    |       | 1.40                |
| D                       | +/-0.20     |       | 22.00               |
| D1                      | +/-0.10     |       | 20.00               |
| E                       | +/-0.20     |       | 22.00               |
| E1                      | +/-0.10     |       | 20.00               |
| L                       | +0.15/-0.10 |       | 0.60                |
| e                       | basic       |       | 0.50                |
| b                       | +/-0.05     |       | 0.22                |
| ddd                     |             |       | 0.08                |
| ccc                     | max.        |       | 0.08                |
| o                       |             |       | 0°-5°               |

- Notes:
1. All dimensions are in millimeters
  2. Dimensions shown are nominal with tolerances as indicated
  3. L/F: etfec 64T copper or equivalent
  4. Foot length: "L" is measured at gauge plane at 0.25 mm above the seating plane



Note: Thermally enhanced package: LQFP 144, 20 x 20 x 1.4 mm.



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