



N-Channel 2.5-V (G-S) MOSFET, ESD Protected

CHARACTERISTICS

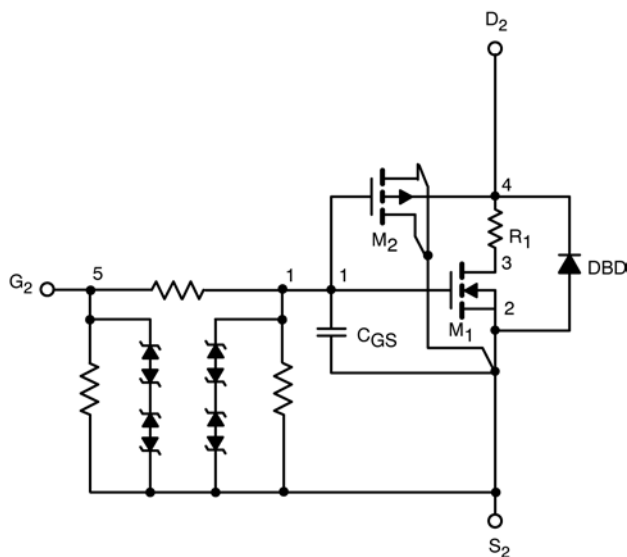
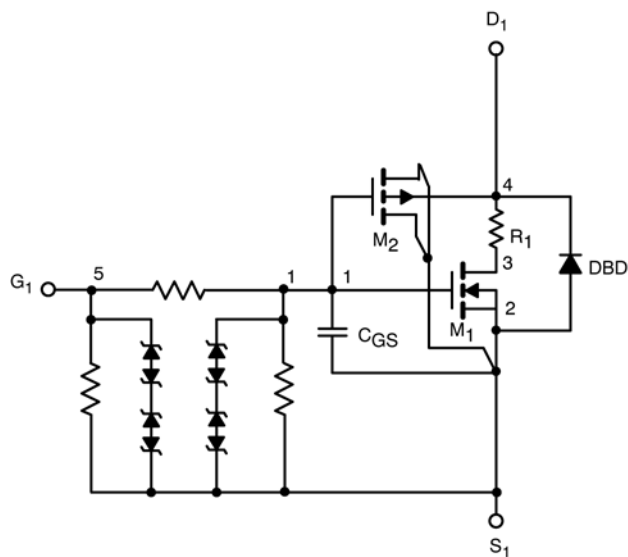
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si6966EDQ

Vishay Siliconix



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.923	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	120	A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.2 A	0.02	Ω
		V _{GS} = 2.5 V, I _D = 4.5 A	0.027	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5.2 A	19.5	S
Schottky Diode Forward Voltage ^a	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	0.65	V
		I _S = 1.25 A, V _{GS} = 0 V, T _J = 125°C	0.57	
Dynamic ^b				
Total Gate Charge ^b	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 5.2 A	13.4	nC
Gate-Source Charge ^b	Q _{gs}		2.1	
Gate-Drain Charge ^b	Q _{gd}		5.7	
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω	0.35	ns
Rise Time ^b	t _r		76	
Turn-Off Delay Time ^b	t _{d(off)}		131	
Fall Time ^b	t _f		290	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.25 A, di/dt = 100 A/μs	210	

Notes

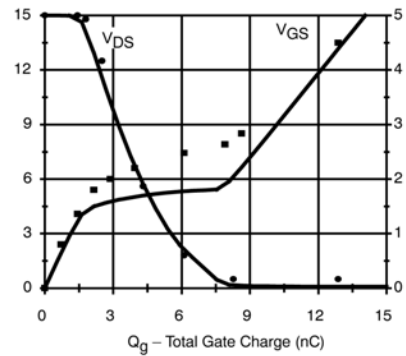
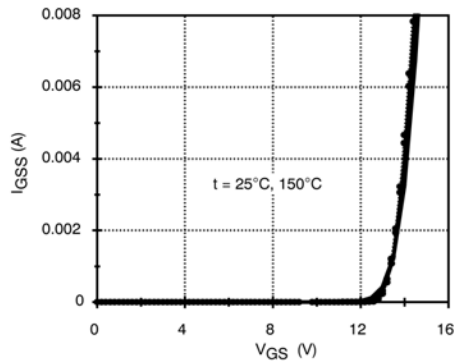
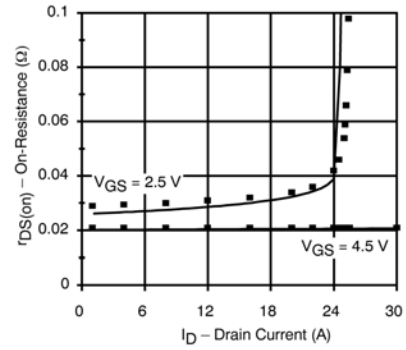
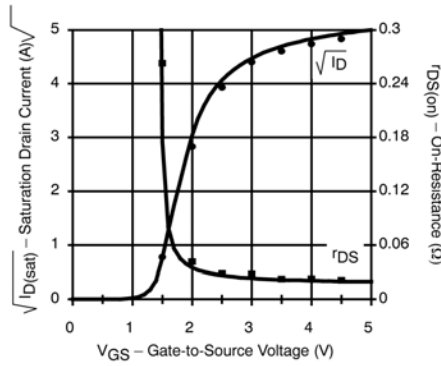
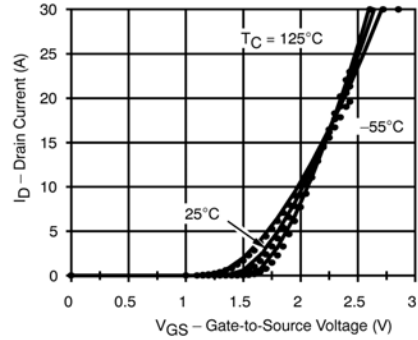
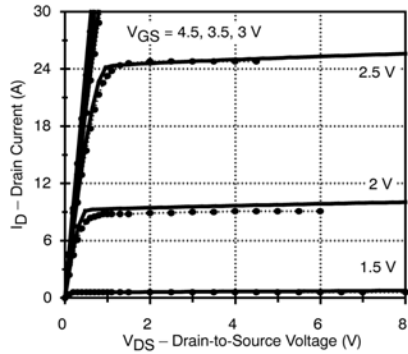
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.