FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27240-1E

ASSP for Power Supply Applications (Secondary Battery)

DC/DC Converter IC for Charging Li-ion Battery

MB39A113

■ DESCRIPTION

MB39A113 is a DC/DC converter IC of pulse width modulation (PWM) type for charging, capable of independently controlling the output voltage and output current. MB39A113 is suitable for down conversion.

MB39A113 can dynamically control the charge current of the secondary battery, to keep the power constant by detecting a voltage drop in an AC adapter (dynamically-controlled charging) .

MB39A113 can easily set the charge current value, making it ideal for use as a built-in charging device in products such as notebook PC.

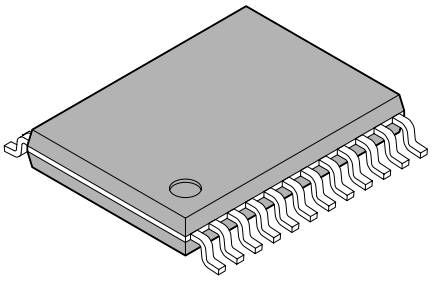
■ FEATURES

- Built-in dual constant-current control circuits
- Analog control of charge current is possible. (+INE1 and +INE2 terminals)
- Built-in AC adapter detection function (fixing the output in the off state when the VCC voltage is lower than the battery voltage + 0.2 V)
- Possible to prevent mis-detecting of fully-charged state by constant-voltage control state detection function (CVM terminal)
- Built-in overvoltage detection function of charge-voltage (OVP terminal)

(Continued)

■ PACKAGE

24-pin plastic SSOP



(FPT-24P-M03)

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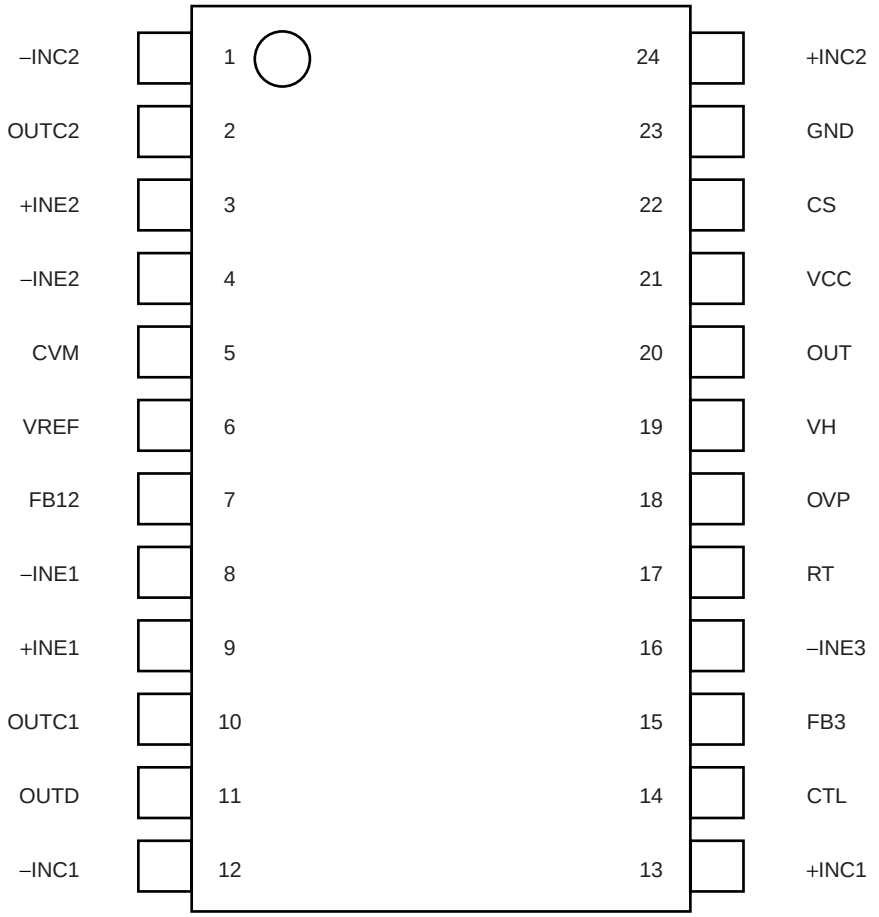
- Wide range of operating power-supply voltage : 8 V to 25 V
- Output voltage setting accuracy : ± 0.74% (Ta = –10 °C to + 85 °C)
- Built-in high accuracy current detection amplifier : ± 5% (At the input voltage difference of 100 mV) ,
  ± 15% (At the input voltage difference of 20 mV)
- Output voltage setting resistor is open to enable prevention of invalidity current at IC standby. (I_{CC} = 0 µA Typ)
- Oscillation frequency range : 100 kHz to 500 kHz
- Built-in current detection amplifier with wide in-phase input voltage range : 0 V to V_{CC}
- Built-in soft-start function independent of loads
- Built-in standby current function : 0 µA (Typ)
- Built-in totem-pole output stage supporting P-channel MOS FETs devices

■ PIN ASSIGNMENT

(TOP VIEW)

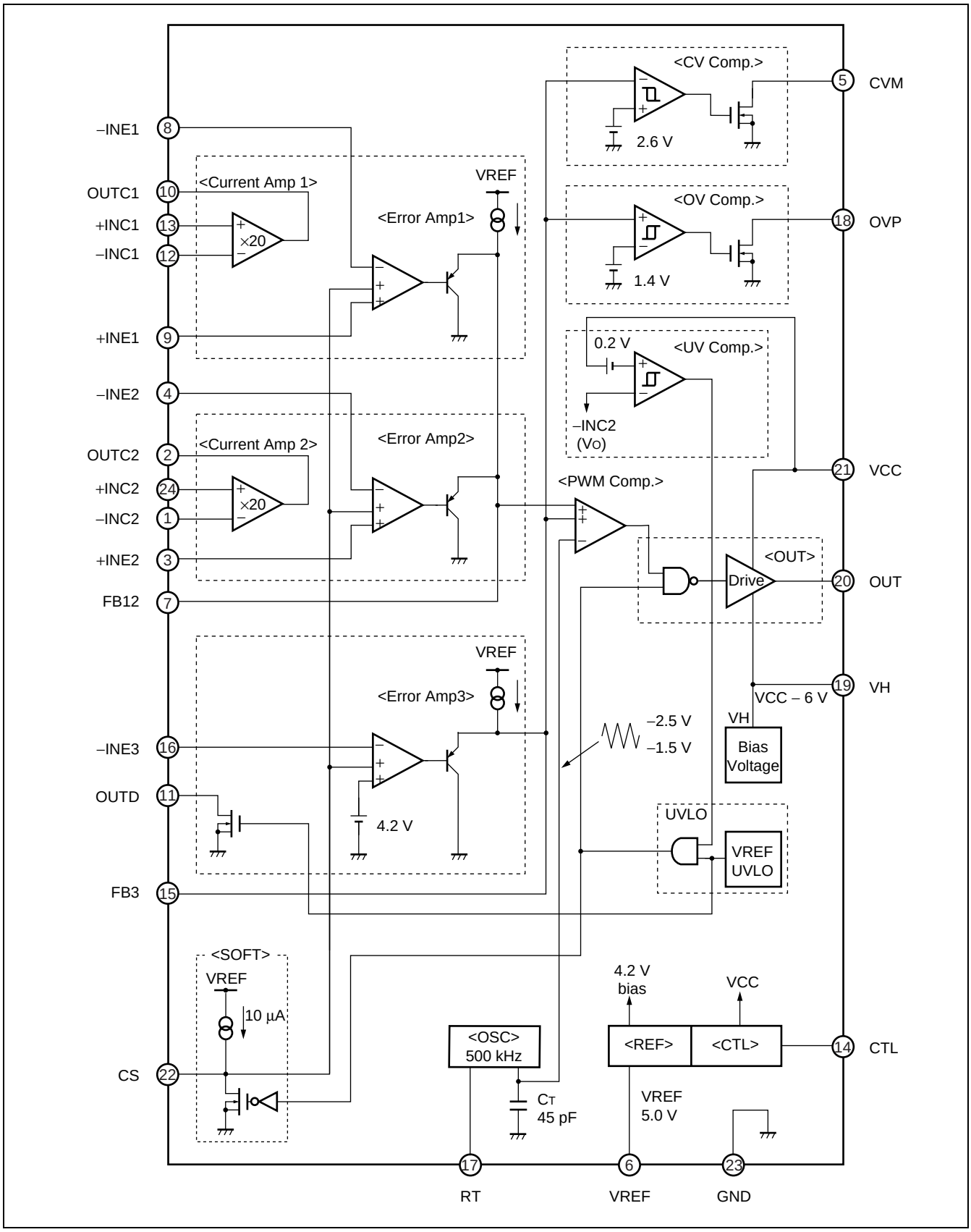


(FPT-24P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	–INC2	I	Current detection amplifier (Current Amp2) inverted input terminal
2	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
3	+ INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
4	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
5	CVM	O	Open drain type output terminal of constant-voltage control state detection comparator (CV Comp.)
6	VREF	O	Reference voltage output terminal
7	FB12	O	Error amplifier (Error Amp1, Error Amp2) output terminal
8	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
9	+ INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
10	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
11	OUTD	O	With IC in standby mode, this terminal is set to Hi-Z to prevent loss of current through output voltage setting resistance. CTL terminal : Output “L” level at “H” level
12	–INC1	I	Current detection amplifier (Current Amp1) inverted input terminal
13	+ INC1	I	Current detection amplifier (Current Amp1) non-inverted input terminal
14	CTL	I	Power supply control terminal Setting the CTL terminal at “L” level places the IC in the standby mode.
15	FB3	O	Error amplifier (Error Amp3) output terminal
16	–INE3	I	Error amplifier (Error Amp3) inverted input terminal
17	RT	—	Triangular wave oscillation frequency setting resistor connection terminal
18	OVP	O	Open drain type output terminal of overvoltage detection comparator (OVComp.)
19	VH	O	Power supply terminal for FET drive circuit. (VH = VCC–6 V)
20	OUT	O	External FET gate drive terminal.
21	VCC	—	Power supply terminal for reference power supply control circuit and output circuit
22	CS	—	Soft-start capacitor connection terminal
23	GND	—	Ground terminal
24	+ INC2	I	Current detection amplifier (Current Amp2) non-inverted input terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC terminal	—	28	V
Output current	I_{OUT}	—	—	60	mA
Peak output current	I_{OUT}	Duty ≤ 5% (t = 1/fosc × Duty)	—	700	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	740*	mW
Storage temperature	T_{STG}	—	–55	+125	°C

* : The package are mounted on the dual-sided epoxy board (10 cm × 10 cm) .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Sym-bol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC terminal	8	—	25	V
Reference voltage output current	I_{REF}	—	–1	—	0	mA
VH terminal output current	I_{VH}	—	0	—	30	mA
Input voltage	V_{INE}	–INE1 to –INE3, + INE1, + INE2 terminal	0	—	5	V
	V_{INC}	+ INC1, + INC2, –INC1, –INC2 terminal	0	—	V_{CC}	V
CTL terminal input voltage	V_{CTL}	—	0	—	25	V
Output current	I_{OUT}	—	–45	—	+45	mA
Peak output current	I_{OUT}	Duty ≤ 5% (t = 1/fosc × Duty)	–600	—	+600	mA
CVM terminal output voltage	V_{CVM}	—	0	—	25	V
CVM terminal output current	I_{CVM}	—	0	—	1	mA
OVP terminal output voltage	V_{OVP}	—	0	—	25	V
OVP terminal output current	I_{OVP}	—	0	—	1	mA
OUTD terminal output voltage	V_{OUTD}	—	0	—	17	V
OUTD terminal output current	I_{OUTD}	—	0	—	2	mA
Oscillation frequency	fosc	—	100	300	500	kHz
Timing resistor	R_T	—	27	47	130	kΩ
Soft-start capacitor	C_S	—	—	0.022	1.0	µF
VH terminal capacitor	C_{VH}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Output voltage	V_{REF1}	6	Ta = +25 °C	4.975	5.000	5.025	V
		V_{REF2}	6	Ta = –10 °C to +85 °C	4.963	5.000	5.037	V
	Input stability	Line	6	VCC = 8 V to 25 V	—	3	10	mV
	Load stability	Load	6	VREF = 0 mA to –1 mA	—	1	10	mV
	Short-circuit output current	Ios	6	VREF = 1 V	–50	–25	–12	mA
Under-Voltage (VCC) Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	6	VREF = ↗	2.6	2.8	3.0	V
		V_{THL}	6	VREF = ↘	2.4	2.6	2.8	V
	Hysteresis width	V_H	6	—	—	0.2*	—	V
Soft-start Block [SOFT]	Charge current	I_{CS}	22	—	–14	–10	–6	µA
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	fosc	20	RT = 47 kΩ	270	300	330	kHz
	Frequency temperature stability	Δf/fdt	20	Ta = –30 °C to + 85 °C	—	1*	—	%
Error Amplifier Block [Error Amp1, Error Amp2]	Input offset voltage	V_{IO}	3, 4, 8, 9	FB12 = 2 V	—	1	5	mV
	Input bias current	I_B	3, 4, 8, 9	—	–100	–30	—	nA
	Voltage gain	A_V	7	DC	—	100*	—	dB
	Frequency bandwidth	BW	7	AV = 0 dB	—	1.3*	—	MHz
	Output voltage	V_{FBH}	7	—	4.8	5.0	—	V
		V_{FBL}	7	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	7	FB12 = 2 V	—	–120	–60	µA
	Output sink current	I_{SINK}	7	FB12 = 2 V	2.0	4.0	—	mA

* : Standard design value

(Continued)

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error Amplifier Block [Error Amp3]	Input current	I_{INE}	16	–INE3 = 0 V	–100	–30	—	nA
	Voltage gain	A_V	15	DC	—	100*	—	dB
	Frequency bandwidth	BW	15	AV = 0 dB	—	1.3*	—	MHz
	Output voltage	V_{FBH}	15	—	4.8	5.0	—	V
		V_{FBL}	15	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	15	FB3 = 2 V	—	–120	–60	µA
	Output sink current	I_{SINK}	15	FB3 = 2 V	2.0	4.0	—	mA
	Threshold voltage	V_{TH1}	16	FB3 = 2 V, Ta = + 25 °C	4.179	4.200	4.221	V
		V_{TH2}	16	FB3 = 2 V, Ta = –10 °C to + 85 °C	4.169	4.200	4.231	V
	OUTD terminal output leak current	I_{LEAK}	11	OUTD = 17 V	—	0	1	µA
	OUTD terminal output ON resistor	R_{ON}	11	OUTD = 1 mA	—	35	50	Ω
Current Detection Amplifier Block [Current Amp1, Current Amp2]	Input offset voltage	V_{IO}	1, 12, 13, 24	+ INC1 = + INC2 = –INC1 = –INC2 = 3 V to VCC	–3	—	+3	mV
	Input current	I_{+INCH}	13, 24	+ INC1 = + INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	20	30	µA
		$I_{–INCH}$	1, 12	+ INC1 = + INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	0.1	0.2	µA
		I_{+INCL}	13, 24	+ INC1 = + INC2 = 0 V, ΔV_{IN} = –100 mV	–180	–120	—	µA
		$I_{–INCL}$	1, 12	+ INC1 = + INC2 = 0 V, ΔV_{IN} = –100 mV	–195	–130	—	µA
	Current detection voltage	V_{OUTC1}	2, 10	+ INC1 = + INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	1.9	2.0	2.1	V
		V_{OUTC2}	2, 10	+ INC1 = + INC2 = 3 V to VCC, ΔV_{IN} = –20 mV	0.34	0.40	0.46	V
		V_{OUTC3}	2, 10	+ INC1 = + INC2 = 0 V, ΔV_{IN} = –100 mV	1.8	2.0	2.2	V
		V_{OUTC4}	2, 10	+ INC1 = + INC2 = 0 V, ΔV_{IN} = –20 mV	0.2	0.4	0.6	V
	In-phase input voltage range	V_{CM}	1, 12, 13, 24	—	0	—	V_{CC}	V
	Voltage gain	A_V	2, 10	+ INC1 = + INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	19	20	21	V/V
	Frequency bandwidth	BW	2, 10	AV = 0 dB	—	2*	—	MHz
	Output voltage	V_{OUTCH}	2, 10	—	4.7	4.9	—	V
		V_{OUTCL}	2, 10	—	—	20	200	mV
	Output source current	I_{SOURCE}	2, 10	OUTC1 = OUTC2 = 2 V	—	–2	–1	mA
	Output sink current	I_{SINK}	2, 10	OUTC1 = OUTC2 = 2 V	150	300	—	µA

* : Standard design value

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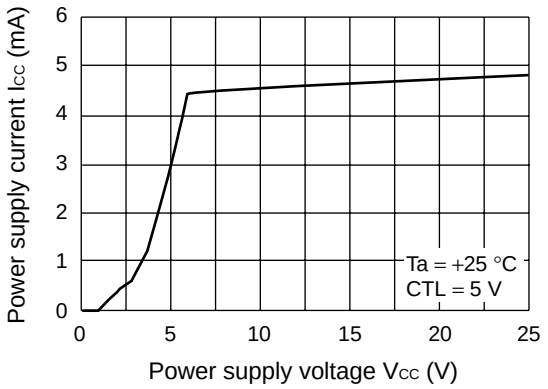
(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
PWM Comparator Block [PWM Comp.]	Threshold voltage	V_{TL}	7, 15	Duty cycle = 0%	1.4	1.5	—	V
		V_{TH}	7, 15	Duty cycle = 100%	—	2.5	2.6	V
Output Block [OUT]	Output source current	I_{SOURCE}	20	OUT = 13 V, Duty ≤ 5% (t = 1/fosc × Duty)	—	–400*	—	mA
	Output sink current	I_{SINK}	20	OUT = 19 V, Duty ≤ 5% (t = 1/fosc × Duty)	—	400*	—	mA
	Output ON resistor	R_{OH}	20	OUT = –45 mA	—	6.5	9.8	Ω
		R_{OL}	20	OUT = 45 mA	—	5.0	7.5	Ω
	Rise time	tr1	20	OUT = 3300 pF	—	50*	—	ns
	Fall time	tf1	20	OUT = 3300 pF	—	50*	—	ns
AC Adaptor Detection Block [UV Comp.]	Threshold voltage	V_{TLH}	21	VCC = ↗, –INC2 = 16.8 V	17.2	17.4	17.6	V
		V_{THL}	21	VCC = ↘, –INC2 = 16.8 V	16.8	17.0	17.2	V
	Hysteresis width	V_H	21	—	—	0.4*	—	V
Constant-voltage Control State Detection Block [CV Comp.]	Threshold voltage	V_{TLH}	5	FB3 = ↗	2.6	2.7	2.8	V
		V_{THL}	5	FB3 = ↘	2.5	2.6	2.7	V
	Hysteresis width	V_H	5	—	—	0.1*	—	V
	CVM terminal output leakage current	I_{LEAK}	5	CVM = 25 V	—	0	1	µA
	CVM terminal output ON resistor	R_{ON}	5	CVM = 1 mA	—	200	400	Ω
Overvoltage Detection Block [OV Comp.]	Threshold voltage	V_{TLH}	18	FB3 = ↗	1.3	1.4	1.5	V
		V_{THL}	18	FB3 = ↘	1.2	1.3	1.4	V
	Hysteresis width	V_H	18	—	—	0.1*	—	V
	OVP terminal output leak current	I_{LEAK}	18	OVP = 25 V	—	0	1	µA
	OVP terminal output ON resistor	R_{ON}	18	OVP = 1 mA	—	200	400	Ω
Control Block [CTL]	CTL input voltage	V_{ON}	14	IC operation mode	2	—	25	V
		V_{OFF}	14	IC standby mode	0	—	0.8	V
	Input current	I_{CTLH}	14	CTL = 5 V	—	100	150	µA
		I_{CTLL}	14	CTL = 0 V	—	0	1	µA
Bias Voltage Block [VH]	Output voltage	V_H	19	VCC = 8 V to 25 V, VH = 0 mA to 30 mA	V_{CC} –6.5	V_{CC} –6.0	V_{CC} –5.5	V
General	Standby current	I_{CCS}	21	CTL = 0 V	—	0	10	µA
	Power supply current	I_{CC}	21	CTL = 5 V	—	5	7.5	mA

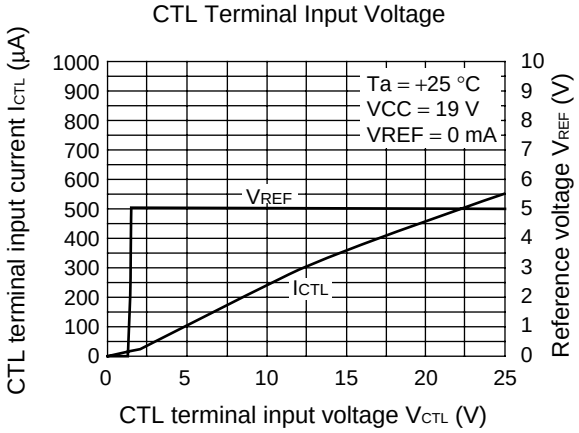
* : Standard design value

■ TYPICAL CHARACTERISTICS

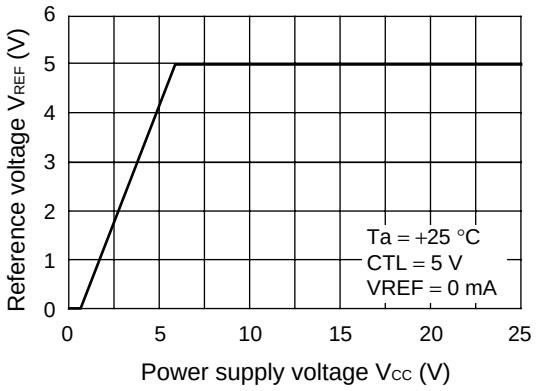
Power Supply Current vs. Power Supply Voltage



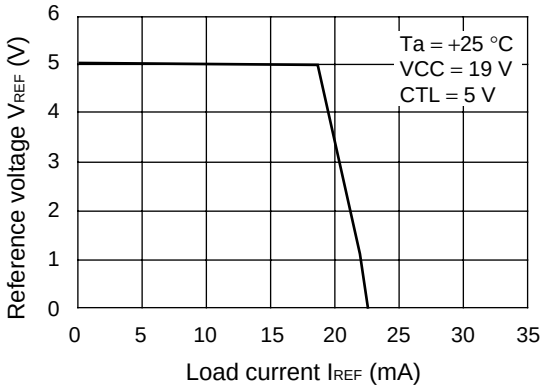
CTL Terminal Input Current, Reference Voltage vs. CTL Terminal Input Voltage



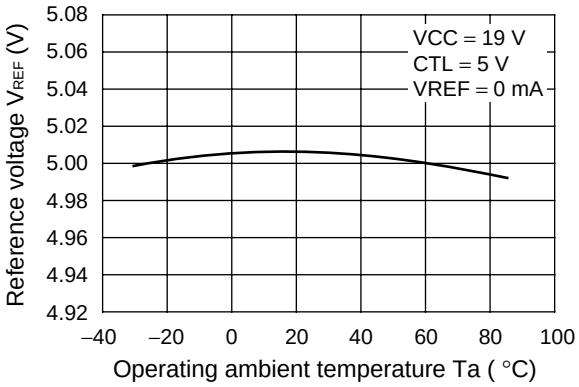
Reference Voltage vs. Power Supply Voltage



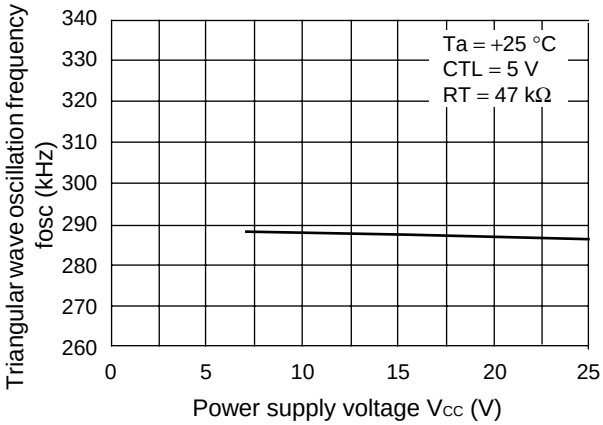
Reference Voltage vs. Load Current



Reference Voltage vs. Operating Ambient Temperature



Triangular Wave Oscillation Frequency vs. Power Supply Voltage



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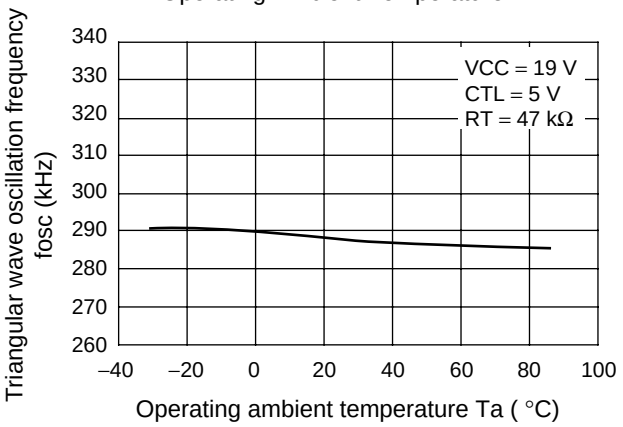
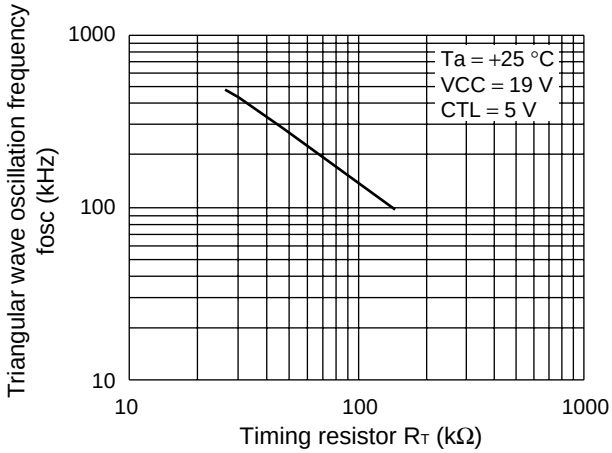
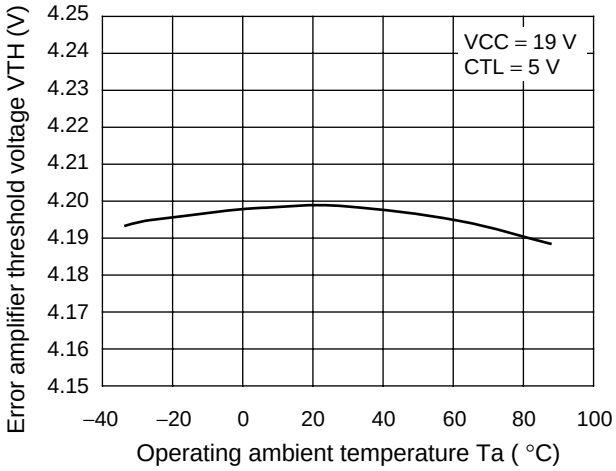
Triangular Wave Oscillation Frequency vs.
Operating Ambient Temperature



Triangular Wave Oscillation Frequency vs.
Timing Resistor



Error Amplifier Threshold Voltage vs.
Operating Ambient Temperature



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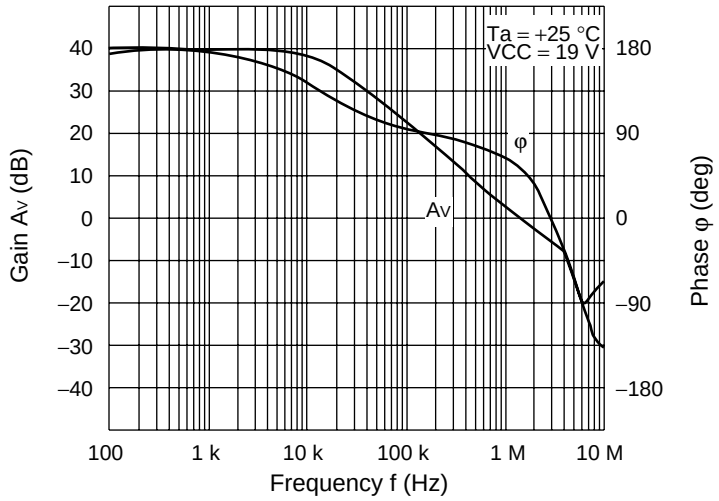
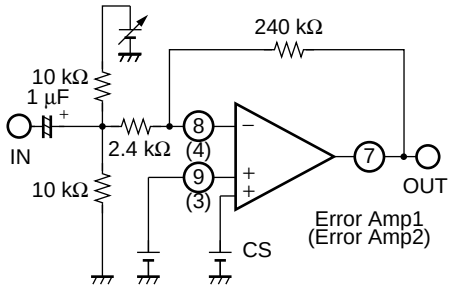
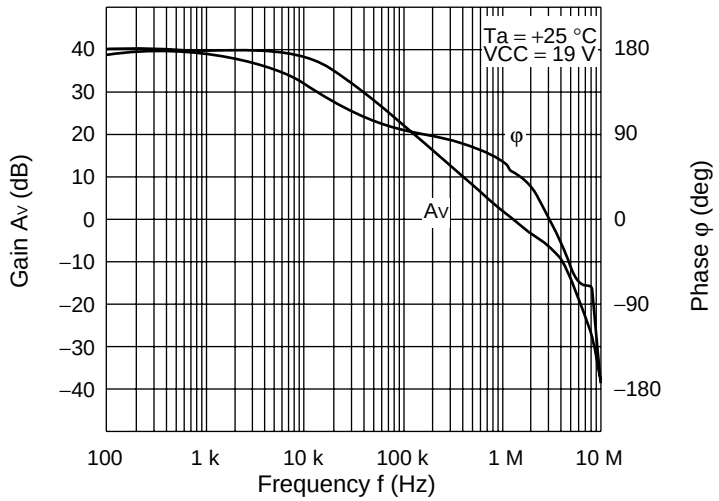
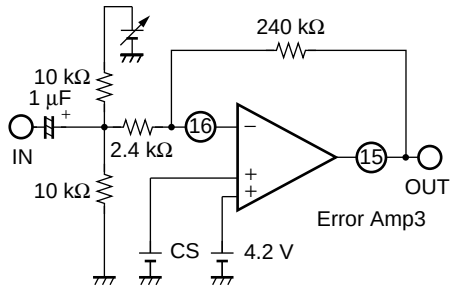
Error Amplifier, Gain and Phase vs. Frequency



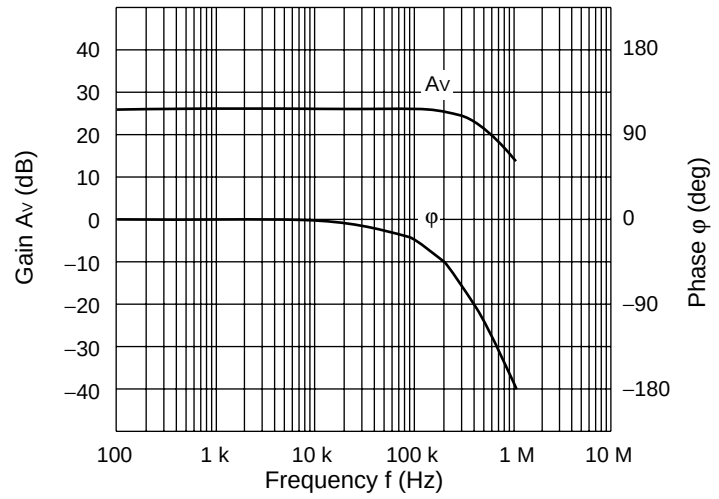


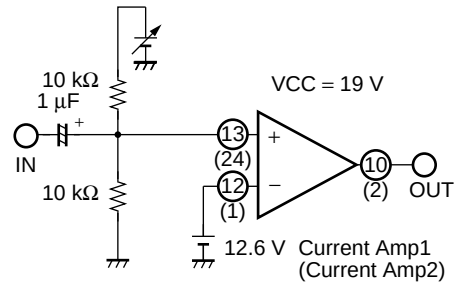
Error Amplifier, Gain and Phase vs. Frequency





Current Detection Amplifier, Gain and Phase vs. Frequency





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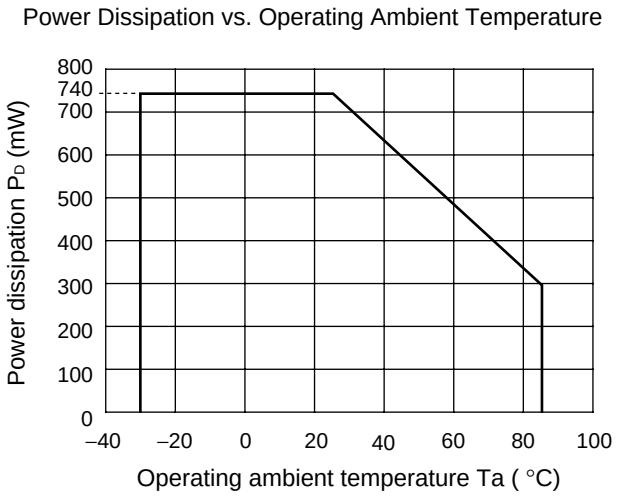

Power Dissipation vs. Operating Ambient Temperature
Power dissipation P_D (mW)
800
740
700
600
500
400
300
200
100
0
–40
–20
0
20
40
60
80
100
Operating ambient temperature Ta (°C)

■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Block

(1) Reference voltage block (REF)

The reference voltage circuit generates a temperature-compensated reference voltage (5.0 V Typ) using the voltage supplied from the VCC terminal (pin 21) . The voltage is used as the reference voltage for the IC's internal circuit.

The reference voltage can be used to supply a load current of up to 1 mA to an external device through the VREF terminal (pin 6) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator block has built-in a frequency setting capacitor, and generates the triangular wave oscillation waveforms by connecting the frequency setting resistor with the RT terminal (pin 17) .

The triangular wave is input to the IC's internal PWM comparator.

(3) Error amplifier block (Error Amp1)

The error amplifier (Error Amp1) detects voltage drop of the AC adaptor and a PWM control signal is output.

By connecting a feedback resistor and capacitor between FB12 terminal (pin 7) and –INE1 terminal (pin 8) , it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 22) .

The use of error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

(4) Error amplifier block (Error Amp2)

The error amplifier detects output signal of current detection amplifier (Current Amp2) and outputs PWM control signal by comparison with +INE2 terminal (pin 3) , also controls charge current.

By connecting a feedback resistor and capacitor between FB12 terminal (pin 7) and –INE2 terminal (pin 4) , it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 22) . The use of error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

(5) Error amplifier block (Error Amp3)

The error amplifier (Error Amp3) detects the DC/DC converter output voltage and outputs PWM control signals. An arbitrary output voltage can be set for 1 to 4 cells by connecting external output voltage setting resistors to the error amplifier inverting input pins.

By connecting a feedback resistor and capacitor between FB3 terminal (pin15) and –INE3 terminal (pin 16) , it is possible to create any desired level of loop gain, thereby providing stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS terminal (pin 22) . The use of error amplifier for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) detects voltage drop which occurs between both ends of the output sense resistor (R_S) due to the flow of the charge current, using the +INC1 terminal (pin 13) and –INC1 terminal (pin 12) . Then it outputs the signal amplifier by 20 times to the error amplifier (Error Amp1) at the next stage.

(7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) detects voltage drop which occurs between both ends of the output sense resistor (R_S) due to the flow of the charge current, using the +INC2 terminal (pin 24) and –INC2 terminal (pin 1) . Then it outputs the signal amplified by 20 times to the error amplifier (Error Amp2) at the next stage.

(8) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-to-pulse width modulator that controls the output duty depending on the output voltage of error amplifier (Error Amp1 to Error Amp3) .

The PWM comparator circuit compares the triangular wave generated by the triangular wave oscillator to the error amplifier output voltage and turns on the external output transistor during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(9) Output block (OUT)

The output circuit uses a totem-pole configuration capable of driving an external P-channel MOS FET.

The output “L” level sets the output amplitude to 6 V (Typ) using the voltage generated by the bias voltage block (VH) .

This results in increasing conversion efficiency and suppressing the withstand voltage of the connected external transistor in a wide range of input voltages.

(10) Power supply control block (CTL)

Setting the CTL terminal (pin 14) low places the IC in the standby mode.
(The supply current is 10 μA at maximum in the standby mode.)

CTL function table

CTL	Power
L	OFF (Standby)
H	ON (Active)

(11) Bias voltage block (VH)

The bias voltage circuit outputs V_{CC}–6 V (Typ) as the minimum potential of the output circuit. In the standby mode, this circuit outputs the potential equal to VCC.

2. Protection Functions

(1) Under-voltage lockout protection circuit (UVLO)

The transient state of when the power supply (VCC) is turned on or a momentary decrease in supply voltage/ internal reference voltage (VREF) may cause malfunctions in the control IC, resulting in breakdown or degradation of the system. To prevent such malfunctions, the under-voltage lockout protection circuit detects an internal reference voltage drop and fixes OUT terminal (pin 20) to “H” level. The system restores when the internal reference voltage reaches the threshold voltage of the under-voltage lockout protection circuit.

Protection circuit (UVLO) operation function table

At UVLO operating (VREF voltage is lower than UVLO threshold voltage.)

OUTD	OUT	CS	CVM	OVP
Hi-Z	H	L	H	H

(2) AC adapter detection block (UV Comp.)

This block detects that power-supply voltage (VCC) is lower than the battery voltage + 0.2 V (Typ) , and the OUT terminal (pin 18) fixed at the “H” level. The system restores voltage supply when the supply voltage reaches the threshold voltage of the AC adapter detection block.

Protection circuit (UV Comp.) operation function table

At UV Comp. operating (VCC voltage is lower than UV Comp. threshold voltage.)

OUTD	OUT	CS
L	H	L

3. Soft-start Function

Soft-start block (SOFT)

Connecting a capacitor to the CS terminal (pin 22) prevents rush currents from flowing upon activation of the power supply.

Using the error amplifier to detect a soft-start allows to soft-start at constant setting time intervals independent of the output load of the DC/DC converter.

4. Detection Function

(1) Constant-voltage control state detection block (CV Comp.)

Error amplifier (Error Amp3) detects the voltage at FB3 (pin 15) falling to or below 2.6 V (Typ) and outputs “L” level to the constant-voltage control state detection block output terminal (CVM, pin 5).

(2) Overvoltage detection block (OV Comp.)

Error amplifier (Error Amp3) detects the voltage at FB3 (pin 15) falling to or below 1.3 V (Typ) and outputs “H” level to the overvoltage detection block output terminal (OVP, pin 18).

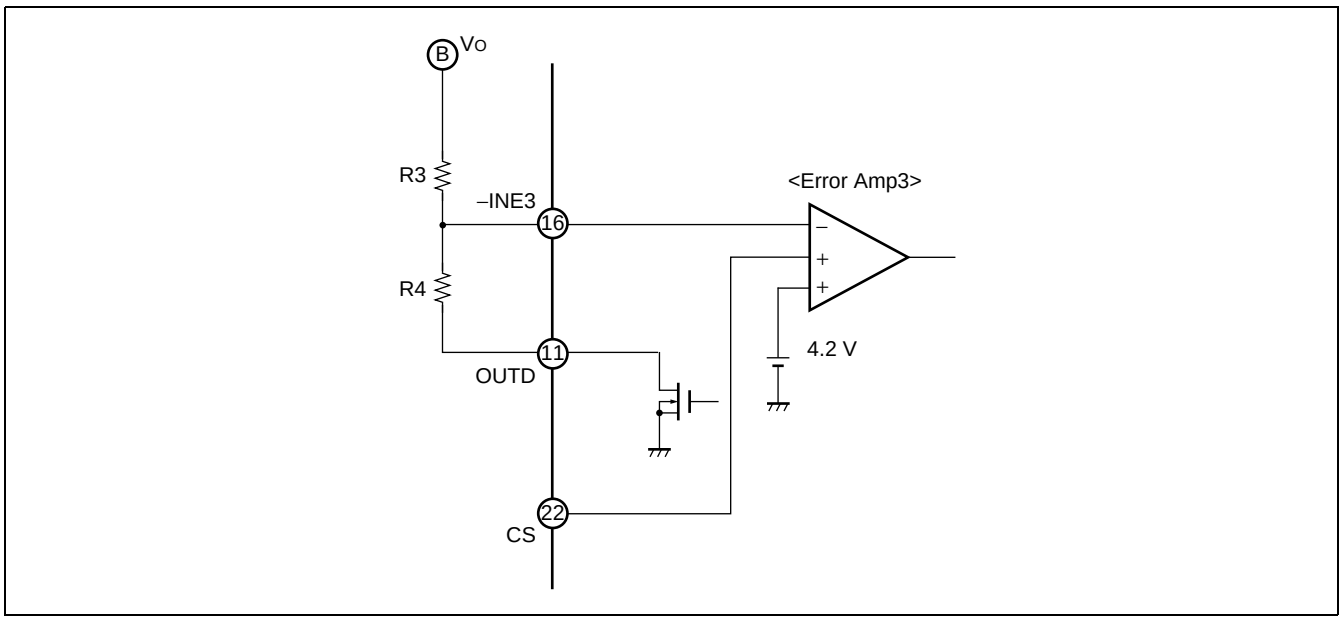
■ SETTING THE CHARGING VOLTAGE

The charge voltage (DC/DC output voltage) can be set by connecting an external output voltage setting resistors (R3, R4) to the –INE3 terminal (pin 16) .

Select a resistor value at which the on-resistor (35 Ω at 1 mA) of the built-in FET connected to the OUTD terminal (pin 11) can be ignored.

Charge voltage of battery : V_O

V_O (V) = (R3 + R4) /R4 × 4.2 (V)



■ SETTING THE CHARGING CURRENT

The charge current value (output limit current) can be set depending on the voltage value at the +INE2 terminal (pin 3) .

If a current exceeding the set current value attempts to flow, the charge voltage drops according to the set current value.

Battery charge current setting voltage : + INE2

+ INE2 (V) = 20 × I1 (A) × R_S (Ω)

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency is determined by the timing resistor (R_T) connected to the RT terminal (pin 17) .

Triangular wave oscillation frequency : fosc

fosc (kHz) ≒ 14100/R_T (kΩ)

■ SETTING OF SOFT-START TIME

(1) Setting constant voltage mode soft-start

To prevent rush currents when the IC is turned on, the IC allows soft-start using the capacitor (C_S) connected to the CS terminal (pin 22) .

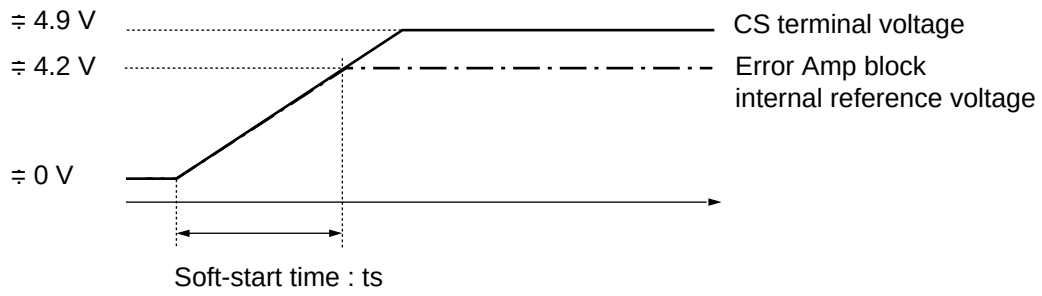
When the CTL terminal (pin 14) is placed under “H” level and IC is activated (threshold voltage of $V_{CC} \geq$ UVLO) , and Q2 is turned off and the external soft-start capacitor (C_S) connected to the CS terminal is charged at 10 μA.

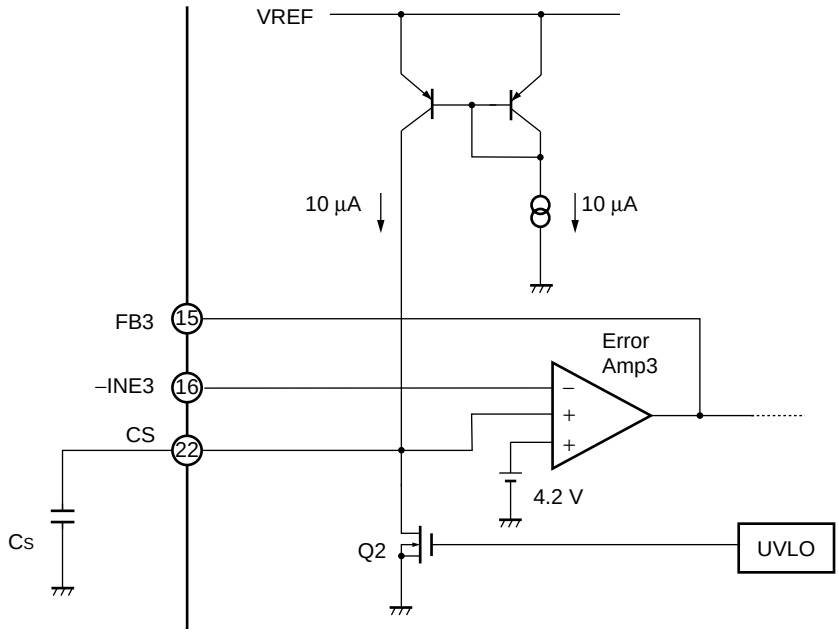
The Error Amp output potential (FB3 terminal (pin 15)) is determined through comparison between either of the lower potentials at two non-inverting input terminals (internal reference voltage (4.2 V Typ) , CS terminal voltage), and the inverting input terminal voltage (– INE3 terminal (pin 16)) . Within the soft-start period (CS terminal voltage < 4.2 V) , FB3 is determined by comparison between – INE3 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.

The soft-start time is obtained from the following formula.

Soft-start time : ts (time until output voltage 100%)

ts (s) ≒ 0.42 × C_S (μF)





Soft-start circuit

(2) Setting constant current mode soft-start

To prevent rush currents when the IC is turned on, the IC allows soft-start using the capacitor (C_S) connected to the CS terminal (pin 22) .

When the CTL terminal (pin 14) is placed under “H” level and IC is activated (threshold voltage of VREF ≥ UVLO) , and Q2 is turned off and the external soft-start capacitor (C_S) connected to the CS terminal is charged at 10 μA.

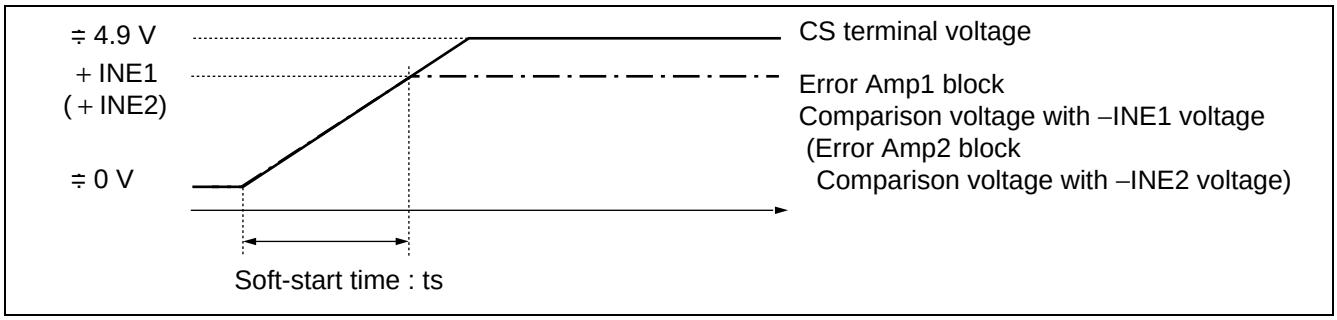
The Error Amp1 output potential (FB12 terminal (pin 7)) is determined through comparison between either of the lower potentials at two non-inverting input terminals (+ INE1 terminal (pin 9) voltage and CS terminal voltage), and the inverting input terminal voltage (– INE1 terminal (pin 8)) . Within the soft-start period (CS terminal voltage < + INE1) , FB12 is determined by comparison between – INE1 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.

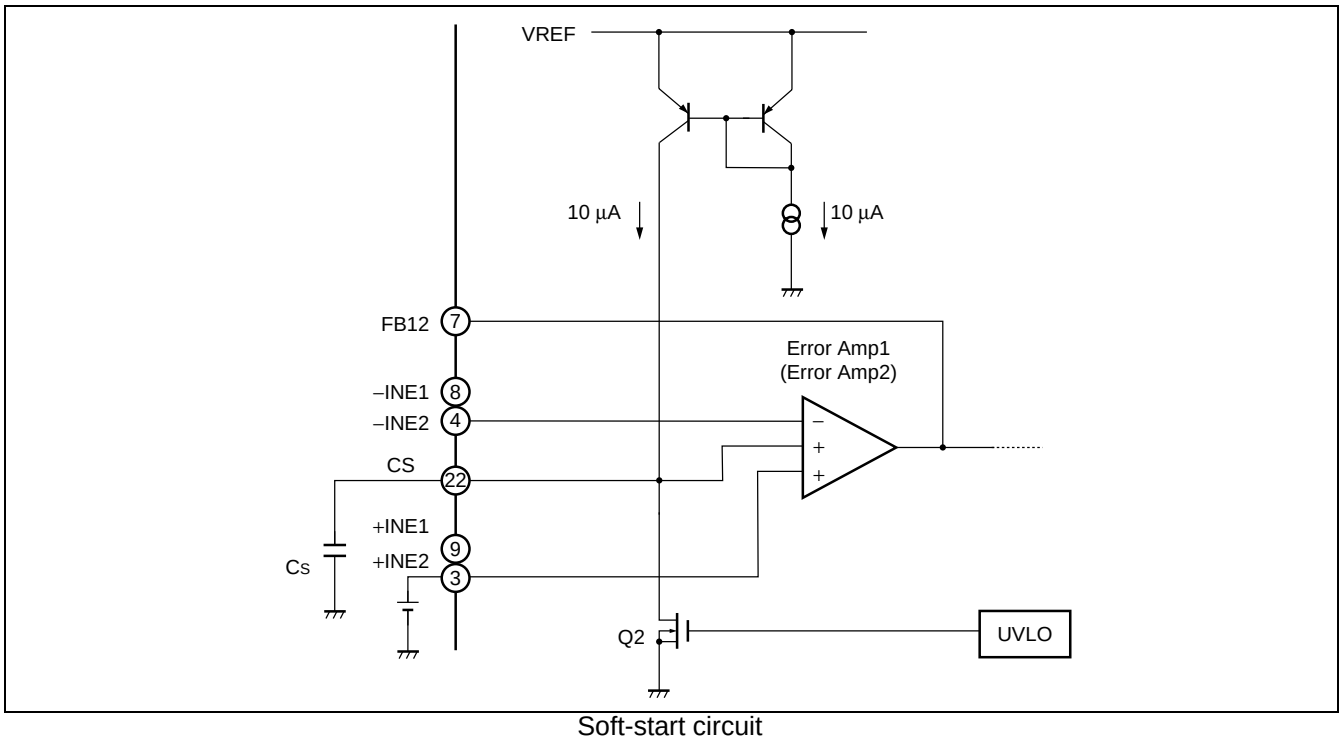
The Error Amp1 output potential (FB12 terminal (pin 7)) is determined through comparison between either of the potentials at two non-inverting input terminals (+ INE2 terminal (pin 3)) voltage and CS terminal voltage), and the inverting input terminal voltage (– INE2 terminal (pin 4)) . Within the soft-start period (CS terminal voltage < + INE2) , FB12 is determined by comparison between – INE2 terminal voltage and CS terminal voltage, and DC/DC converter output voltage goes up proportionately with the increase of CS terminal voltage caused by charging on the soft-start capacitor.

The soft-start time is obtained from the following formula.

Soft-start time : ts (time until output voltage 100%)

ts (s) ≒ + INE1 (+ INE2) /10 μA × C_S (μF)





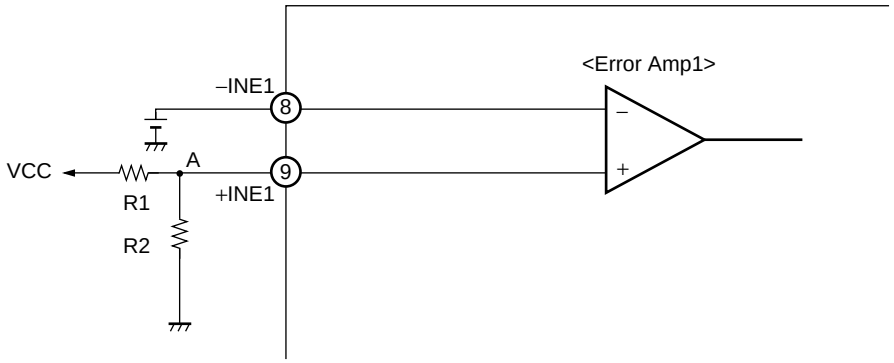
Soft-start circuit

■ SETTING THE DYNAMICALLY-CONTROLLED CHARGING

With an external resistor connected to + INE1(pin 9), the IC enters the dynamically-controlled charging mode to reduce the charge current to keep AC adapter power constant when the partial potential point A of the AC adapter voltage (VCC) become lower the – INE2 terminal voltage.

Dynamically-controlled charging setting voltage : Vth

Vth (V) = (R1 + R2) /R2 × –INE1

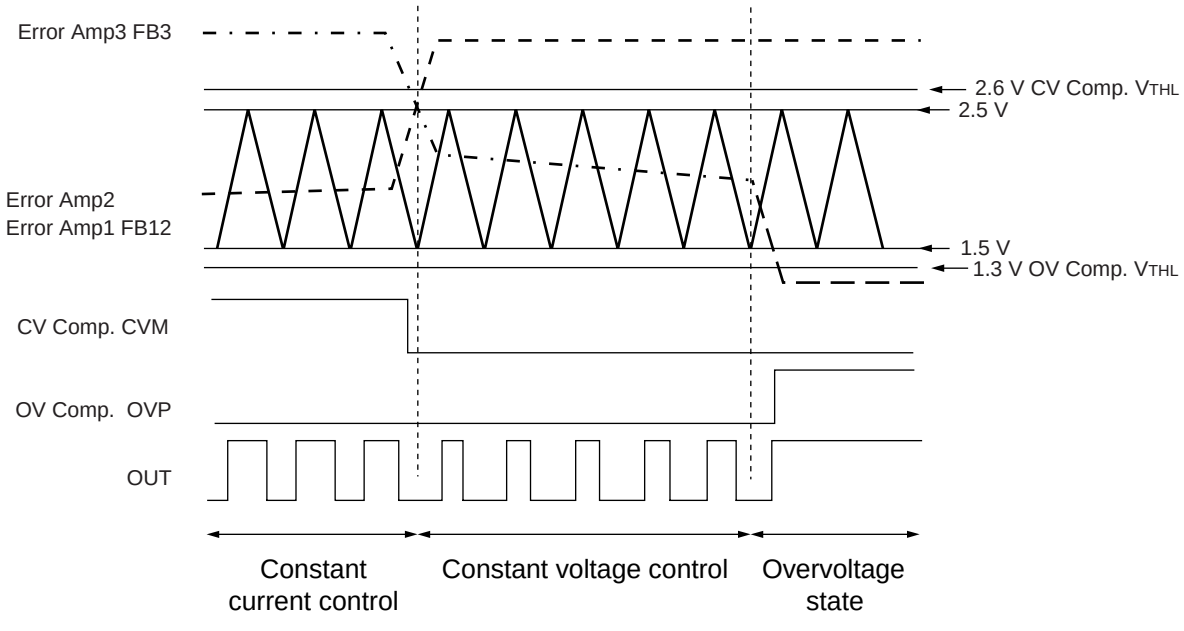


■ ABOUT CONSTANT-VOLTAGE CONTROL STATE DETECTION/OVERVOLTAGE DETECTION TIMING CHART

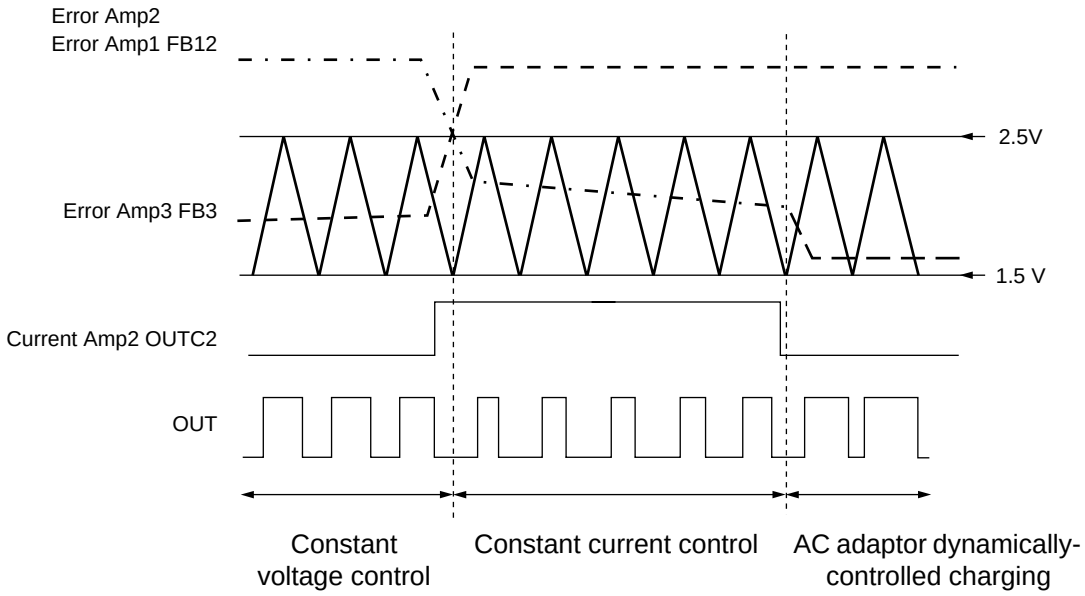
In the constant-voltage control state, the CVM terminal (pin 5) of the constant-voltage control state detection block (CV Comp.) outputs “L” level, when the voltage at the FB3 terminal (pin 15) of the error amplifier (ErrorAmp 3) becomes 2.6 V (Typ) or less.

When the DC/DC converter output voltage enters the state of the over-voltage higher than a setting voltage, the voltage at FB3 terminal (pin 15) of the error amplifier (Error Amp3) becomes 1.3 V (Typ) or less. As a result, the OVP terminal (pin 18) of the overvoltage detection block (OV Comp.) outputs “H” level.

Both the CVM terminal and the OVP terminal are open-drain output forms :



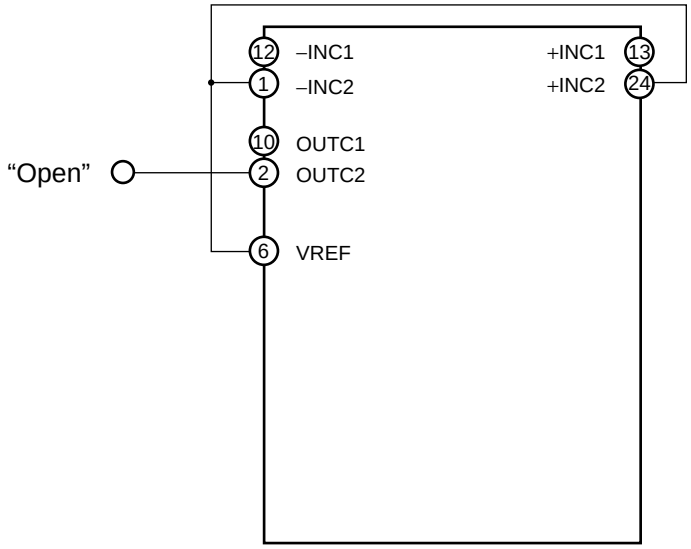
■ ABOUT THE OPERATION TIMING CHART



■ PROCESSING WITHOUT USING OF THE CURRENT AMP1 AND AMP2

When Current Amp is not used, connect the +INC1 terminal (pin 13), +INC2 terminal (pin 24), –INC1 terminal (pin 12), and –INC2 terminal (pin 1) to VREF, and open the OUTC1 terminal (pin 10) and OUTC2 terminal (pin 2).

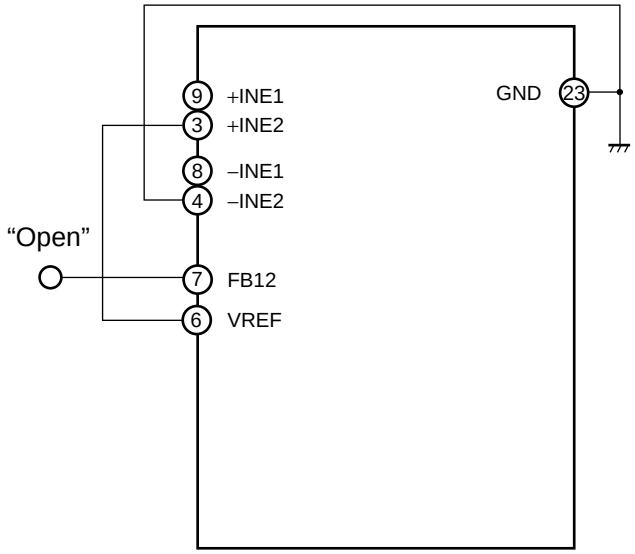
• Connection when Current Amp is not used



■ PROCESSING WITHOUT USING OF THE ERROR AMP1 AND AMP2

When Error Amp is not used, leave the FB12 terminal (pin 7) open and connect the –INE1 terminal (pin 8) and –INE2 terminal (pin 4) to GND, and connect +INE1 terminal (pin 9) and +INE2 terminal (pin 3) to VREF.

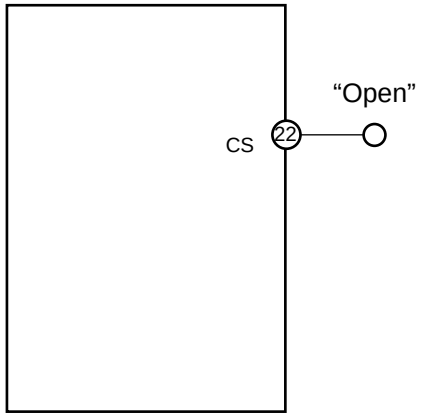
• Connection when Error Amp is not used



■ PROCESSING WITHOUT USING OF THE CS TERMINAL

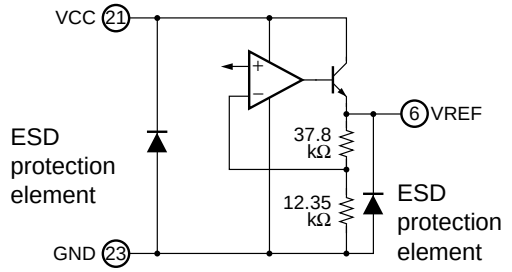
When soft-start function is not used, leave the CS terminal (pin 22) open.

- When no soft-start function is specified

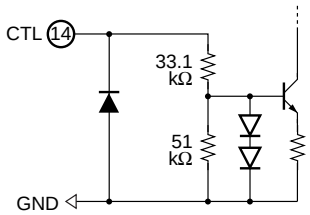


■ I/O EQUIVALENT CIRCUIT

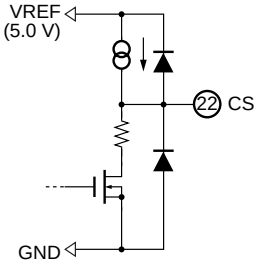
Reference voltage block



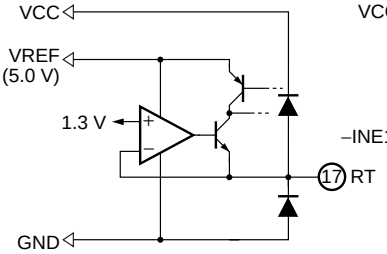
Control block



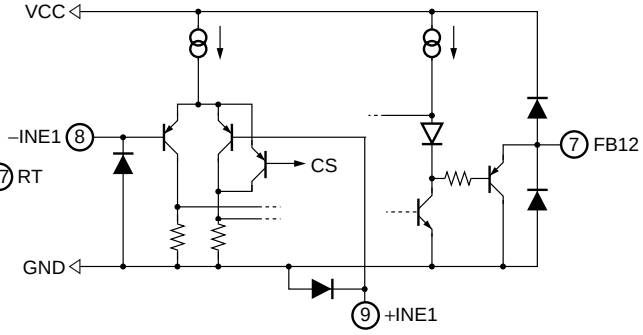
Soft-start block



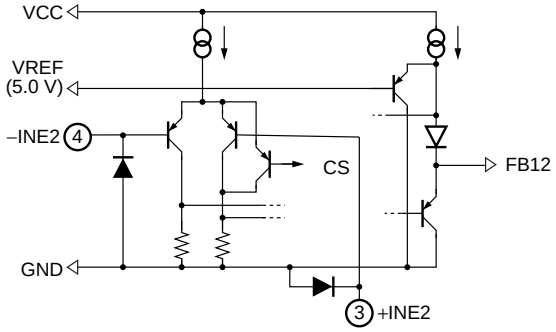
Triangular wave oscillator block



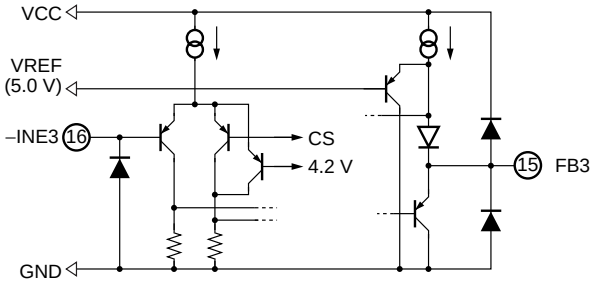
Error amplifier block (Error Amp1)



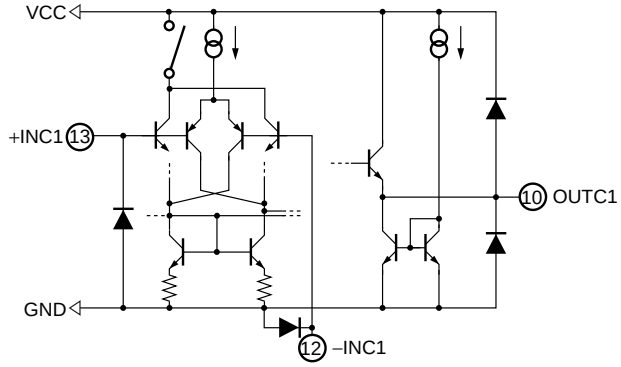
Error amplifier block (Error Amp2)



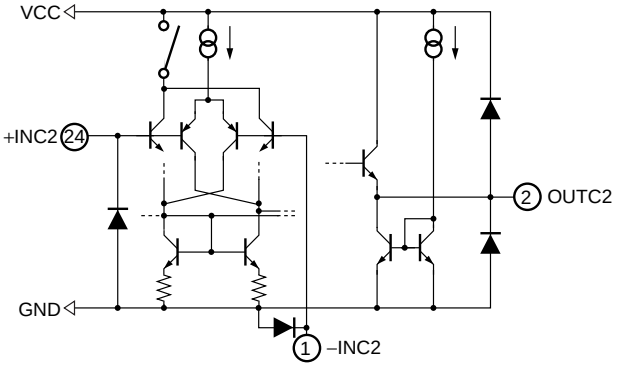
Error amplifier block (Error Amp3)



Current detection amplifier block (Current Amp1)



Current detection amplifier block (Current Amp2)



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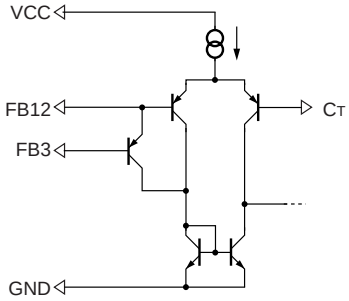
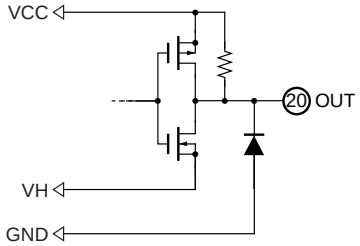
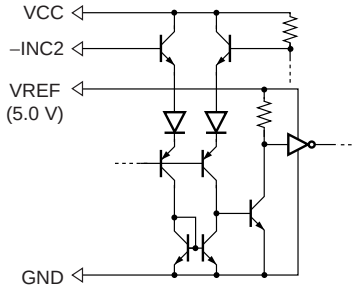
PWM comparator block



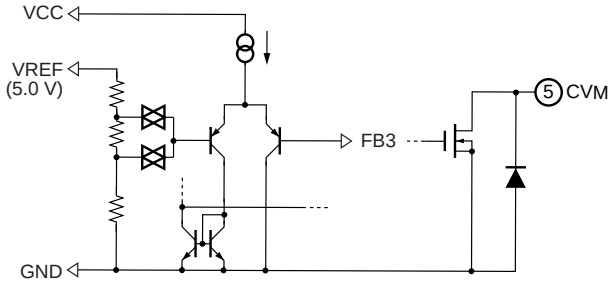
Output block



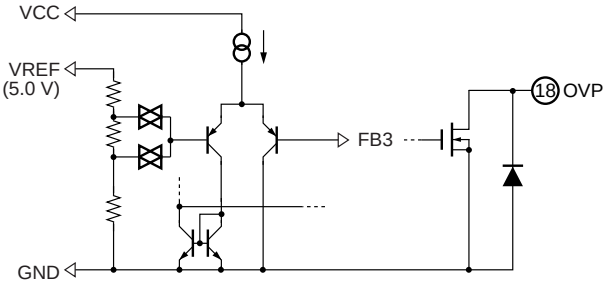
AC adaptor detection block



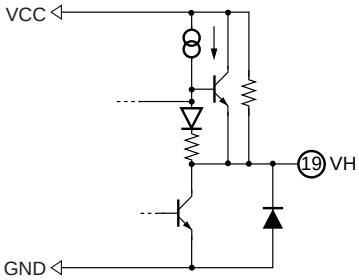
Constant-voltage control state detection block



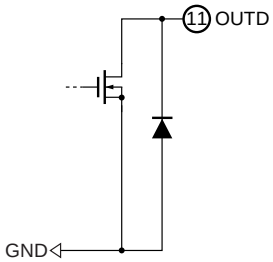
Overvoltage detection block



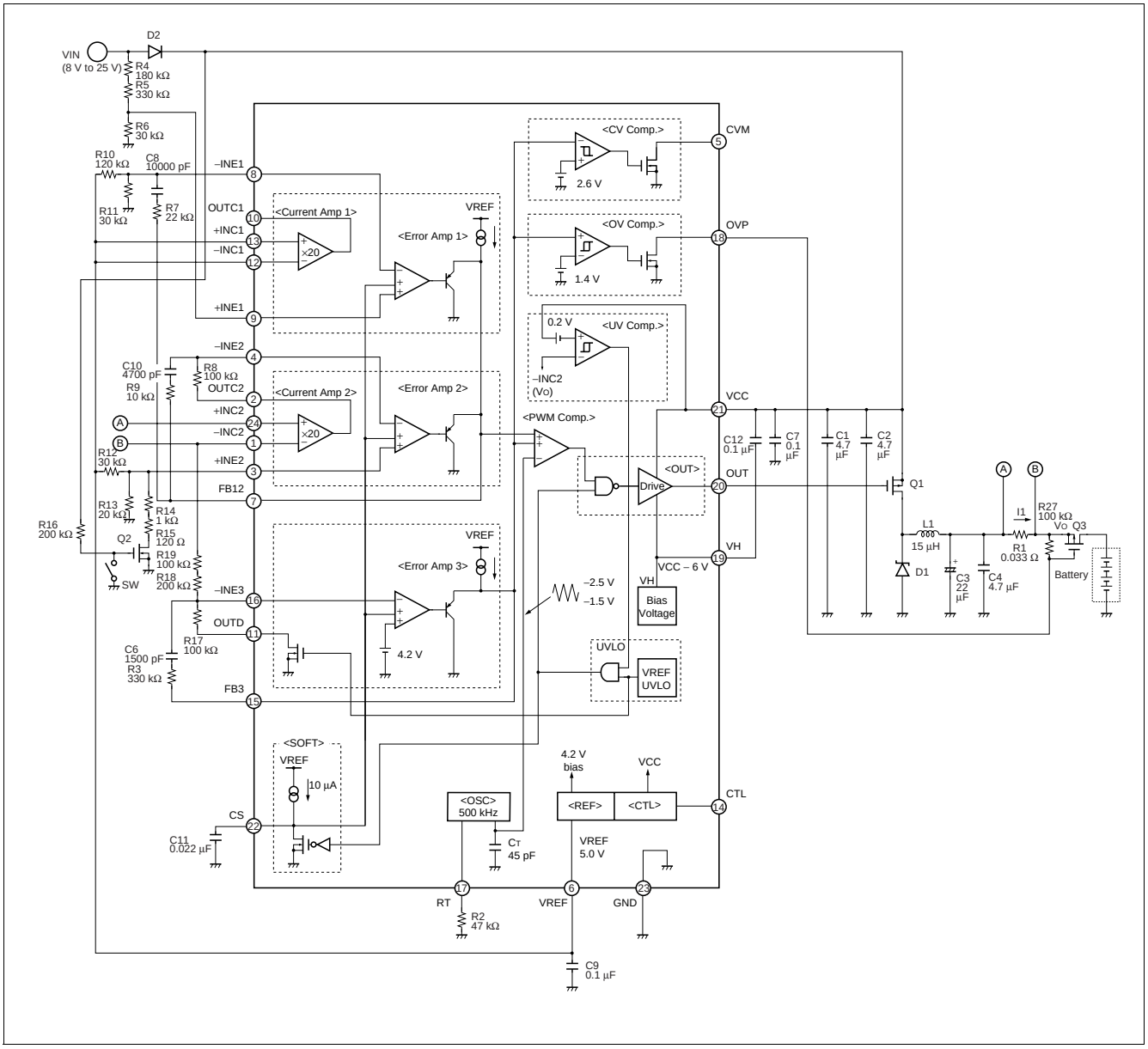
Bias voltage block



Prevent inefficient current block



■ APPRICATION EXAMPLE



■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q3 Q2	Pch FET Nch FET	VDS = –30 V, ID = –7.0 A VDS = 30 V, ID = 1.4 A		NEC SANYO	µPA2714GR MCH3401
D1, D2	Diode	VF = 0.42 V (Max) , At IF = 3 A		ROHM	RB053L-30
L1	Inductor	15 µH	3.6 A, 50 mΩ	SUMIDA	CDRH104R-150
C1, C2, C4	Ceramics Condenser	4.7 µF	25 V	TDK	C3225JB1E475K
C3	OS-CON™	22 µF	20 V	SANYO	20SVP22M
C6	Ceramics Condenser	1500 pF	50 V	TDK	C1608JB1H152K
C7, C9	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C8	Ceramics Condenser	0.01 µF	50 V	TDK	C1608JB1H103K
C10	Ceramics Condenser	4700 pF	50 V	TDK	C1608JB1H472K
C11	Ceramics Condenser	0.022 µF	50 V	TDK	C1608JB1H223K
C12	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
R1	Resistor	33 mΩ	1%	KOA	SL1TTE33LOF
R2	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R3, R5	Resistor	330 kΩ	0.5%	ssm	RR0816P-334-D
R4	Resistor	180 kΩ	0.5%	ssm	RR0816P-184-D
R6	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R7	Resistor	22 kΩ	0.5%	ssm	RR0816P-223-D
R8	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R9	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R10	Resistor	120 kΩ	0.5%	ssm	RR0816P-124-D
R11, R12	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R13	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R14	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R15	Resistor	120 Ω	0.5%	ssm	RR0816P-121-D
R16, R18	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D
R17, R19	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R27	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D

Note : NEC : NEC Corporation
SANYO : SANYO Electric Co., Ltd
ROHM : ROHM CO., LTD.
SUMIDA : Sumida Corporation
TDK : TDK Corporation
KOA : KOA Corporation
ssm : SUSUMU CO., LTD
OS-CON is a trademark of SANYO Electric Co., Ltd.

■ SELECTION OF COMPONENTS

• Pch MOS FET

The P-channel MOSFET for switching use should be rated for at least + 20% more than the input voltage. To minimize continuity loss, use a FET with low $R_{DS\,(ON)}$ between the drain and source. For high input voltage and high frequency operation, on-cycle switching loss will be higher so that power dissipation must be considered. In this application, the µPA2714GR (NEC products) is used. Continuity loss, on/off switching loss and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values.

Continuity loss : Pc

$$P_C = I_D^2 \times R_{DS\,(ON)} \times \text{Duty}$$

On-cycle switching loss : $P_{S\,(ON)}$

$$P_{S\,(ON)} = \frac{V_{D\,(Max)} \times I_D \times tr \times fosc}{6}$$

Off-cycle switching loss : $P_{S\,(OFF)}$

$$P_{S\,(OFF)} = \frac{V_{D\,(Max)} \times I_{D\,(Max)} \times tf \times fosc}{6}$$

Total loss : P_T

$$P_T = P_C + P_{S\,(ON)} + P_{S\,(OFF)}$$

Example) Using the µPA2714GR

Setting 16.8 V

Input voltage $V_{IN} = 25$ V, output voltage $V_O = 16.8$ V, drain current $I_D = 3$ A, oscillation frequency fosc = 300 kHz, L = 15 µH, drain-source ON resistance $R_{DS\,(ON)} \fallingdotseq 18$ mΩ, tr ≒ 15 ns, tf ≒ 42 ns

Drain current (Max) : $I_{D\,(Max)}$

$$I_{D\,(Max)} = Io + \frac{V_{IN} - Vo}{2L} \times t_{ON}$$

$$= 3 + \frac{25 - 16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{3.6\ A}$$

Drain current (Min) : $I_{D\,(Min)}$

$$I_{D\,(Min)} = Io - \frac{V_{IN} - Vo}{2L} \times t_{ON}$$

$$= 3 - \frac{25 - 16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{2.4\ A}$$

$$P_C = I_D^2 \times R_{DS\,(ON)} \times \text{Duty}$$

$$= 3^2 \times 0.018 \times 0.672$$

$$\fallingdotseq \underline{0.109\ W}$$

$$P_S\,(ON) = \frac{V_D \times I_D \times tr \times fosc}{6}$$
$$= \frac{25 \times 3 \times 15 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.056\ W}$$

$$P_S\,(OFF) = \frac{V_D \times I_D\,(Max) \times tf \times fosc}{6}$$
$$= \frac{25 \times 3.6 \times 42 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.189\ W}$$

$$P_T = PC + P_S\,(ON) + P_S\,(OFF)$$
$$\fallingdotseq 0.109 + 0.056 + 0.189$$
$$\fallingdotseq 0.354\ W$$

The above power dissipation figures for the µPA2714GR are satisfied with ample margin at 2.0 W.

Setting 12.6 V

Input voltage V_{IN} = 22 V, output voltage V_O = 12.6 V, drain current I_D = 3 A, oscillation frequency fosc = 300 kHz, L = 15 µH, drain-source ON resistance $R_{DS}\,(ON)$ ≒ 18 mΩ, tr ≒ 15 ns, tf ≒ 42 ns

Drain current (Max) : $I_D\,(Max)$

$$I_D\,(Max) = Io + \frac{V_{IN} - Vo}{2L}\ t_{ON}$$
$$= 3 + \frac{22 - 12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$
$$\fallingdotseq \underline{3.6\ A}$$

Drain current (Min) : $I_D\,(Min)$

$$I_D\,(Min) = Io - \frac{V_{IN} - Vo}{2L}\ t_{ON}$$
$$= 3 - \frac{22 - 12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$
$$\fallingdotseq \underline{2.4\ A}$$

$$P_C = I_D^2 \times R_{DS}\,(ON) \times Duty$$
$$= 3^2 \times 0.018 \times 0.572$$
$$\fallingdotseq \underline{0.093\ W}$$

$$P_S\,(ON) = \frac{V_D \times I_D \times tr \times fosc}{6}$$
$$= \frac{22 \times 3 \times 15 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.050\ W}$$

$$P_S\,(OFF) = \frac{V_D \times I_D\,(Max) \times tf \times fosc}{6}$$
$$= \frac{22 \times 3.6 \times 42 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.166\ W}$$

$$P_T = PC + P_S\,(ON) + P_S\,(OFF)$$
$$\fallingdotseq 0.093 + 0.050 + 0.166$$
$$\fallingdotseq \underline{0.309\ W}$$

The above power dissipation figures for the µPA2714GR are satisfied with ample margin at 2.0 W.

• Inductor

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light-load.

Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.

Note also that the DC superimposition characteristic becomes worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency.

The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current.

Inductance values are determined by the following formulas.

The L value for all load current conditions is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

Inductance value : L

$$L \geq \frac{2\,(V_{IN} - Vo)}{Io}\ t_{ON}$$

16.8 V output
Example)

$$L \geq \frac{2\,(V_{IN}\,(Max) - Vo)}{Io}\ t_{ON}$$
$$\geq \frac{2 \times (25 - 16.8)}{3} \times \frac{1}{300 \times 10^3} \times 0.672$$
$$\geq \underline{12.2\ \mu H}$$

12.6 V output
Example)

$$L \geq \frac{2\,(V_{IN}\,(Max) - Vo)}{Io}\ t_{ON}$$

$$\geq \frac{2 \times (22-12.6)}{3} \times \frac{1}{300 \times 10^3} \times 0.572$$

$$\geq \underline{12.0\ \mu H}$$

Inductance values derived from the above formulas are values that provide sufficient margin for continuous operation at maximum load current, but at which continuous operation is not possible at light-loads. So, it is necessary to determine the load level at which continuous operation becomes possible. In this application, the SUMIDA CDRH104R-150 is used. The following equation is available to obtain the load current as a continuous current condition when 15 μH is used.

The load current value under continuous operating conditions : Io

$$Io \geq \frac{Vo}{2L}\ t_{OFF}$$

Example) Using the CDRH104R-150

15 μH (tolerance ± 30%) , rated current = 3.6 A

16.8 V output

$$Io \geq \frac{Vo}{2L}\ t_{OFF}$$

$$\geq \frac{16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.672)$$

$$\geq \underline{0.61\ A}$$

12.6 V output

$$Io \geq \frac{Vo}{2L}\ t_{OFF}$$

$$\geq \frac{12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1-0.572)$$

$$\geq \underline{0.60\ A}$$

To determine whether the current through the inductor is within rated values, it is necessary to determine the peak value of the ripple current as well as the peak-to-peak values of the ripple current that affect the output ripple voltage.

The peak value and peak-to-peak value of the ripple current can be determined by the following formulas.

Peak value : I_L

$$I_L \geq Io + \frac{V_{IN}-Vo}{2L}\ t_{ON}$$

Peak-peak value : ΔI_L

$$\Delta I_L = \frac{V_{IN}-Vo}{L}\ t_{ON}$$

Example) Using the CDRH104R-150
15 μH (tolerance ± 30%) , rated current = 3.6 A

Peak value
16.8 V output

$$I_L \geq Io + \frac{V_{IN}-Vo}{2L} t_{ON}$$

$$\geq 3 + \frac{25-16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\geq \underline{3.6\ A}$$

12.6 V output

$$I_L \geq Io + \frac{V_{IN}-Vo}{2L} t_{ON}$$

$$\geq 3 + \frac{22-12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$

$$\geq \underline{3.6\ A}$$

Peak-peak value
16.8 V output

$$\Delta I_L = \frac{V_{IN}-Vo}{L} t_{ON}$$

$$= \frac{25-16.8}{15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{1.22\ A}$$

12.6 V output

$$\Delta I_L = \frac{V_{IN}-Vo}{L} t_{ON}$$

$$= \frac{22-12.6}{15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$

$$\fallingdotseq \underline{1.2\ A}$$

• Flyback diode

As a flyback diode, in general, a Schottky barrier diode (SBD) is used when the reverse voltage to the diode is 40 V or less. The SBD has the characteristic of higher speed in terms of faster reverse recovery time, and lower forward voltage, and is ideal for archiving high efficiency. There is no problem as long as the DC reverse voltage is sufficiently higher than the input voltage, and the mean current flowing during the diode conduction time is within the mean output current level, and as the peak current is within the peak surge current limits.

In this application the RB053L-30 (ROHM) are used. The diode mean current and diode peak current can be obtained by the following formulas.

Diode mean current : I_{Di}

$$I_{Di} \geq Io \times \left(1 - \frac{Vo}{V_{IN}}\right)$$

Diode peak current : I_{Dip}

$$I_{Dip} \geq \left(Io + \frac{Vo}{2L} t_{OFF}\right)$$

Example) Using the RB053L-30

VR (DC reverse voltage) = 30 V, average output current = 3.0 A, peak surge current = 70 A

VF (forward voltage) = 0.42 V, at IF = 3.0 A

16.8 V output

$$I_{Di} \geq Io \times \left(1 - \frac{Vo}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.672)$$

$$\geq \underline{0.984\ A}$$

12.6 V output

$$I_{Di} \geq Io \times \left(1 - \frac{Vo}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.572)$$

$$\geq \underline{1.284\ A}$$

16.8 V output

$$I_{Dip} \geq \left(Io + \frac{Vo}{2L}\ t_{OFF}\right)$$

$$\geq \underline{3.6\ A}$$

12.6 V output

$$I_{Dip} \geq \left(Io + \frac{Vo}{2L}\ t_{OFF}\right)$$

$$\geq \underline{3.6\ A}$$

- **Smoothing capacitor**

The smoothing capacitor is an indispensable element for reducing ripple voltage in output. In selecting a smoothing capacitor, it is essential to consider equivalent series resistance (ESR) and allowable ripple current. Higher ESR means higher ripple voltage, so that to reduce ripple voltage it is necessary to select a capacitor with low ESR. Note, however, that the use of a capacitor with low ESR has substantial effects on loop phase characteristics, and impairing system stability. Care should also be taken to use a capacity with sufficient margin for allowable ripple current. In this application the 20SVP22M (OS-CON™ : SANYO) are used.

The ESR, capacitance value, and ripple current can be obtained by the following formulas.

Equivalent series resistance : ESR

$$ESR \leq \frac{\Delta Vo}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

Capacitance value : C_L

$$C_L \geq \frac{\Delta I_L}{2\pi f\ (\Delta Vo - \Delta I_L \times ESR)}$$

Ripple current : $IC_L rms$

$$IC_L rms \geq \frac{(V_{IN} - Vo)\ t_{ON}}{2\sqrt{3}L}$$

Example) Using the 20SVP22M

Rated voltage = 20 V, ESR = 60 mΩ, maximum allowable ripple current = 1450 mArms

Equivalent series resistance

16.8 V output

$$ESR \leq \frac{\Delta Vo}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

$$\leq \frac{0.168}{1.22} - \frac{1}{2\pi \times 300 \times 10^3 \times 22 \times 10^{-6}}$$

$$\leq \underline{114\ m\Omega}$$

12.6 V output

$$ESR \leq \frac{\Delta Vo}{\Delta I_L} - \frac{1}{2\pi f C_L}$$

$$\leq \frac{0.126}{1.2} - \frac{1}{2\pi \times 300 \times 10^3 \times 22 \times 10^{-6}}$$

$$\leq \underline{80\ m\Omega}$$

Capacitance value

16.8 V output

$$C_L \geq \frac{\Delta I_L}{2\pi f\ (\Delta Vo - \Delta I_L \times ESR)}$$

$$\geq \frac{1.22}{2\pi \times 300 \times 10^3 \times\ (0.168 - 1.22 \times 0.06)}$$

$$\geq \underline{6.8\ \mu F}$$

12.6 V output

$$C_L \geq \frac{\Delta I_L}{2\pi f\ (\Delta Vo - \Delta I_L \times ESR)}$$

$$\geq \frac{1.2}{2\pi \times 300 \times 10^3 \times\ (0.126 - 1.2 \times 0.06)}$$

$$\geq \underline{11.8\ \mu F}$$

Ripple current

16.8 V output

$$IC_Lrms \geq \frac{(V_{IN} - Vo)\ t_{ON}}{2\sqrt{3}L}$$

$$\geq \frac{(25 - 16.8)\ \times 0.672}{2\sqrt{3} \times 15 \times 10^{-6} \times 300 \times 10^3}$$

$$\geq \underline{707\ mArms}$$

12.6 V output

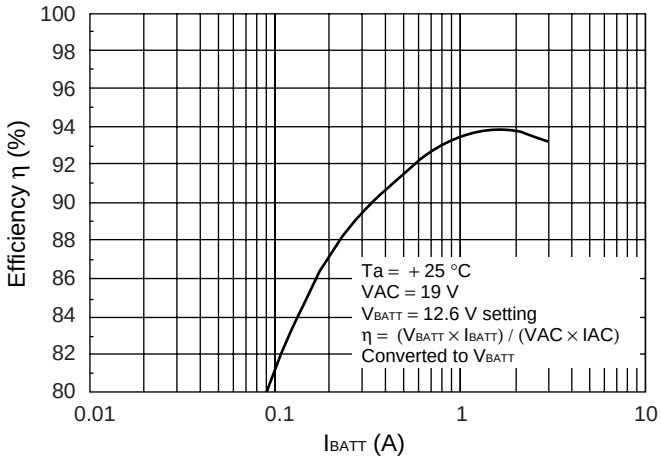
$$IC_Lrms \geq \frac{(V_{IN} - Vo)\ t_{ON}}{2\sqrt{3}L}$$

$$\geq \frac{(22 - 12.6)\ \times 0.572}{2\sqrt{3} \times 15 \times 10^{-6} \times 300 \times 10^3}$$

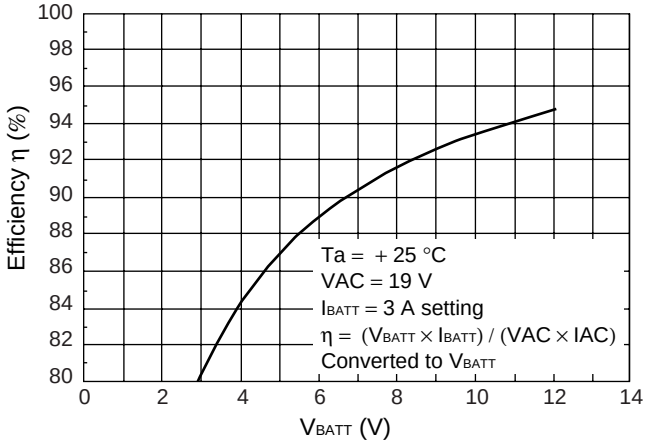
$$\geq \underline{690\ mArms}$$

■ REFERENCE DATA

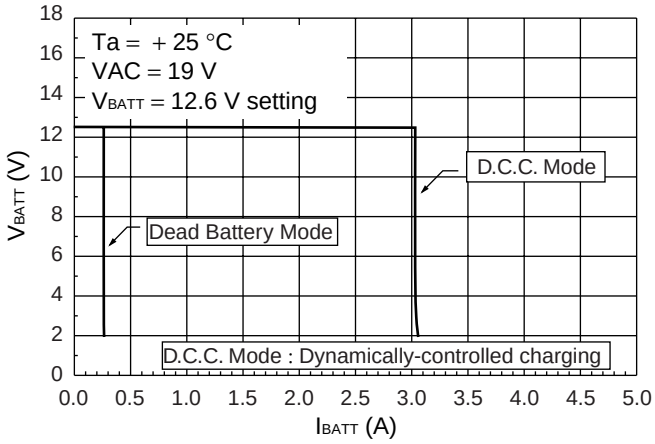
Conversion Efficiency vs. Charge Current
(constant voltage mode)



Conversion Efficiency vs. Charge Voltage
(constant current mode)



BATT Voltage vs. BATT Charge Current (12.6 V setting)



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Conversion Efficiency vs. Charge Current
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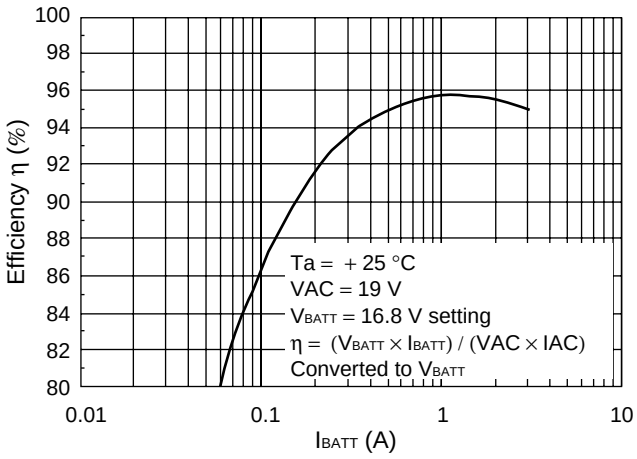
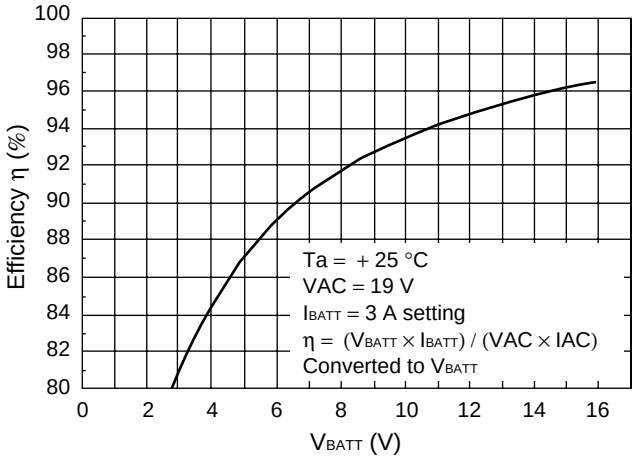
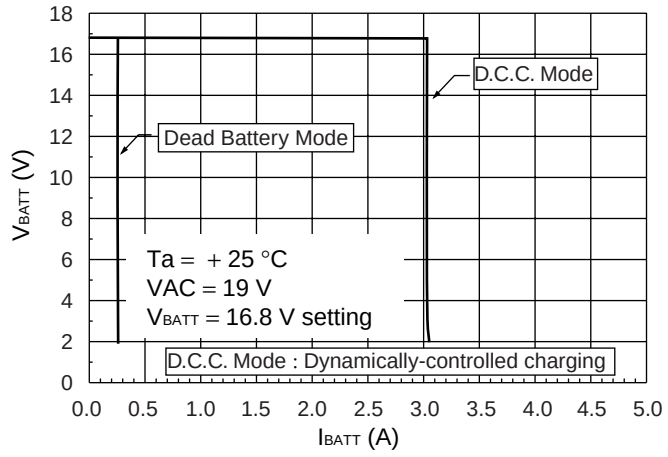


Conversion Efficiency vs. Charge Voltage
(constant current mode)



BATT Voltage vs. BATT Charge Current (16.8 V setting)



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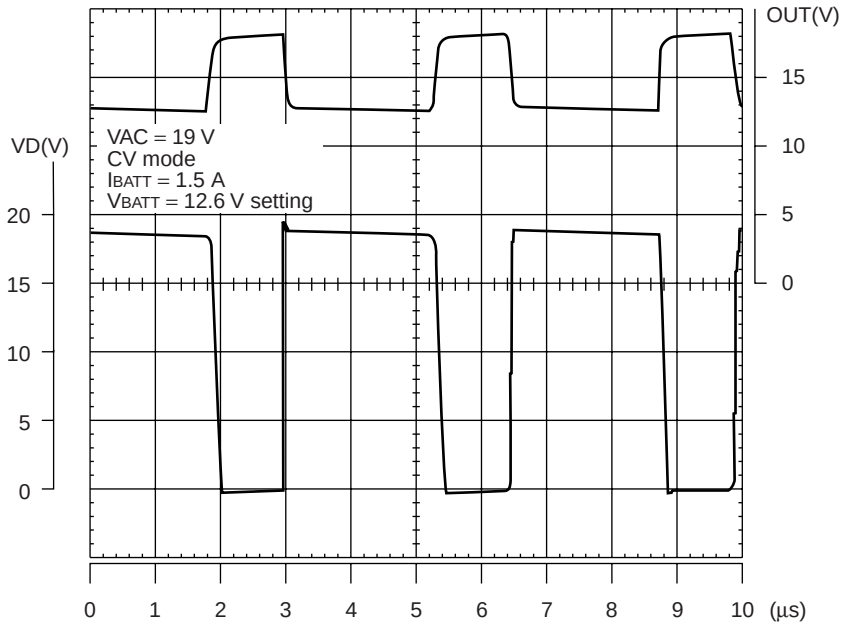
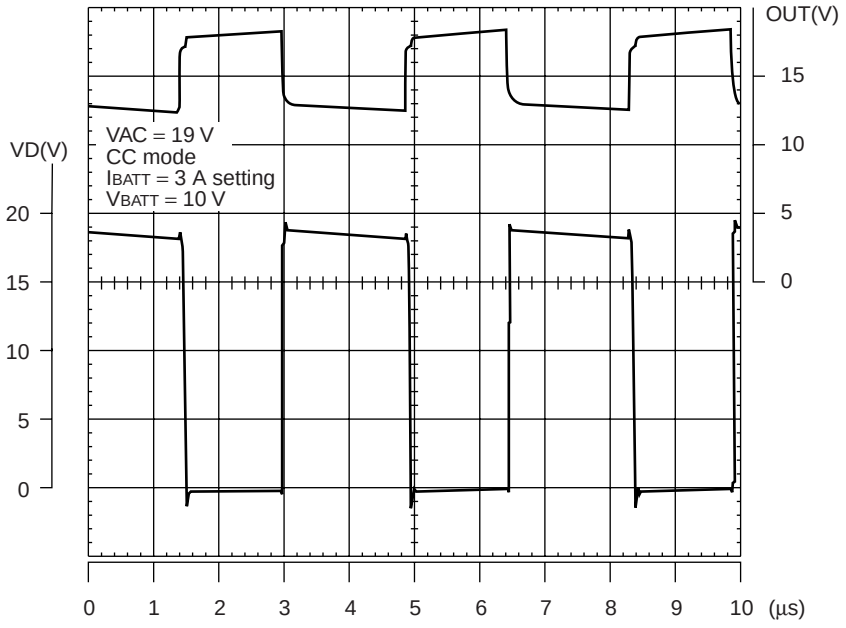
Switching Waveform at Constant Voltage Mode (12.6 V setting)



Switching Waveform at Constant Current Mode (12.6 V setting at 10 V)



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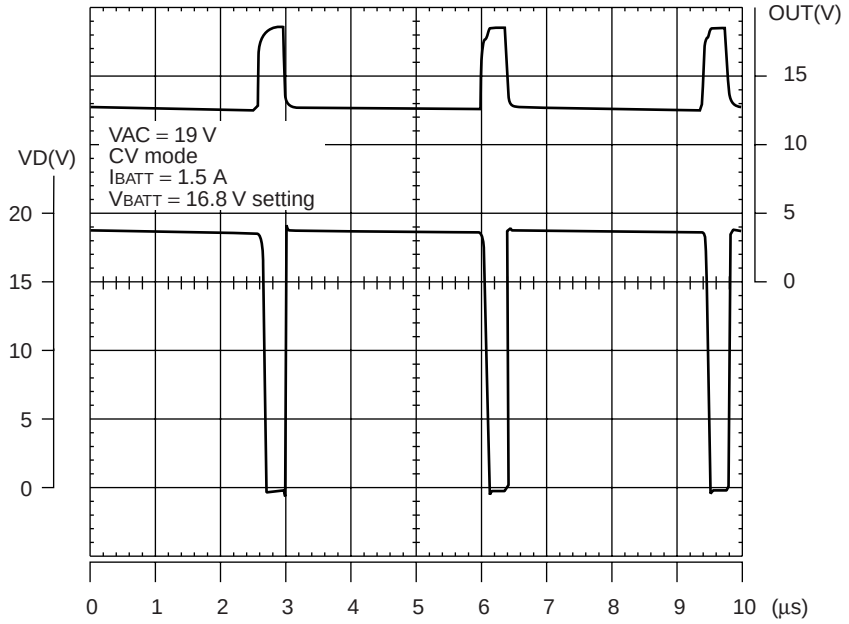
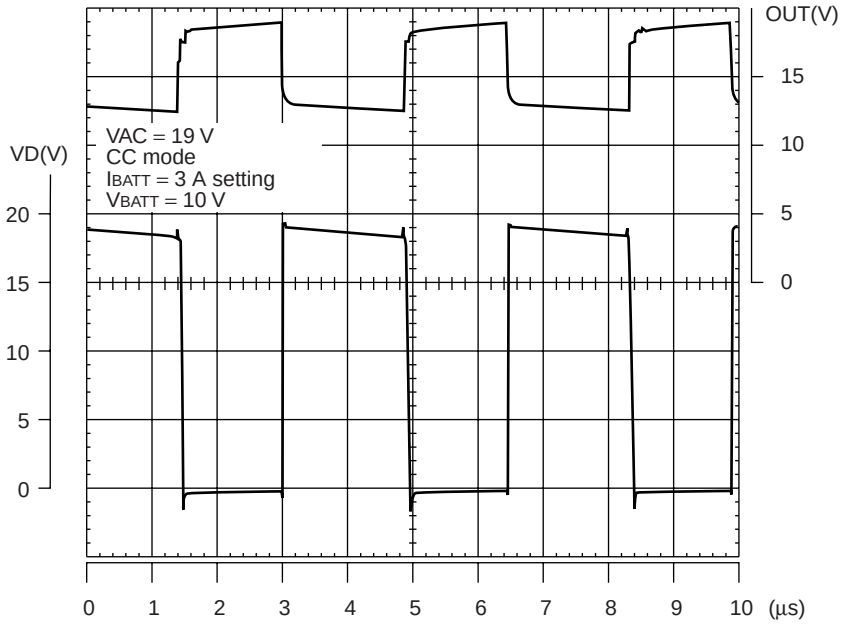
Switching Waveform at Constant Voltage Mode (16.8 V setting)



Switching Waveform at Constant Current Mode (16.8 V setting at 10 V)



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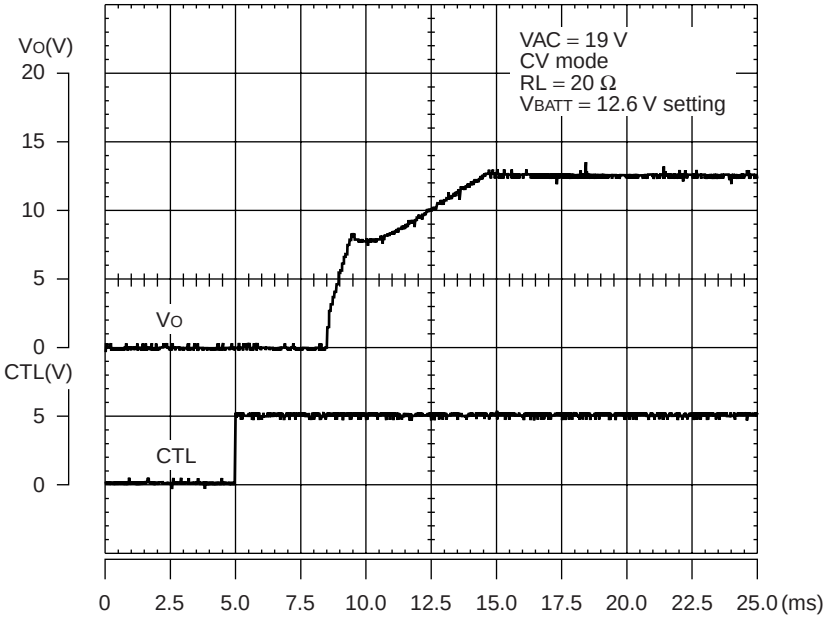
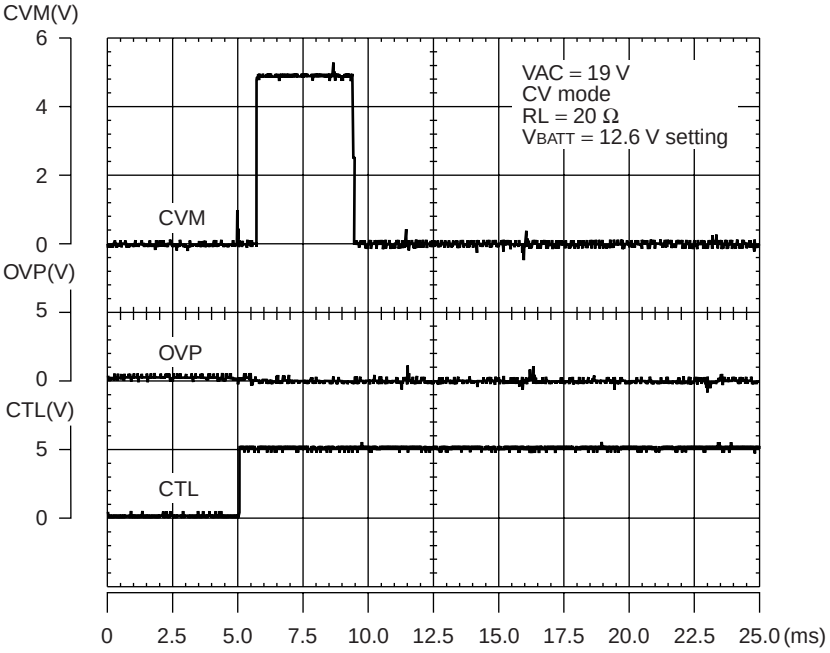
Soft-start Operating Waveform at Constant Voltage Mode (12.6 V setting) (1)



Soft-start Operating Waveform at Constant Voltage Mode (12.6 V setting) (2)



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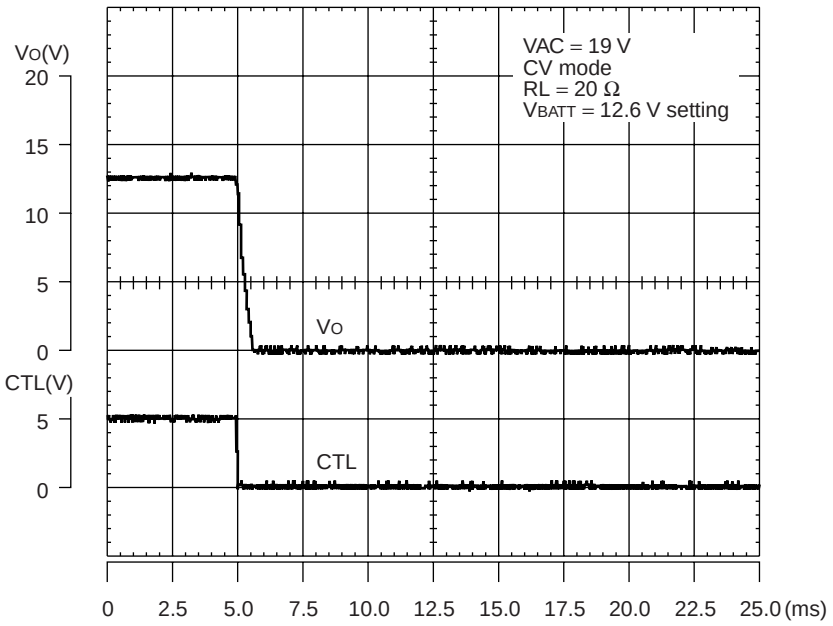
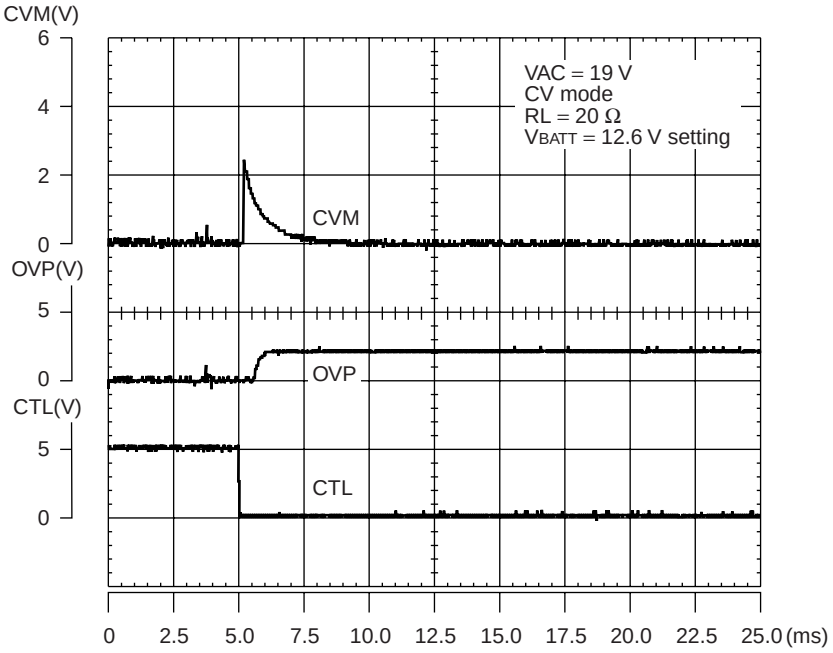
Discharge Operating Waveform at Constant Voltage Mode (12.6 V setting) (1)



Discharge Operating Waveform at Constant Voltage Mode (12.6 V setting) (2)



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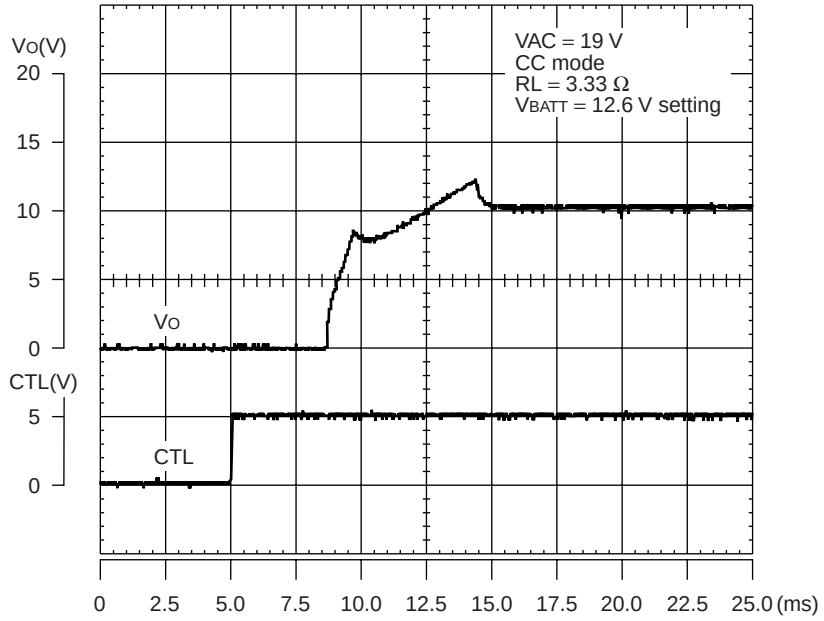
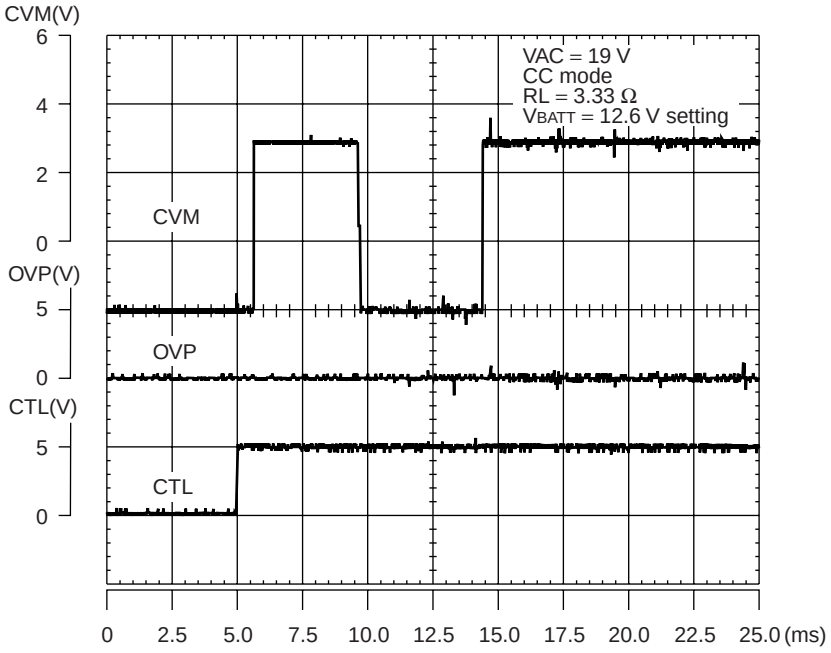
Soft-start Operating Waveform at Constant Current Mode (12.6 V setting) (1)



Soft-start Operating Waveform at Constant Current Mode (12.6 V setting) (2)



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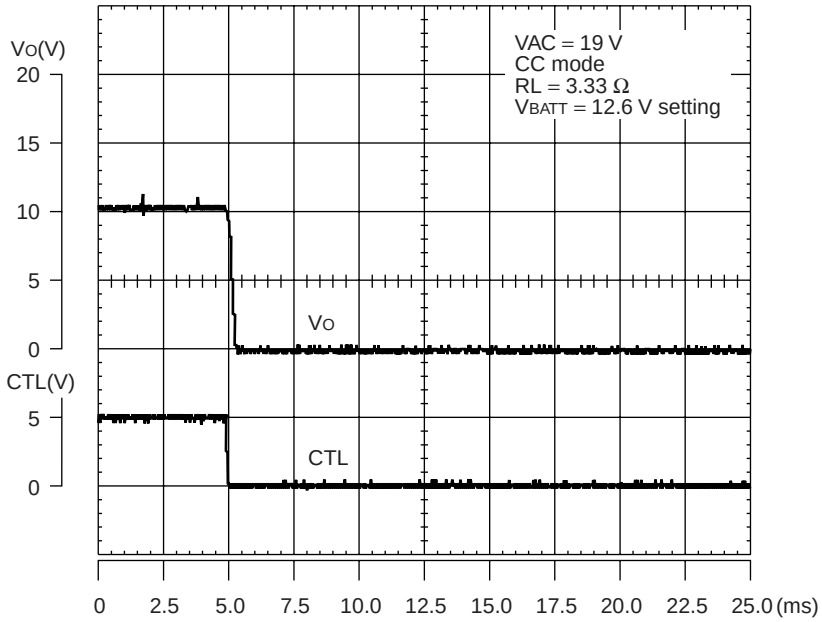
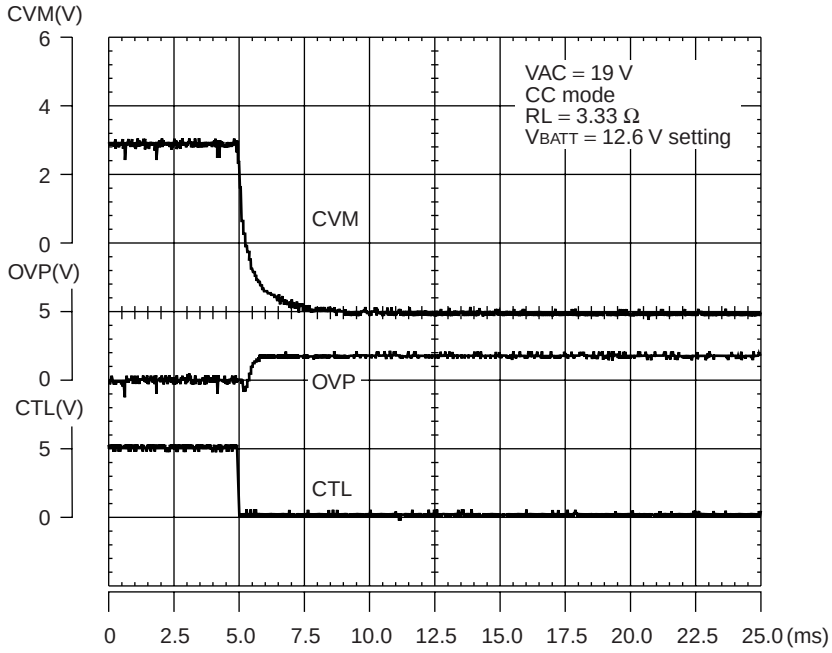
Discharge Operating Waveform at Constant Current Mode (12.6 V setting) (1)



Discharge Operating Waveform at Constant Current Mode (12.6 V setting) (2)



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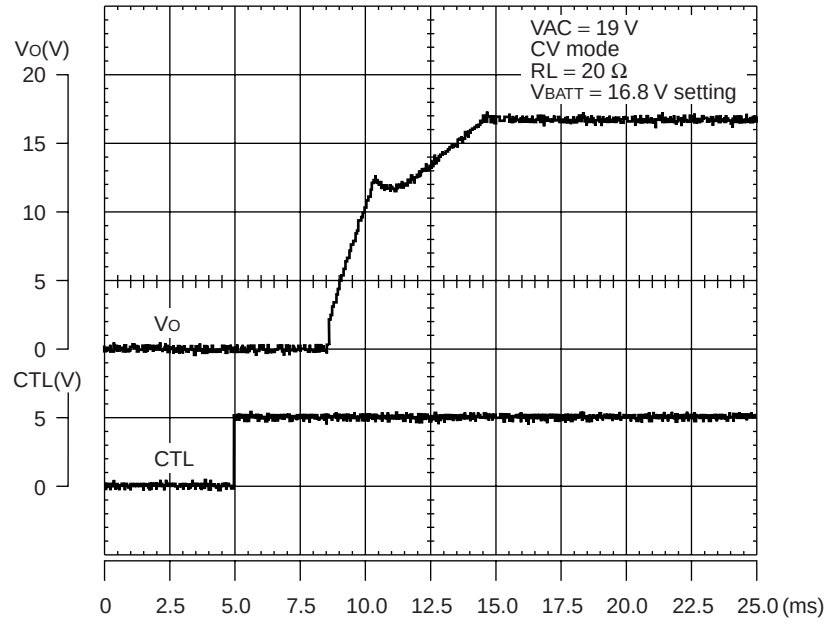
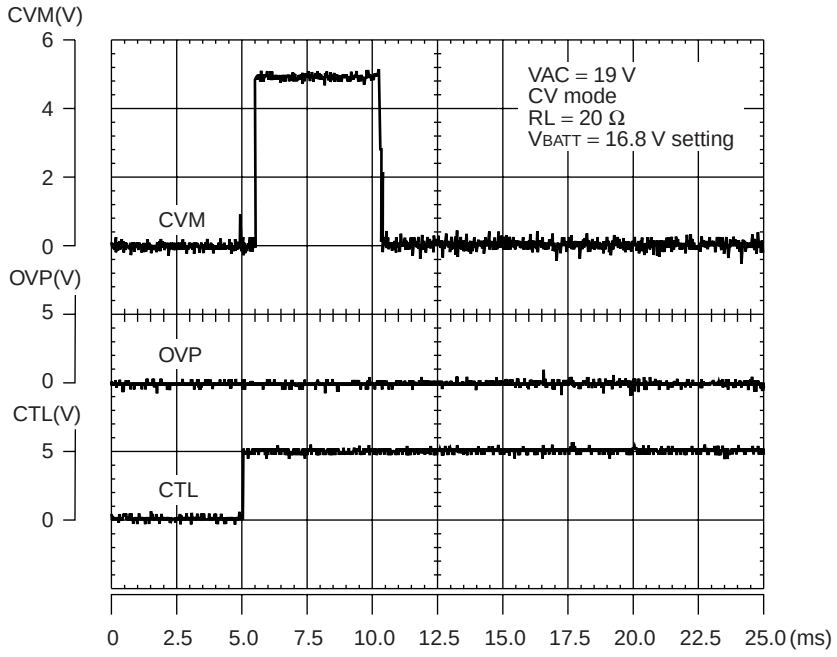
Soft-start Operating Waveform at Constant Voltage Mode (16.8 V setting) (1)



Soft-start Operating Waveform at Constant Voltage Mode (16.8 V setting) (2)



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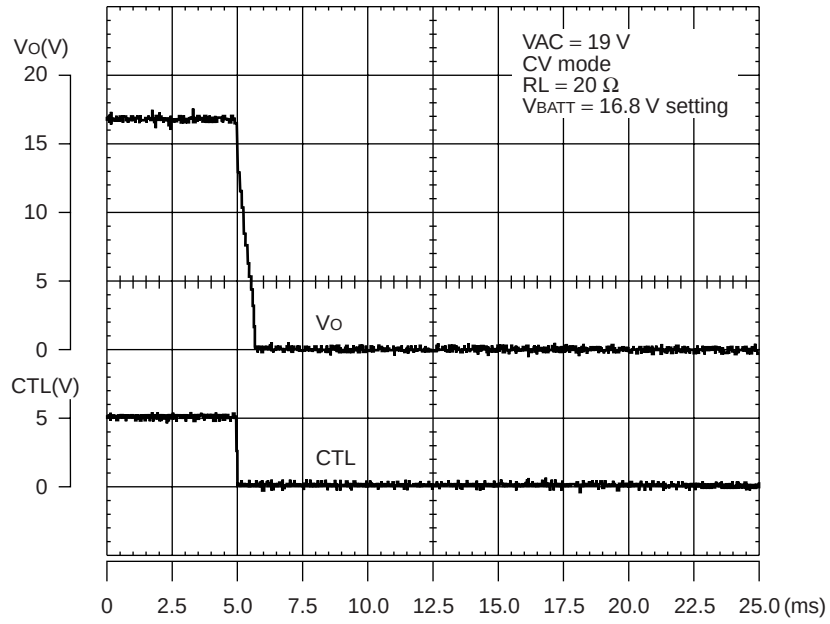
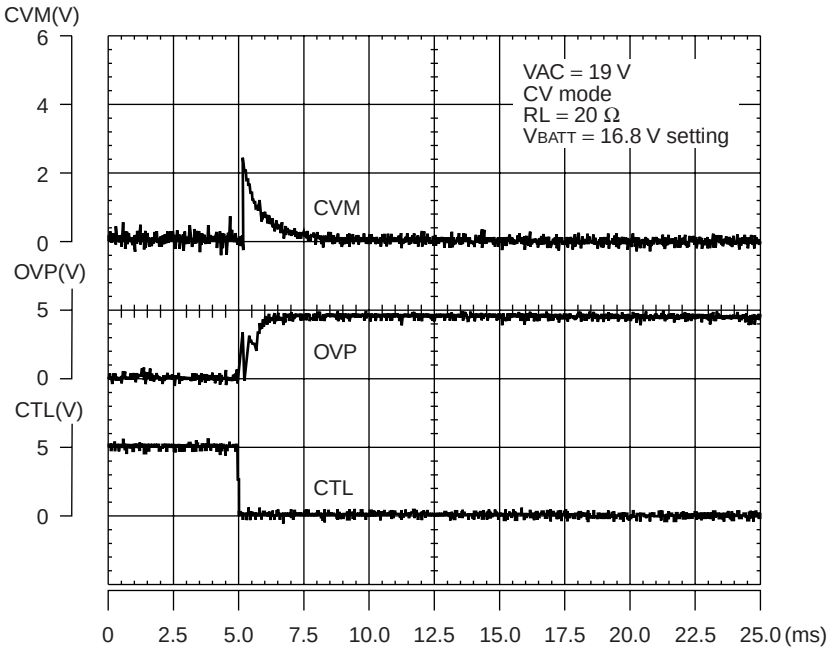
Discharge Operating Waveform at Constant Voltage Mode (16.8 V setting) (1)



Discharge Operating Waveform at Constant Voltage Mode (16.8 V setting) (2)



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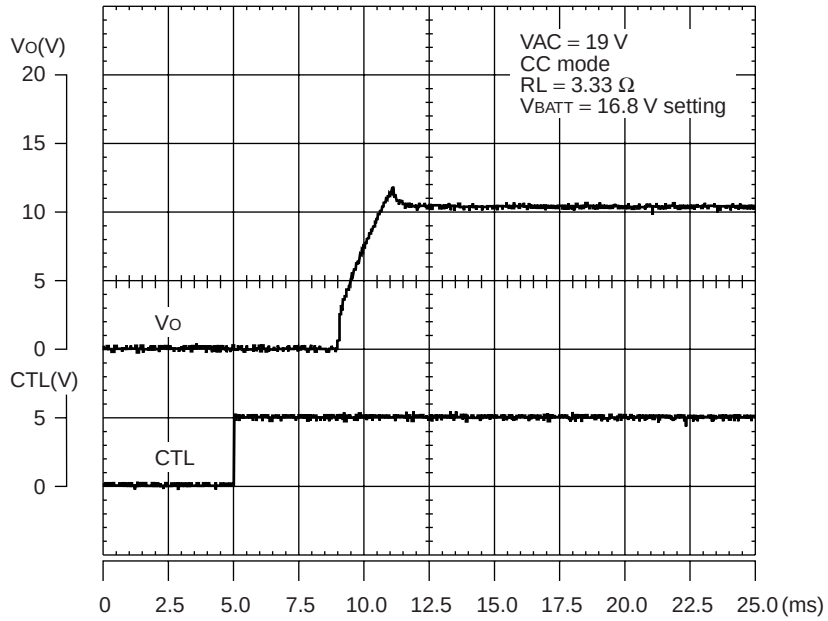
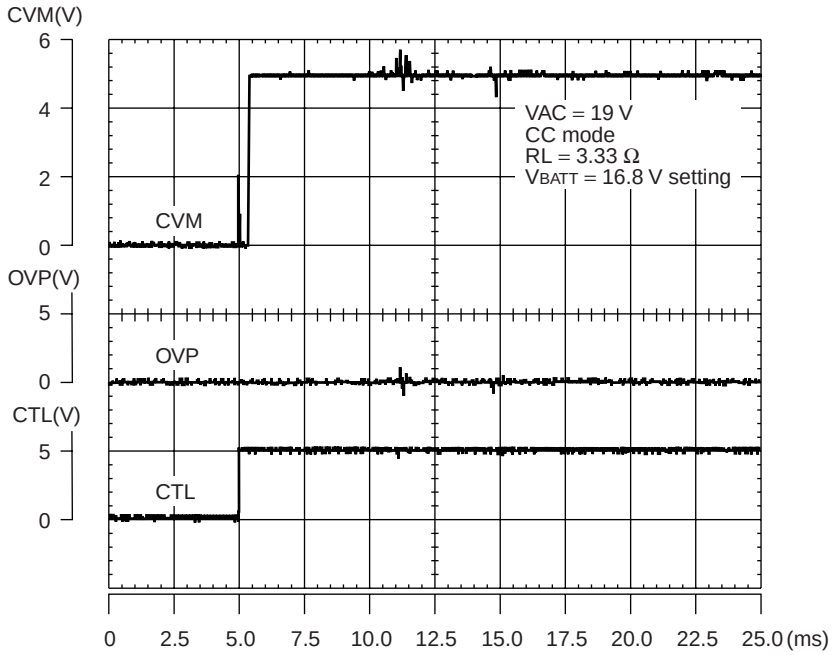
Soft-start Operating Waveform at Constant Current Mode (16.8 V setting) (1)



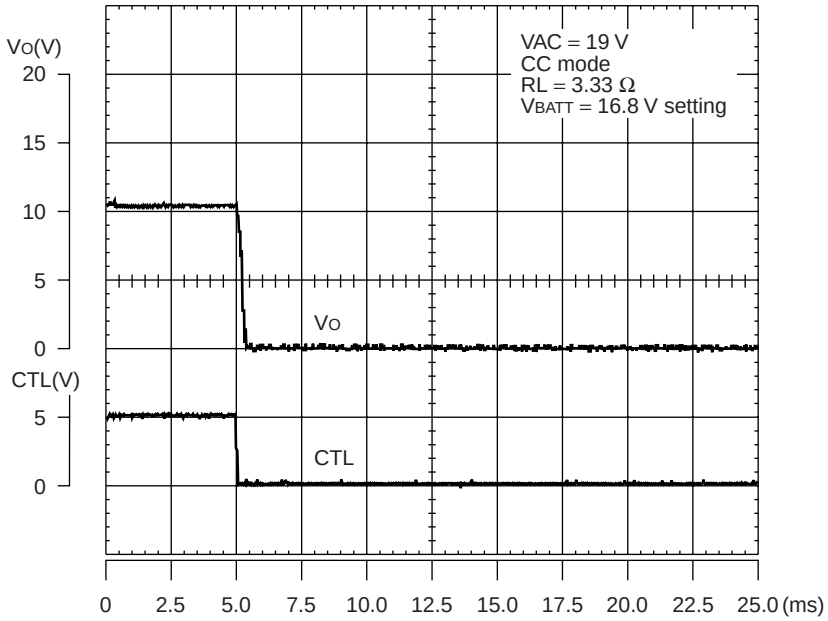
Soft-start Operating Waveform at Constant Current Mode (16.8 V setting) (2)



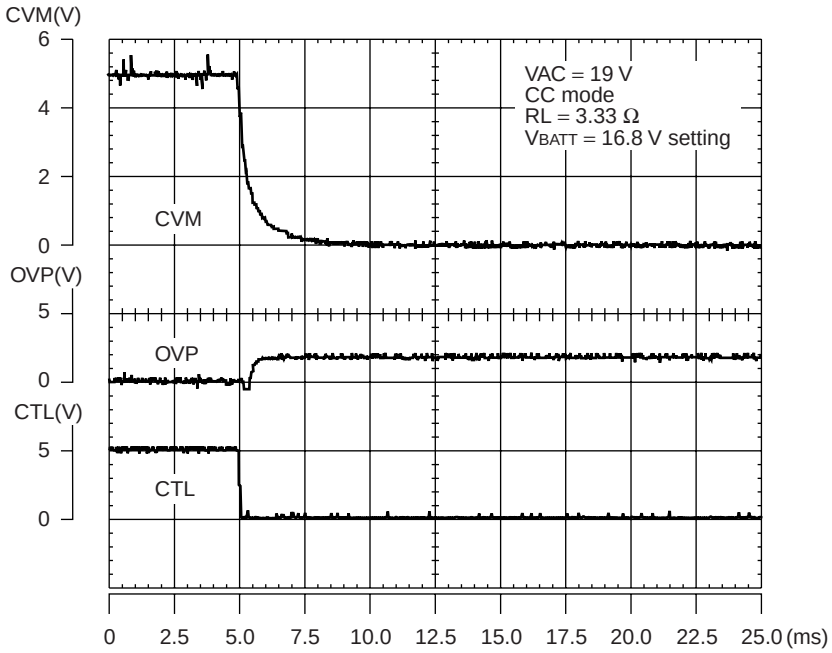
(Continued)

(Continued)

Discharge Operating Waveform at Constant Current Mode (16.8 V setting) (1)



Discharge Operating Waveform at Constant Current Mode (16.8 V setting) (2)



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools, and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage.
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

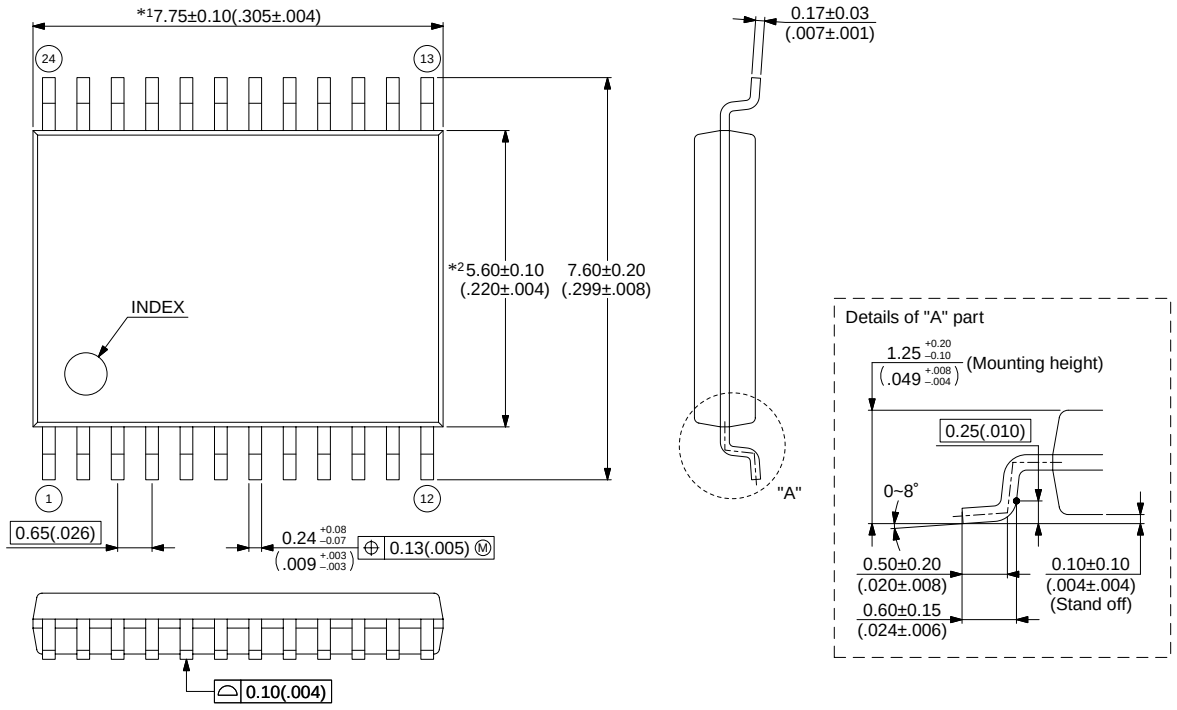
■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A113PFV	24-pin plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSION

24-pin plastic SSOP
(FPT-24P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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