

12-BIT, DUAL, ULTRALOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 2.7-V to 5.5-V Single Supply
- 12-Bit Linearity and Monotonicity
- Rail-to-Rail Voltage Output
- Settling Time: 5 μ s (Max)
- Ultralow Glitch Energy: 0.1 nVs
- Ultralow Crosstalk: -100 dB
- Low Power: 440 μ A (Max)
- Per-Channel Power Down: 2 μ A (Max)
- Power-On Reset to Midscale
- 2s Complement Input Data Format
- SPI-Compatible Serial Interface: Up to 50 MHz
- Daisy-Chain Capability
- Asynchronous Hardware Clear
- Simultaneous or Sequential Update
- Specified Temperature Range: -40°C to 105°C
- Small 3-mm \times 3-mm, 16-Lead QFN Package

APPLICATIONS

- Portable Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Industrial Process Control

DESCRIPTION

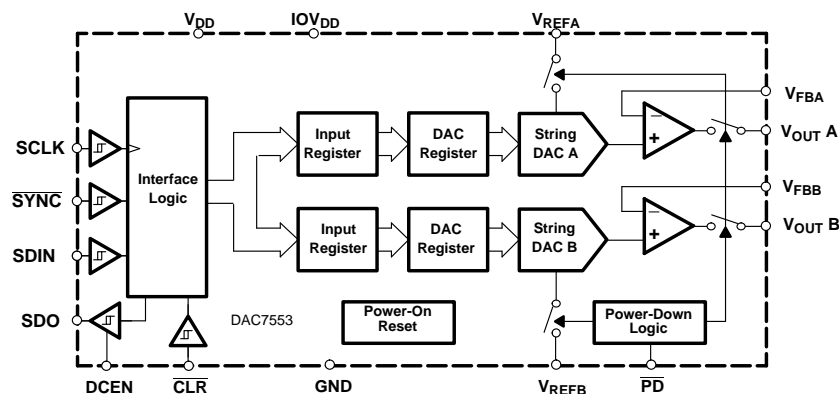
The DAC7553 is a 12-bit, dual-channel, voltage-output DAC with exceptional linearity and monotonicity. Its proprietary architecture minimizes undesired transients such as code-to-code glitch and channel-to-channel crosstalk. The low-power DAC7553 operates from a single 2.7-V to 5.5-V supply. The DAC7553 output amplifiers can drive a 2-k Ω , 200-pF load rail-to-rail with 5- μ s settling time; the output range is set using an external voltage reference.

The 3-wire serial interface operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire™, and DSP interface standards. The outputs of all DACs may be updated simultaneously or sequentially. The parts incorporate a power-on-reset circuit to ensure that the DAC outputs power up at midscale and remain there until a valid write cycle to the device takes place. The parts contain a power-down feature that reduces the current consumption of the device to under 2 μ A.

The small size and low-power operation makes the DAC7553 ideally suited for battery-operated portable applications. The power consumption is typically 1.5 mW at 5 V, 0.75 mW at 3 V, and reduces to 1 μ W in power-down mode.

The DAC7553 is available in a 16-lead QFN package and is specified over -40°C to 105°C .

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---------|---------|--------------------|-----------------------------|-----------------|-----------------|--------------------------|
| DAC7553 | 16 QFN | RGT | –40°C TO 105°C | D753 | DAC7553IRGTT | 250-piece Tape and Reel |
| | | | | | DAC7553IRGTR | 2500-piece Tape and Reel |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | UNIT |
|-----------------------------------|----------------------------|
| V_{DD} to GND | –0.3 V to 6 V |
| Digital input voltage to GND | –0.3 V to $V_{DD} + 0.3$ V |
| V_{out} to GND | –0.3 V to $V_{DD} + 0.3$ V |
| Operating temperature range | –40°C to 105°C |
| Storage temperature range | –65°C to 150°C |
| Junction temperature (T_J Max) | 150°C |

- (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = V_{DD}$, $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications -40°C to 105°C , unless otherwise specified

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|-----------------------|-------|-----------------------|---------------|
| STATIC PERFORMANCE ⁽¹⁾ | | | | | |
| Resolution | | | 12 | | Bits |
| Relative accuracy | | | ±0.35 | ±1 | LSB |
| Differential nonlinearity | Specified monotonic by design | | ±0.08 | ±0.5 | LSB |
| Offset error | | | | ±12 | mV |
| Zero-scale error | All zeroes loaded to DAC register | | | ±12 | mV |
| Gain error | | | | ±0.15 | %FSR |
| Full-scale error | | | | ±0.5 | %FSR |
| Zero-scale error drift | | | 7 | | μV/°C |
| Gain temperature coefficient | | | 3 | | ppm of FSR/°C |
| PSRR | V _{DD} = 5 V | | 0.75 | | mV/V |
| OUTPUT CHARACTERISTICS ⁽²⁾ | | | | | |
| Output voltage range | | 0 | | VREF | V |
| Output voltage settling time | R _L = 2 kΩ; 0 pF < C _L < 200 pF | | | 5 | μs |
| Slew rate | | | 1.8 | | V/μs |
| Capacitive load stability | R _L = ∞ | | 470 | | pF |
| | R _L = 2 kΩ | | 1000 | | |
| Digital-to-analog glitch impulse | 1 LSB change around major carry | | 0.1 | | nV-s |
| Channel-to-channel crosstalk | 1-kHz full-scale sine wave, outputs unloaded | | −100 | | dB |
| Digital feedthrough | | | 0.1 | | nV-s |
| Output noise density (10-kHz offset frequency) | | | 120 | | nV/rtHz |
| Total harmonic distortion | F _{OUT} = 1 kHz, F _S = 1 MSPS, BW = 20 kHz | | −85 | | dB |
| DC output impedance | | | 1 | | Ω |
| Short-circuit current | V _{DD} = 5 V | | 50 | | mA |
| | V _{DD} = 3 V | | 20 | | |
| Power-up time | Coming out of power-down mode, V _{DD} = 5 V | | 15 | | μs |
| | Coming out of power-down mode, V _{DD} = 3 V | | 15 | | |
| REFERENCE INPUT | | | | | |
| VREF Input range | | 0 | | V _{DD} | V |
| Reference input impedance | V _{REF} A and V _{REF} B shorted together | | 50 | | kΩ |
| Reference current | V _{REF} A = V _{REF} B = V _{DD} = 5 V, V _{REF} A and V _{REF} B shorted together | | 100 | 250 | μA |
| | V _{REF} A = V _{REF} B = V _{DD} = 3 V, V _{REF} A and V _{REF} B shorted together | | 60 | 123 | |
| LOGIC INPUTS ⁽²⁾ | | | | | |
| Input current | | | | ±1 | μA |
| V _{IN_L} , Input low voltage | IOV _{DD} ≥ 2.7 V | | | 0.3 IOV _{DD} | V |
| V _{IN_H} , Input high voltage | IOV _{DD} ≥ 2.7 V | 0.7 IOV _{DD} | | | V |
| Pin capacitance | | | | 3 | pF |

(1) Linearity tested using a reduced code range of 30 to 4065; output unloaded.

(2) Specified by design and characterization, not production tested. For $1.8\text{ V} < IOV_{DD} < 2.7\text{ V}$, It is recommended that $V_{IH} = IOV_{DD}$, $V_{IL} = \text{GND}$.

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = V_{DD}$, $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications -40°C to 105°C , unless otherwise specified

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|-----|------|-----|-------|
| POWER REQUIREMENTS | | | | | |
| V _{DD} , IOV _{DD} ⁽³⁾ | | 2.7 | | 5.5 | V |
| I _{DD} (normal operation) | DAC active and excluding load current | | | | |
| V _{DD} = 3.6 V to 5.5 V | V _{IH} = IOV _{DD} and V _{IL} = GND | | 300 | 440 | μA |
| V _{DD} = 2.7 V to 3.6 V | | | 250 | 400 | |
| I _{DD} (all power-down modes) | V _{IH} = IOV _{DD} and V _{IL} = GND | | | | |
| V _{DD} = 3.6 V to 5.5 V | | | 0.2 | 2 | μA |
| V _{DD} = 2.7 V to 3.6 V | | | 0.05 | 2 | |
| POWER EFFICIENCY | | | | | |
| I _{OUT} /I _{DD} | I _{LOAD} = 2 mA, V _{DD} = 5 V | | 93% | | |

(3) IOV_{DD} operates down to 1.8 V with slightly degraded timing, as long as $V_{IH} = IOV_{DD}$ and $V_{IL} = \text{GND}$.

TIMING CHARACTERISTICS⁽¹⁾⁽²⁾

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND; all specifications $-40^\circ\text{C to }105^\circ\text{C}$, unless otherwise specified

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|-----|-----|-----|-------|
| $t_1^{(3)}$ SCLK cycle time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 20 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 20 | | | |
| t_2 SCLK HIGH time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 10 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 10 | | | |
| t_3 SCLK LOW time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 10 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 10 | | | |
| t_4 $\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 4 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 4 | | | |
| t_5 Data setup time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 5 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 5 | | | |
| t_6 Data hold time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 4.5 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 4.5 | | | |
| t_7 SCLK falling edge to $\overline{\text{SYNC}}$ rising edge | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 0 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 0 | | | |
| t_8 Minimum $\overline{\text{SYNC}}$ HIGH time | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 20 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 20 | | | |
| t_9 SCLK falling edge to SDO valid | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 10 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 10 | | | |
| t_{10} $\overline{\text{CLR}}$ pulse width low | $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 10 | | | ns |
| | $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ | 10 | | | |

(1) All input signals are specified with $t_R = t_F = 1\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

(2) See Serial Write Operation timing diagram [Figure 1](#).

(3) Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7\text{ V to }5.5\text{ V}$.

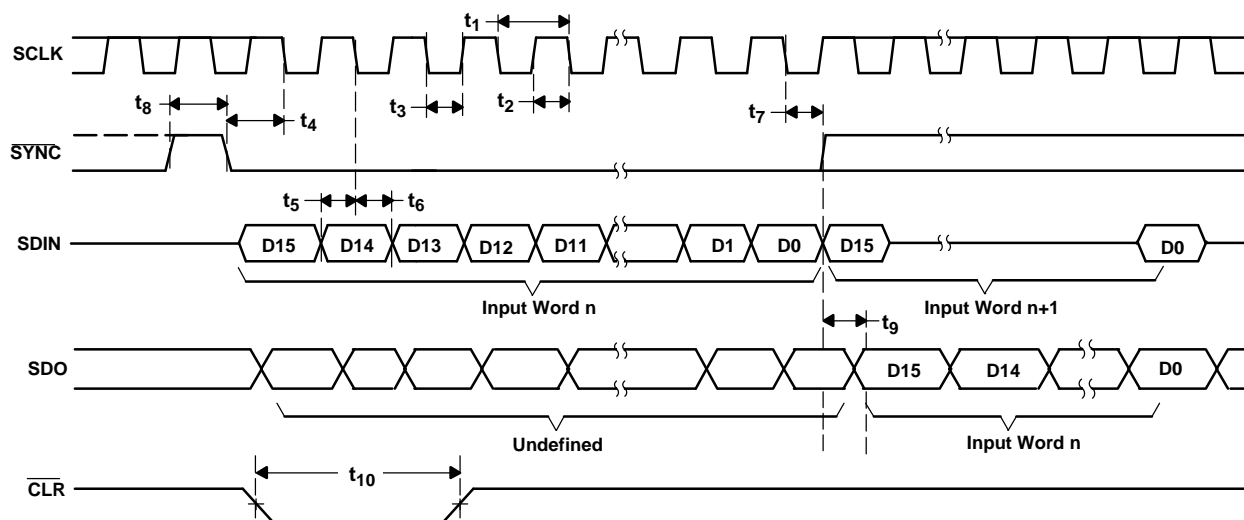
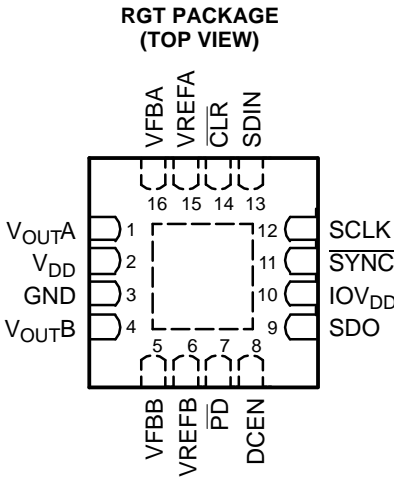


Figure 1. Serial Write Operation

PIN DESCRIPTION



Terminal Functions

| TERMINAL | | DESCRIPTION |
|----------|-------------------|--|
| NO. | NAME | |
| 1 | VOUTA | Analog output voltage from DAC A |
| 2 | VDD | Analog voltage supply input |
| 3 | GND | Ground |
| 4 | VOUTB | Analog output voltage from DAC B |
| 5 | VFBB | DAC B amplifier sense input. |
| 6 | VREFB | Positive reference voltage input for DAC B |
| 7 | \overline{PD} | Power down |
| 8 | DCEN | Daisy-chain enable |
| 9 | SDO | Serial data output |
| 10 | IOVDD | I/O voltage supply input |
| 11 | \overline{SYNC} | Frame synchronization input. The falling edge of the \overline{SYNC} pulse indicates the start of a serial data frame shifted out to the DAC7553 |
| 12 | SCLK | Serial clock input |
| 13 | SDIN | Serial data input |
| 14 | \overline{CLR} | Asynchronous input to clear the DAC registers. When \overline{CLR} is low, the DAC registers are set to 000H and the output to midscale voltage. |
| 15 | VREFA | Positive reference voltage input for DAC A |
| 16 | VFBA | DAC A amplifier sense input. |

TYPICAL CHARACTERISTICS

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

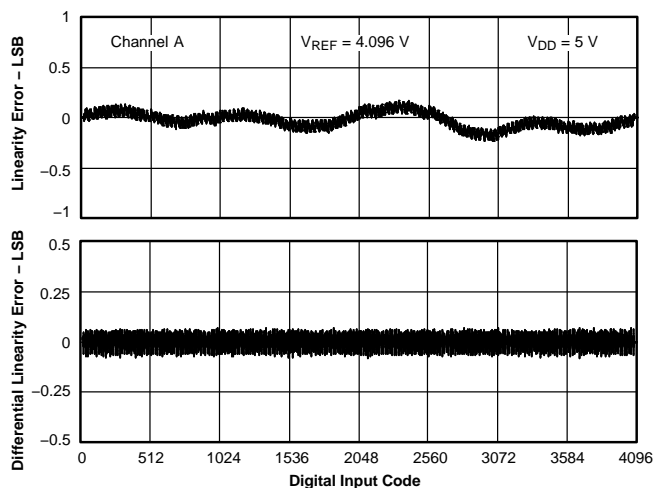


Figure 2.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

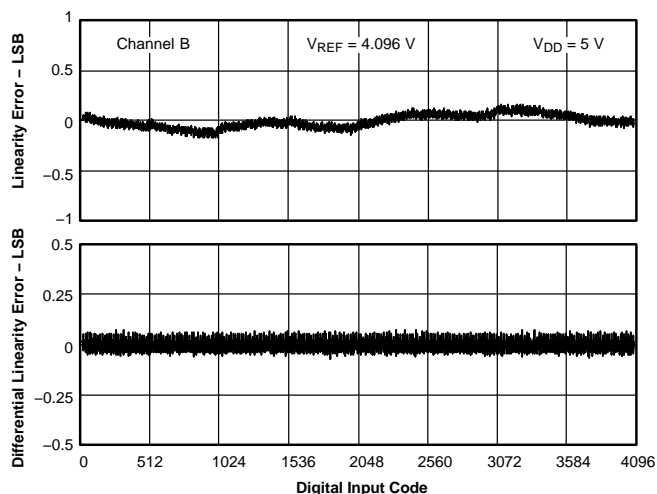


Figure 3.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

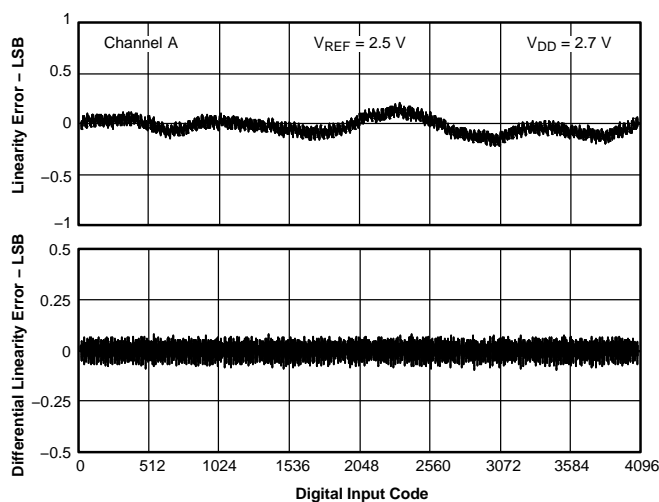


Figure 4.

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
VS
DIGITAL INPUT CODE

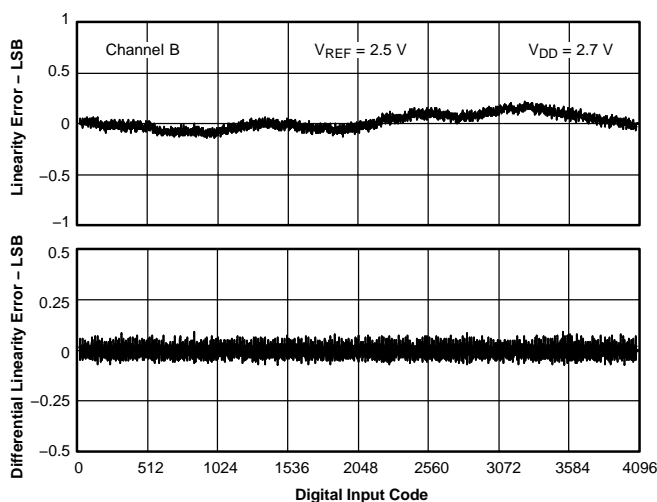


Figure 5.

TYPICAL CHARACTERISTICS (continued)

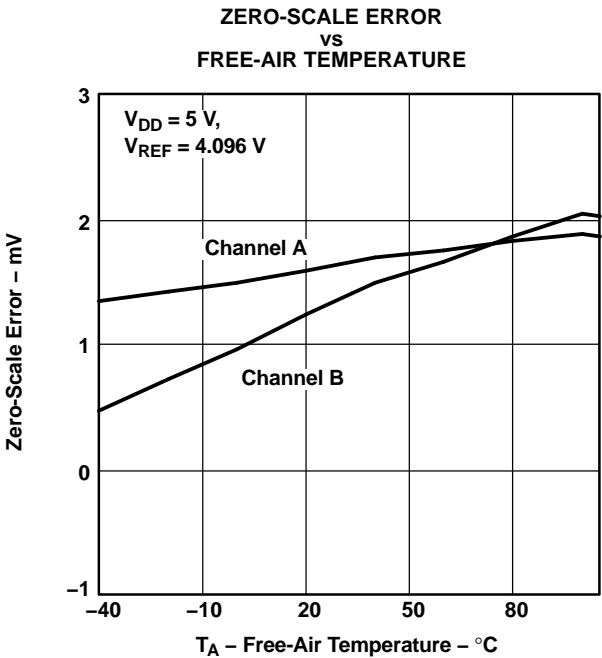


Figure 6.

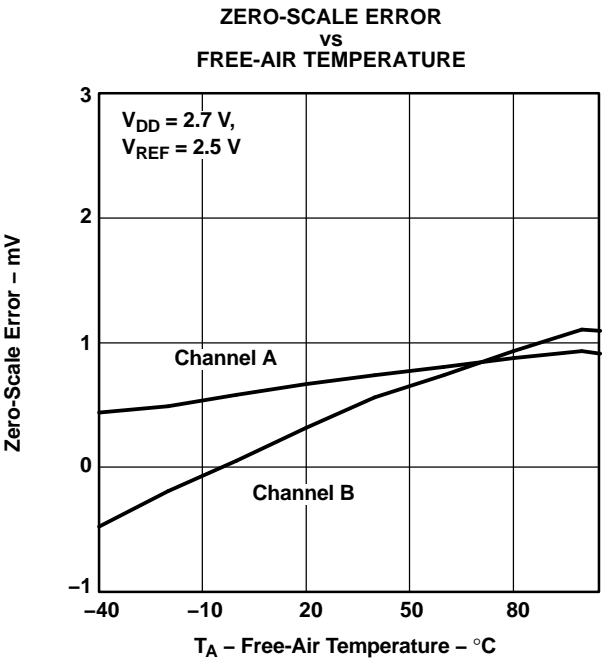


Figure 7.

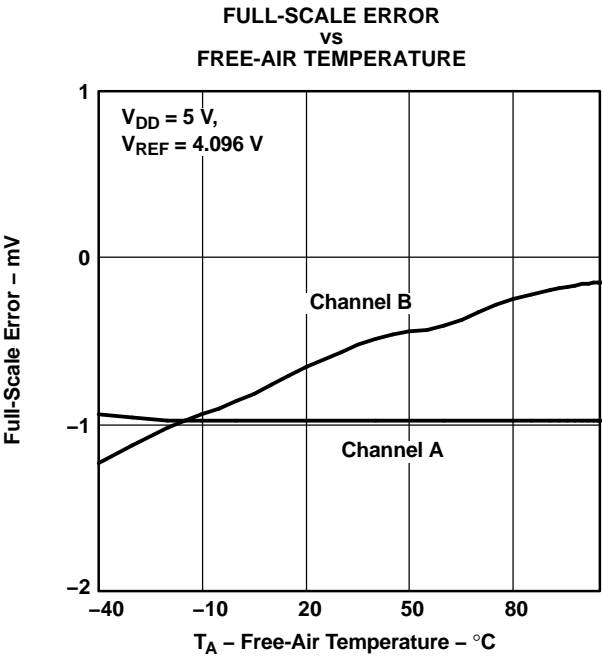


Figure 8.

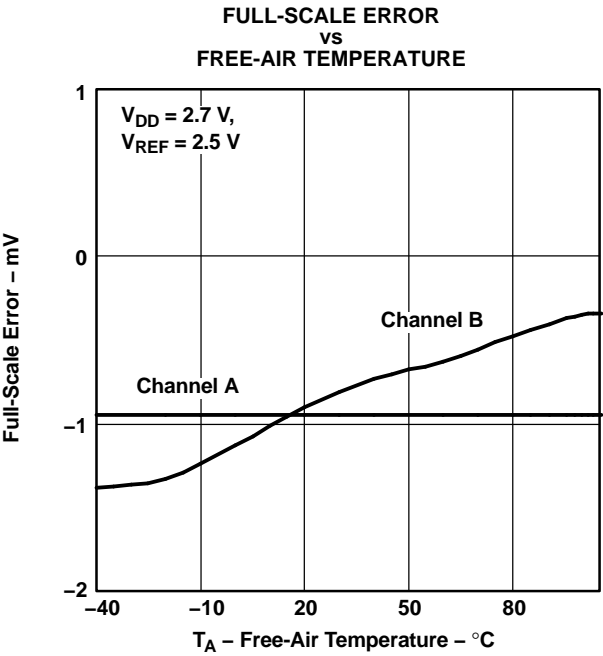


Figure 9.

TYPICAL CHARACTERISTICS (continued)

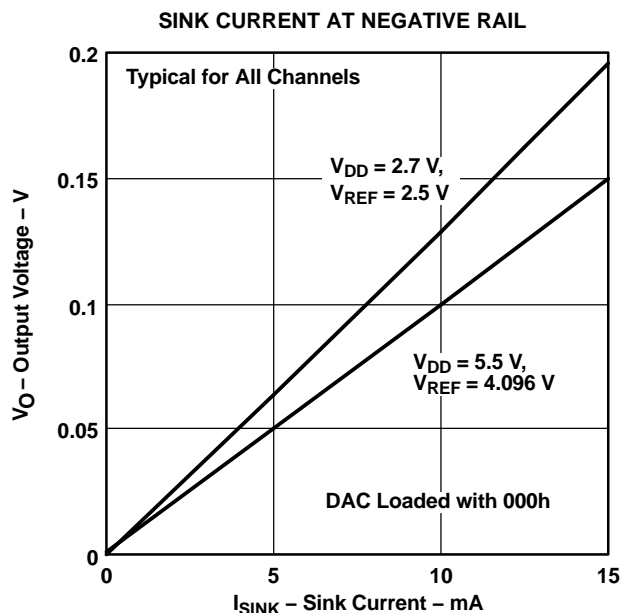


Figure 10.

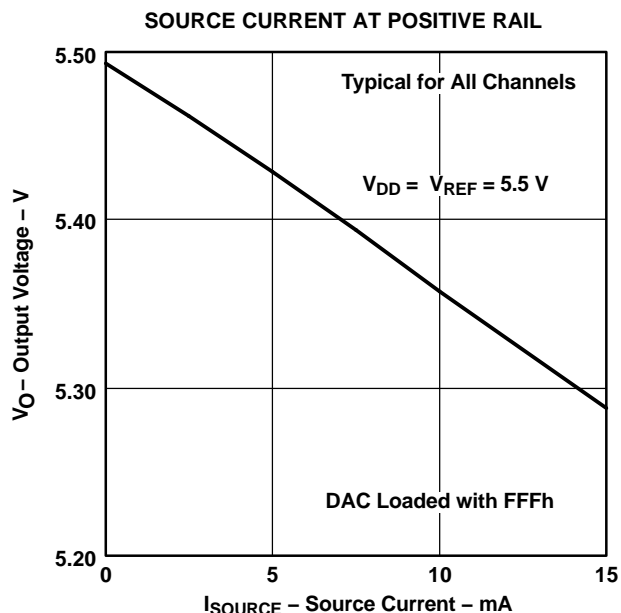


Figure 11.

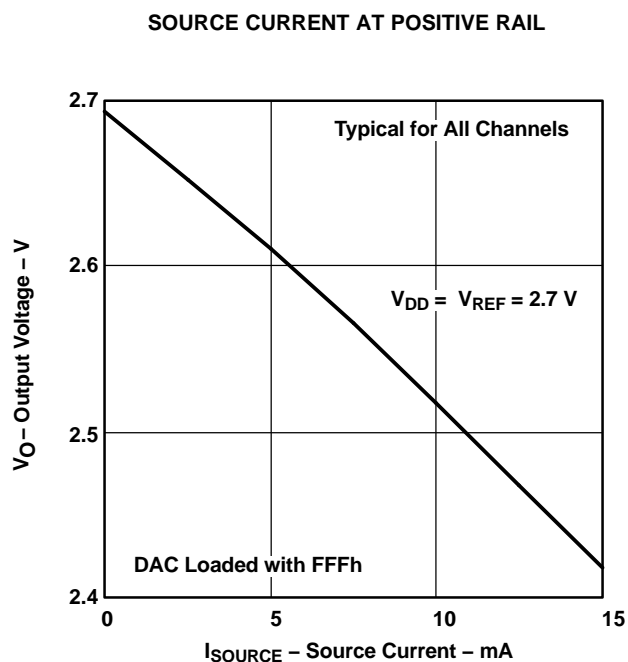


Figure 12.

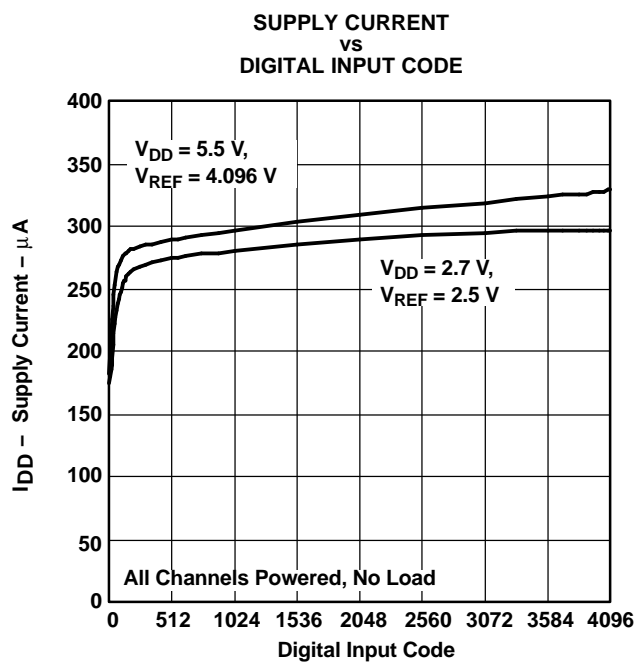


Figure 13.

TYPICAL CHARACTERISTICS (continued)

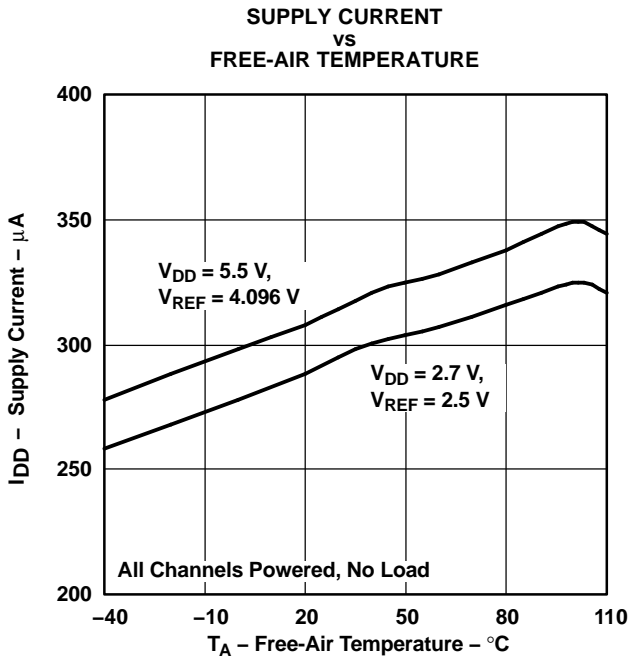


Figure 14.

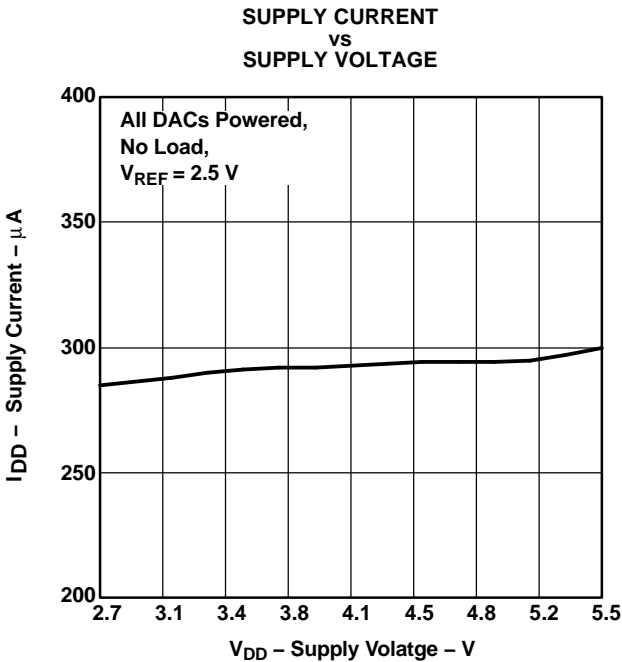


Figure 15.

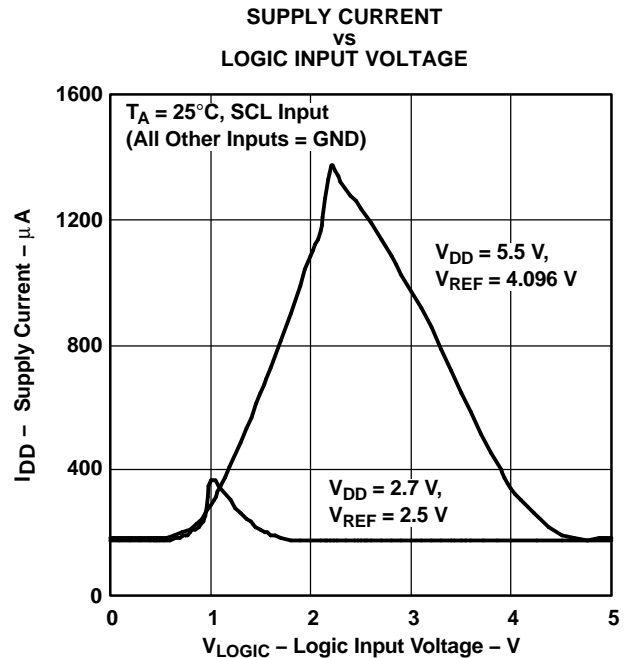


Figure 16.

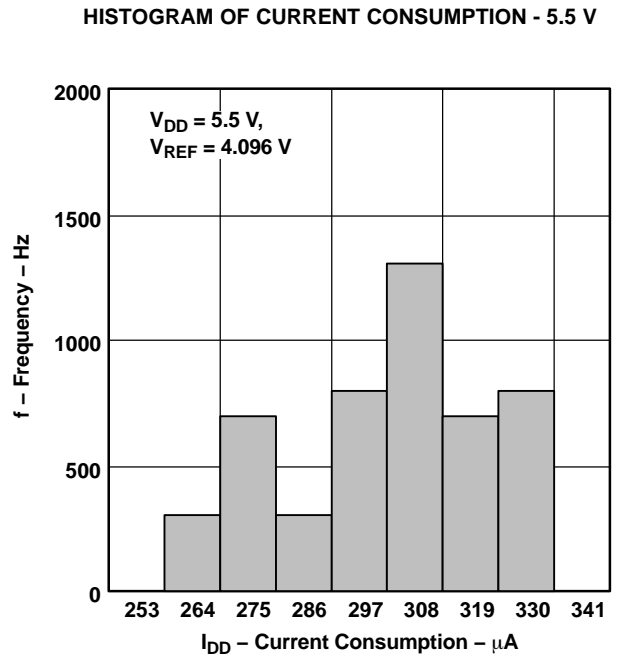


Figure 17.

TYPICAL CHARACTERISTICS (continued)

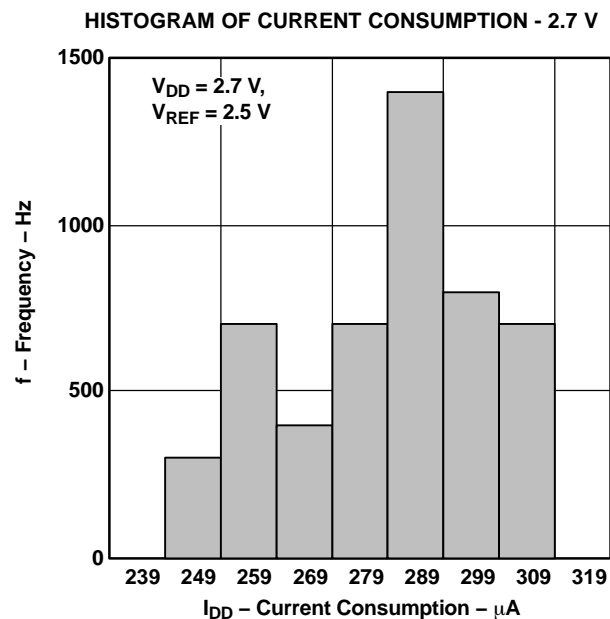


Figure 18.

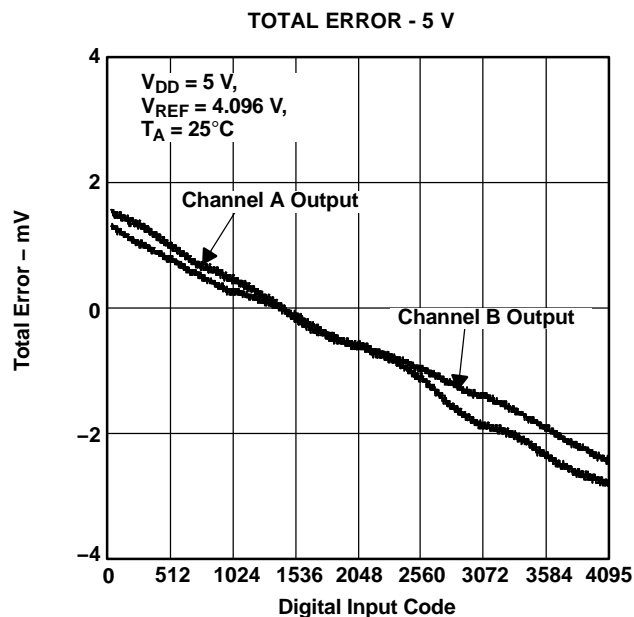


Figure 19.

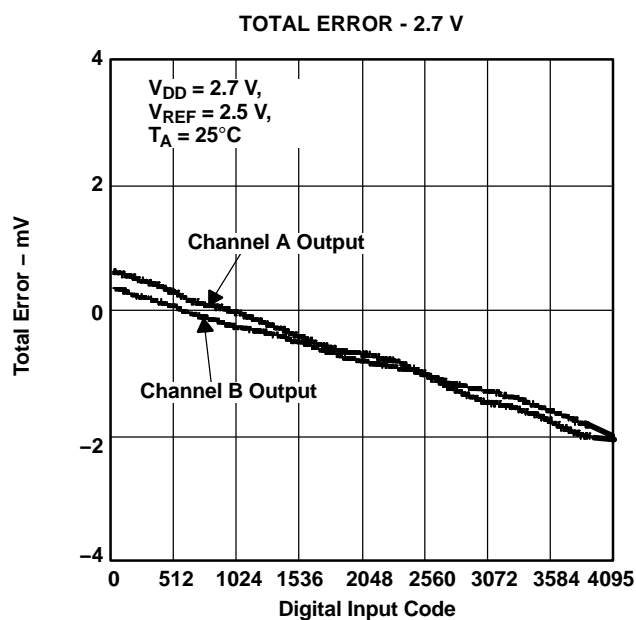


Figure 20.

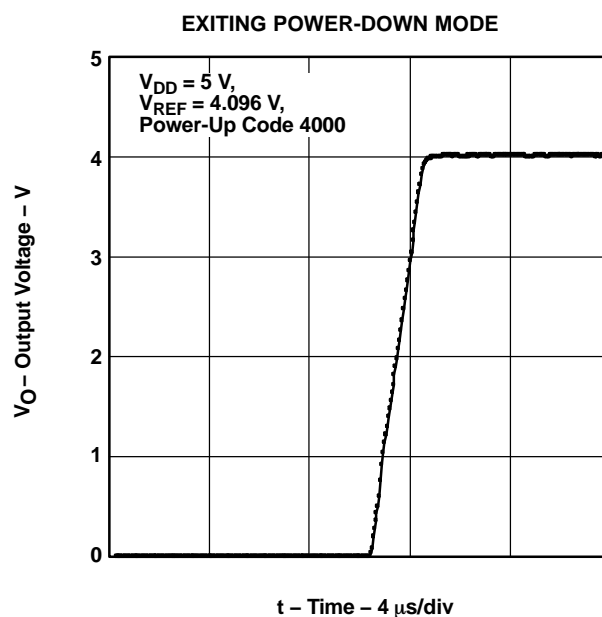


Figure 21.

TYPICAL CHARACTERISTICS (continued)

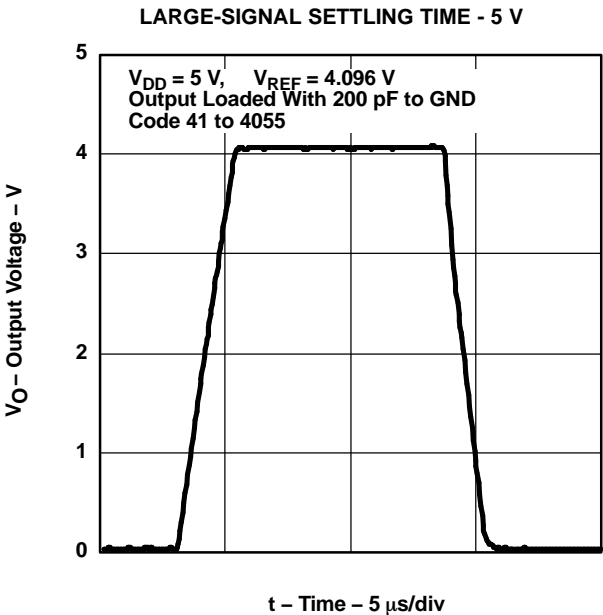


Figure 22.

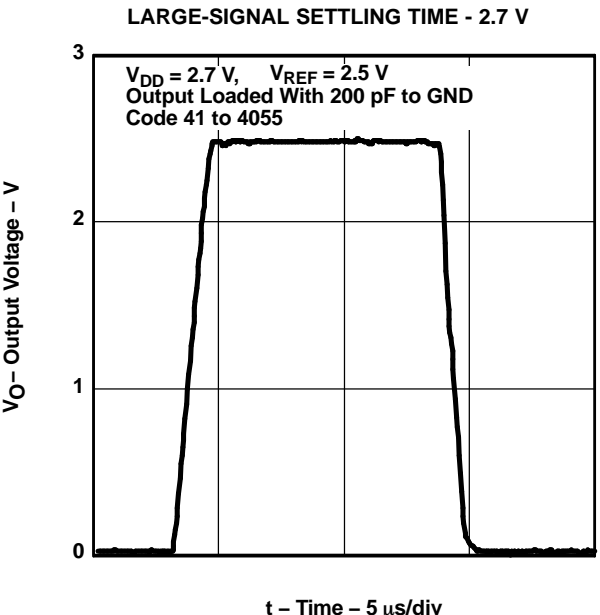


Figure 23.

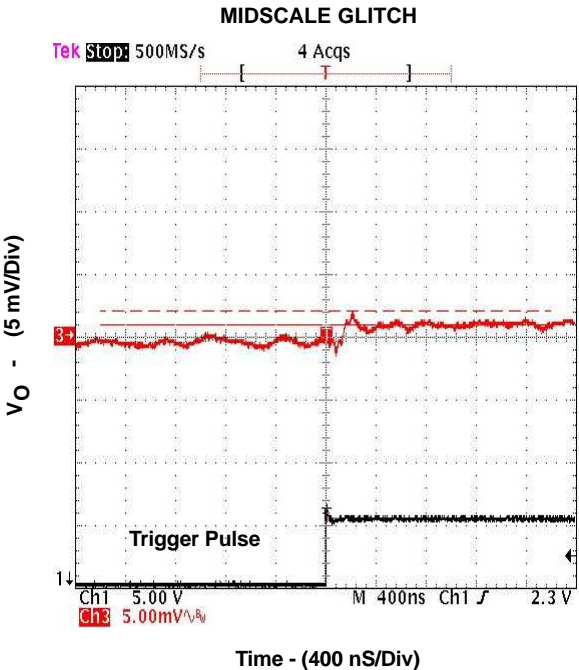


Figure 24.

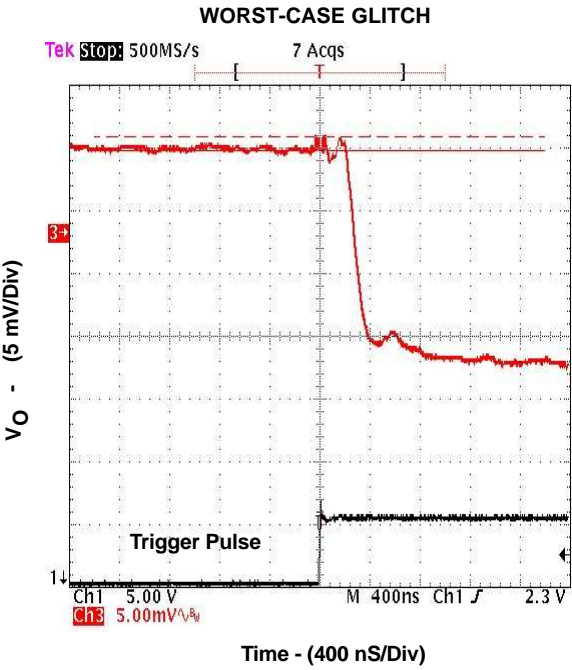


Figure 25.

TYPICAL CHARACTERISTICS (continued)

DIGITAL FEEDTHROUGH ERROR

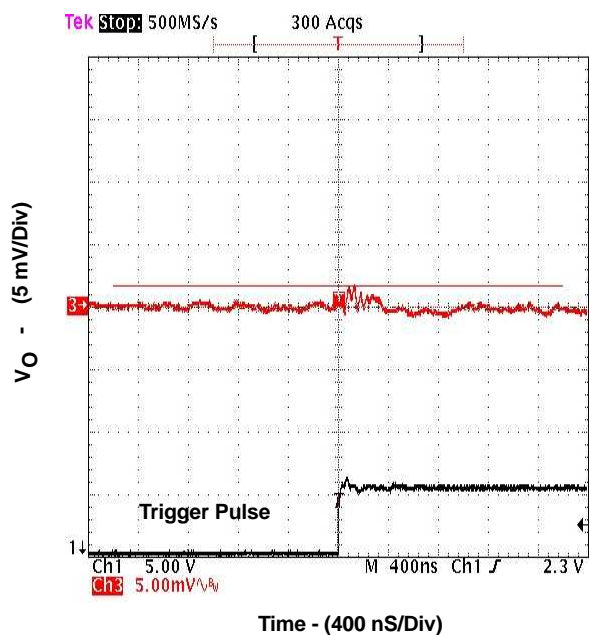


Figure 26.

CHANNEL-TO-CHANNEL CROSSTALK
FOR A FULL-SCALE SWING

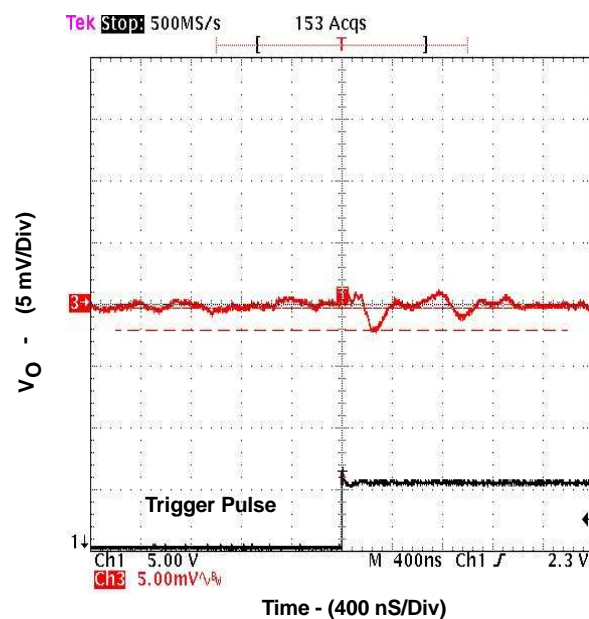


Figure 27.

TOTAL HARMONIC DISTORTION
VS
OUTPUT FREQUENCY

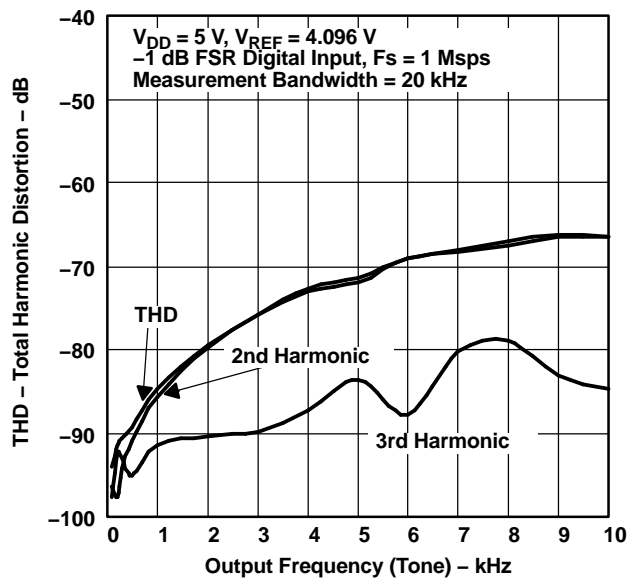


Figure 28.

TYPICAL CHARACTERISTICS (continued)**3-Wire Serial Interface**

The DAC7553 digital interface is a standard 3-wire SPI/QSPI/Microwire/DSP-compatible interface.

Table 1. Serial Interface Programming

| CONTROL | | | | DATA BITS | DAC(s) | FUNCTION |
|---------|------|------|------|-----------|--------|--|
| DB15 | DB14 | DB13 | DB12 | DB11-DB10 | | |
| 0 | 0 | 0 | 0 | data | A | Single Channel Store. The TMP register of channel A is updated. |
| 0 | 0 | 1 | 0 | data | B | Single Channel Store. The TMP register of channel B is updated. |
| 0 | 1 | 0 | 0 | data | A | Single Channel Update. The TMP and DAC registers of channel A are updated. |
| 0 | 1 | 1 | 0 | data | B | Single Channel Update. The TMP and DAC registers of channel A are updated and the DAC register of channel B is updated with input register data. |
| 1 | 0 | 0 | 0 | data | A | Single Channel Update. The TMP and DAC registers of channel B are updated. |
| 1 | 0 | 1 | 0 | data | B | Single Channel Update. The TMP and DAC registers of channel B are updated and the DAC register of channel A is updated with input register data. |
| 1 | 1 | 0 | 0 | data | A–B | All Channel Update. The TMP and DAC registers of channels A and B are updated. |
| 1 | 1 | 1 | 0 | data | A–B | All Channel DAC Update. The DAC register of channels A and B are updated with input register data. |

POWER-DOWN MODE

In power-down mode, the DAC outputs are programmed to one of three output impedances, 1 k Ω , 100 k Ω , or floating.

Table 2. Power-Down Mode Control

| EXTENDED CONTROL | | | | DATA BITS | | | FUNCTION |
|------------------|------|------|------|-----------|------|---------|---|
| DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9-DB0 | |
| 0 | 0 | X | 1 | 0 | 0 | X | PWD Hi-Z (all channels) |
| 0 | 0 | X | 1 | 0 | 1 | X | PWD 1 k Ω (all channels) |
| 0 | 0 | X | 1 | 1 | 0 | X | PWD 100 k Ω (all channels) |
| 0 | 0 | X | 1 | 1 | 1 | X | PWD Hi-Z (all channels) |
| 0 | 1 | X | 1 | 0 | 0 | X | PWD Hi-Z (selected channel = A) |
| 0 | 1 | X | 1 | 0 | 1 | X | PWD 1 k Ω (selected channel = A) |
| 0 | 1 | X | 1 | 1 | 0 | X | PWD 100 k Ω (selected channel = A) |
| 0 | 1 | X | 1 | 1 | 1 | X | PWD Hi-Z (selected channel = A) |
| 1 | 0 | X | 1 | 0 | 0 | X | PWD Hi-Z (selected channel = B) |
| 1 | 0 | X | 1 | 0 | 1 | X | PWD 1 k Ω (selected channel = B) |
| 1 | 0 | X | 1 | 1 | 0 | X | PWD 100 k Ω (selected channel = B) |
| 1 | 0 | X | 1 | 1 | 1 | X | PWD Hi-Z (selected channel = B) |
| 1 | 1 | X | 1 | 0 | 0 | X | PWD Hi-Z (all channels) |
| 1 | 1 | X | 1 | 0 | 1 | X | PWD 1 k Ω (all channels) |
| 1 | 1 | X | 1 | 1 | 0 | X | PWD 100 k Ω (all channels) |
| 1 | 1 | X | 1 | 1 | 1 | X | PWD Hi-Z (all channels) |

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC7553 consists of a string DAC followed by an output buffer amplifier. Figure 29 shows a generalized block diagram of the DAC architecture.

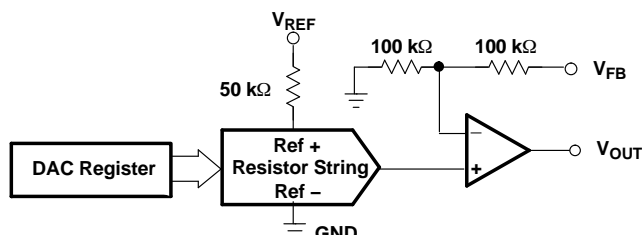


Figure 29. Typical DAC Architecture

The 2s-complement input coding to the DAC7553 gives the ideal output voltage as:

$$V_{OUT} = V_{REF} \times D/4096$$

Where D = decimal equivalent of the 2s-complement input that is loaded to the DAC register, which can range from 0 to 4095.

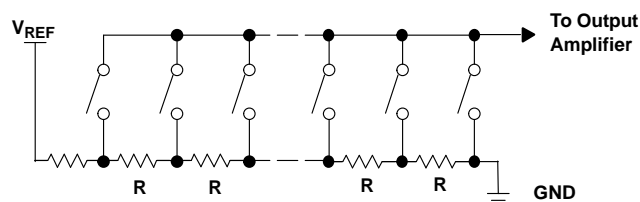


Figure 30. Typical Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 30. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is specified monotonic. The DAC7553 architecture uses four separate resistor strings to minimize channel-to-channel crosstalk.

OUTPUT BUFFER AMPLIFIERS

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD} . It is capable of driving a load of 2 kΩ in parallel with up to 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1.8 V/μs with a typical settling time of 3 μs with the output unloaded.

DAC External Reference Input

Two separate reference pins are provided for two DACs, providing maximum flexibility. VREFA serves DAC A and VREFB serves DAC B. VREFA and VREFB can be externally shorted together for simplicity.

It is recommended to use a buffered reference in the external circuit (e.g., REF3140). The input impedance is typically 100 kΩ for each reference input pin.

Amplifier Sense Input

The DAC7553 contains two amplifier feedback input pins, VFBA and VFBB. For voltage output operation, VFBA and VFBB must externally connect to VOUTA and VOUTB, respectively. For better DC accuracy, these connections should be made at load points. The VFBA and VFBB pins are also useful for a variety of applications, including digitally controlled current sources. Each feedback input pin is internally connected to the DAC amplifier's negative input terminal through a 100-kΩ resistor; and, the amplifier's negative input terminal internally connects to ground through another 100-kΩ resistor (See Figure 29). This forms a gain-of-two, noninverting amplifier configuration. Overall gain remains one because the resistor string has a divide-by-two configuration. The resistance seen at each VFBB pin is approximately 200 kΩ to ground.

Power-On Reset

On power up, all internal registers are cleared and all channels are updated with midscale voltages. Until valid data is written, all DAC outputs remain in this state. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up. In order not to turn on ESD protection devices, V_{DD} should be applied before any other pin is brought high.

Power Down

The DAC7553 has a flexible power-down capability as described in Table 2. Individual channels could be powered down separately or all channels could be powered down simultaneously. During a power-down condition, the user has flexibility to select the output impedance of each channel. During power-down operation, each channel can have either 1-k Ω , 100-k Ω , or Hi-Z output impedance to ground.

Asynchronous Clear

The DAC7553 output is asynchronously set to midscale voltage immediately after the $\overline{\text{CLR}}$ pin is brought low. The $\overline{\text{CLR}}$ signal resets all internal registers and therefore behaves like the Power-On Reset. The DAC7553 updates at the first rising edge of the $\overline{\text{SYNC}}$ signal that occurs after the $\overline{\text{CLR}}$ pin is brought back to high.

IOVDD and Level Shifters

The DAC7553 can be used with different logic families that require a wide range of supply voltages (from 1.8 V to 5.5 V). To enable this useful feature, the IOVDD pin must be connected to the logic supply voltage of the system. All DAC7553 digital input and output pins are equipped with level-shifter circuits. Level shifters at the input pins ensure that external logic high voltages are translated to the internal logic high voltage, with no additional power dissipation. Similarly, the level shifter for the SDO pin translates the internal logic high voltage (VDD) to the external logic high level (IOVDD). For single-supply operation, the IOVDD pin can be tied to the VDD pin.

SERIAL INTERFACE

The DAC7553 is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

In daisy-chain mode (DCEN = 1) the DAC7553 requires a falling SCLK edge after the rising $\overline{\text{SYNC}}$, in order to initialize the serial interface for the next update.

16-Bit Word and Input Shift Register

The input shift register is 16 bits wide. DAC data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK, as shown in the Figure 1 timing diagram. The 16-bit word, illustrated in Table 1, consists of four control bits followed by 12 bits of DAC data. The 12-bit data is in 2s-complement format, with 800H corresponding to 0-V output and 7FFH corresponding to full-scale output ($V_{\text{REF}} - 1$ LSB). Data is loaded MSB first (Bit 15) where the first two bits (DB15 and DB14) determine if the input register, DAC register, or both are updated with shift

register input data. Bit 13 (DB13) determines whether the data is for DAC A, DAC B, or both DACs. Bit 12 (DB12) determines either normal mode or power-down mode (see Table 2). All channels are updated when bits 15 and 14 (DB15 and DB14) are high.

The $\overline{\text{SYNC}}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low, observing the minimum $\overline{\text{SYNC}}$ to SCLK falling edge setup time, t_4 . After $\overline{\text{SYNC}}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses.

When DCEN is low, the SDO pin is brought to a Hi-Z state. The first 16 data bits that follow the falling edge of $\overline{\text{SYNC}}$ are stored in the shift register. The rising edge of $\overline{\text{SYNC}}$ that follows the 16th data bit updates the DAC(s). If $\overline{\text{SYNC}}$ is brought high before the 16th data bit, no action occurs.

When DCEN is high, data can continuously be shifted into the shift register, enabling the daisy-chain operation. The SDO pin becomes active and outputs SDIN data with 16 clock cycle delay. A rising edge of $\overline{\text{SYNC}}$ loads the shift register data into the DAC(s). The loaded data consists of the last 16 data bits received into the shift register before the rising edge of $\overline{\text{SYNC}}$.

If daisy-chain operation is not needed, DCEN should permanently be tied to a logic low voltage.

Daisy-Chain Operation

When DCEN pin is brought high, daisy chaining is enabled. The Serial Data Output (SDO) pin is provided to daisy-chain multiple DAC7553 devices in a system.

As long as $\overline{\text{SYNC}}$ is high or DCEN is low, the SDO pin is in a high-impedance state. When $\overline{\text{SYNC}}$ is brought low, the output of the internal shift register is tied to the SDO pin. As long as $\overline{\text{SYNC}}$ is low and DCEN is high, SDO duplicates the SDIN signal with a 16-cycle delay. To support multiple devices in a daisy chain, SCLK and $\overline{\text{SYNC}}$ signals are shared across all devices, and SDO of one DAC7553 should be tied to the SDIN of the next DAC7553. For n devices in such a daisy chain, $16n$ SCLK cycles are required to shift the entire input data stream. After $16n$ SCLK falling edges are received, following a falling $\overline{\text{SYNC}}$, the data stream becomes complete and $\overline{\text{SYNC}}$ can be brought high to update n devices simultaneously. SDO operation is specified at a maximum SCLK speed of 10 MHz.

INTEGRAL AND DIFFERENTIAL LINEARITY

The DAC7553 uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within (+/-) 0.35 LSBs, and differential linearity error is typically within (+/-) 0.08 LSBs.

GLITCH ENERGY

The DAC7553 uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low, they are usually buried within the wide-band noise and cannot be easily detected. The DAC7553 glitch is typically well under 0.1 nV-s. Such low glitch energy provides more than 10X improvement over industry alternatives.

CHANNEL-TO-CHANNEL CROSSTALK

The DAC7553 architecture is designed to minimize channel-to-channel crosstalk. The voltage change in one channel does not affect the voltage output in another channel. The DC crosstalk is in the order of a few microvolts. AC crosstalk is also less than -100 dBs. This provides orders of magnitude improvement over certain competing architectures.

APPLICATION INFORMATION

Waveform Generation

Due to its exceptional linearity, low glitch, and low crosstalk, the DAC7553 is well suited for waveform generation (from DC to 10 kHz). The DAC7553 large-signal settling time is 5 µs, supporting an update rate of 200 KSPS. However, the update rates can exceed 1 MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, REF3140 (4.096 V) or REF02 (5 V) are recommended for reference voltage generation.

Generating ±5-V, ±10-V, and ± 12-V Outputs For Precision Industrial Control

Industrial control applications can require multiple feedback loops consisting of sensors, ADCs, MCUs, DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

Loop Accuracy:

In a control loop, the ADC has to be accurate. Offset, gain, and the integral linearity errors of the DAC are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find it and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental

change the loop can generate. A DNL error less than -1 LSB (non-monotonicity) can create loop instability. A DNL error greater than +1 LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop loses its stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ± 0.08 LSB typical DNL error, 755X DACs are great choices for precision control loops.

Loop Speed:

Many factors determine control loop speed. Typically, the conversion time of the ADC and the computation time of the MCU are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop down only during the start-up. Once the loop reaches its steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop's transfer function, DAC glitches can also slow the loop down. With its 1 MSPS (small-signal) maximum data update rate, DAC7553 can support high-speed control loops. Ultralow glitch energy of the DAC7553 significantly improves loop stability and loop settling time.

Generating Industrial Voltage Ranges:

For control loop applications, DAC gain and offset errors are not important parameters. This could be exploited to lower trim and calibration costs in a high-voltage control circuit design. Using an operational amplifier (OPA130), and a voltage reference (REF3140), the DAC7553 can generate the wide voltage swings required by the control loop.

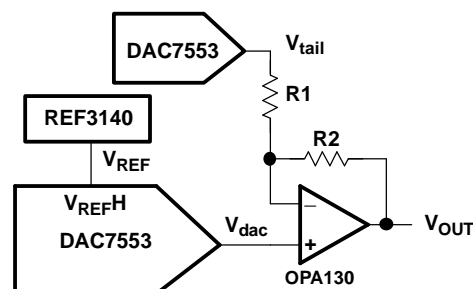


Figure 31. Low-cost, Wide-swing Voltage Generator for Control Loop Applications

The output voltage of the configuration is given by:

$$V_{out} = V_{REF} \left(\frac{R2}{R1} + 1 \right) \frac{Din}{4096} - V_{tail} \frac{R2}{R1} \quad (1)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. Once R2 and R1 set the gain to include some minimal over-range, a DAC7553 channel could be used to set the required offset voltage. Residual

errors are not an issue for loop accuracy because offset and gain errors could be tolerated. One DAC7553 channel can provide the V_{tail} voltage, while the other DAC7553 channel can provide V_{dac} voltage to help generate the high-voltage outputs.

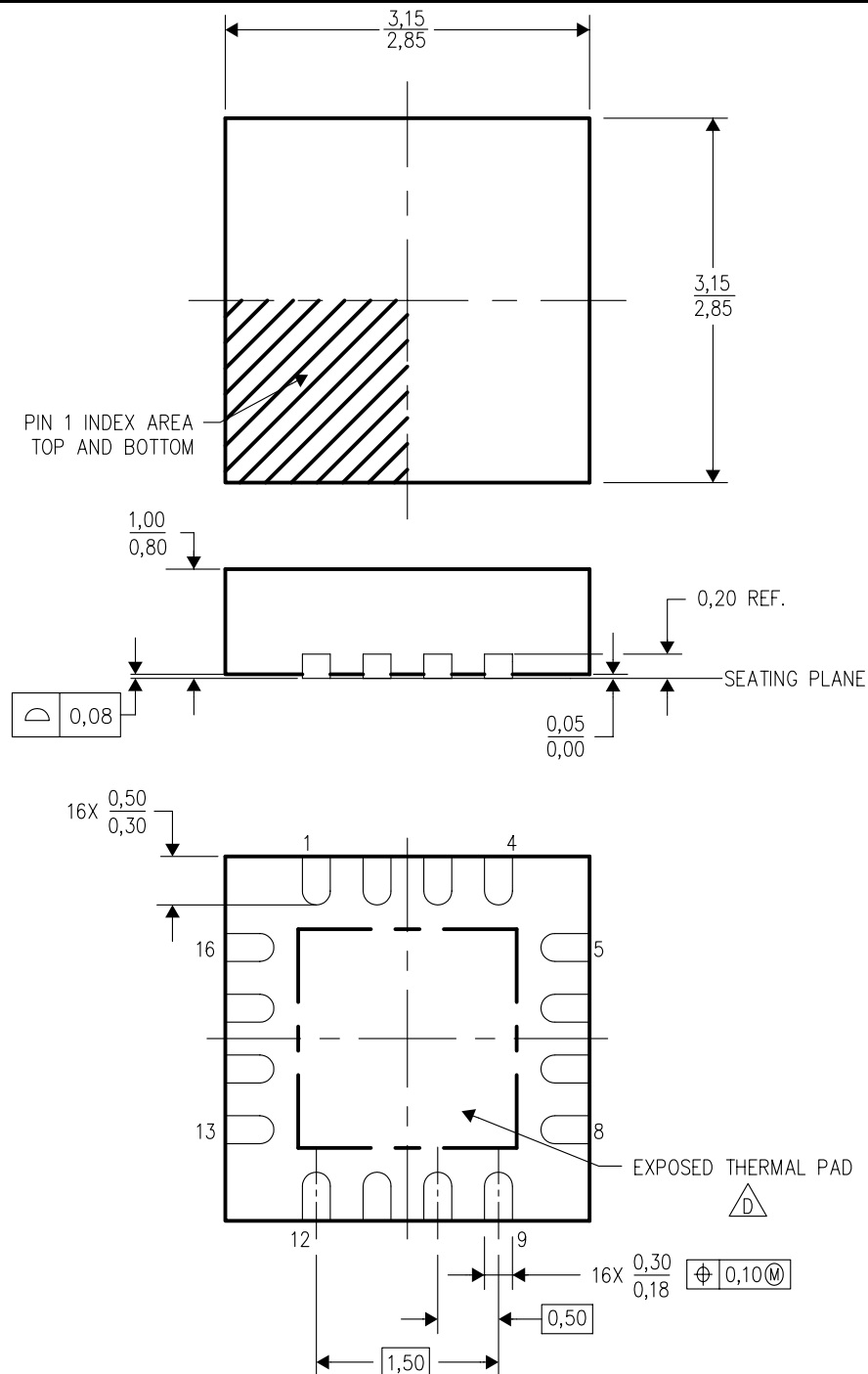
For ± 5 -V operation: $R1=10\text{ k}\Omega$, $R2 = 15\text{ k}\Omega$, $V_{tail} = 3.33\text{ V}$, $V_{REF}= 4.096\text{ V}$

For ± 10 -V operation: $R1=10\text{ k}\Omega$, $R2 = 39\text{ k}\Omega$, $V_{tail} = 2.56\text{ V}$, $V_{REF} = 4.096\text{ V}$

For ± 12 -V operation: $R1=10\text{ k}\Omega$, $R2 = 49\text{ k}\Omega$, $V_{tail} = 2.45\text{ V}$, $V_{REF} = 4.096\text{ V}$

RGT (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4203495/E 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - $\triangle D$ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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