19-2836; Rev 1; 9/03

MAXIM

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

General Description

The MAX1191 is an ultra-low-power, dual, 8-bit, 7.5Msps analog-to-digital converter (ADC). The device features two fully differential wideband track-and-hold (T/H) inputs. These inputs have a 440MHz bandwidth and accept fully differential or single-ended signals. The MAX1191 delivers a typical signal-to-noise and distortion (SINAD) of 48.6dB at an input frequency of 1.875MHz and a sampling rate of 7.5Msps while consuming only 12mW. This ADC operates from a 2.7V to 3.6V analog power supply. A separate 1.8V to 3.6V supply powers the digital output driver. In addition to ultra-low operating power, the MAX1191 features three power-down modes to conserve power during idle periods. Excellent dynamic performance, ultra-low power, and small size make the MAX1191 ideal for applications in imaging, instrumentation, and digital communications.

An internal 1.024V precision bandgap reference sets the full-scale range of the ADC to ±0.512V. A flexible reference structure allows the MAX1191 to use its internal reference or accept an externally applied reference for applications requiring increased accuracy.

The MAX1191 features parallel, multiplexed, CMOS-compatible tri-state outputs. The digital output format is offset binary. A separate digital power input accepts a voltage from 1.8V to 3.6V for flexible interfacing to different logic levels. The MAX1191 is available in a 5mm × 5mm, 28-pin thin QFN package, and is specified for the extended industrial (-40°C to +85°C) temperature range.

For higher sampling frequency applications, refer to the MAX1195–MAX1198 dual 8-bit ADCs. Pin-compatible versions of the MAX1191 are also available. Refer to the MAX1192 data sheet for 22Msps, and the MAX1193 data sheet for 45Msps.

Applications

Ultrasound and Medical Imaging

IQ Baseband Sampling

Battery-Powered Portable Instruments

Low-Power Video

WLAN, Mobile DSL, WLL Receiver

Features

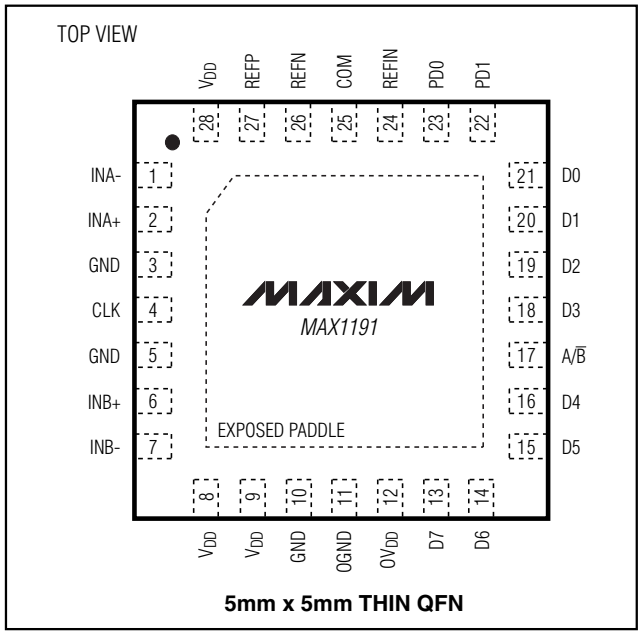
- **Ultra-Low Power**
  12mW (Normal Operation: 7.5Msps)
  0.3µW (Shutdown Mode)
- **Excellent Dynamic Performance**
  48.7dB SNR at f_{IN} = 1.875MHz
  69dBc SFDR at f_{IN} = 1.875MHz
- **2.7V to 3.6V Single Analog Supply**
- **1.8V to 3.6V TTL/CMOS-Compatible Digital Outputs**
- **Fully Differential or Single-Ended Analog Inputs**
- **Internal/External Reference Option**
- **Multiplexed CMOS-Compatible Tri-State Outputs**
- **28-Pin Thin QFN Package**
- **Evaluation Kit Available (Order MAX1193EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1191ETI-T	-40°C to +85°C	28 Thin QFN-EP* (5mm x 5mm)

**EP = Exposed paddle.*

Pin Configuration



5mm x 5mm THIN QFN

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, OV_{DD} to GND .....-0.3V to +3.6V
OGND to GND.....-0.3V to +0.3V
INA+, INA-, INB+, INB- to GND .....-0.3V to (V_{DD} + 0.3V)
CLK, REFIN, REFP, REFN, COM to GND...-0.3V to (V_{DD} + 0.3V)
PD0, PD1 to OGND .....-0.3V to (OV_{DD} + 0.3V)
Digital Outputs to OGND.....-0.3V to (OV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derated 20.8mW/°C above +70°C) ...1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, f_{CLK} = 7.5MHz, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL			±0.15	±1.00	LSB
Differential Nonlinearity	DNL	No missing codes over temperature		±0.13	±1.00	LSB
Offset Error		≥+25°C			±4	%FS
		<+25°C			±6	
Gain Error		Excludes REFP - REFN error			±2	%FS
DC Gain Matching				±0.01	±0.2	dB
Gain Temperature Coefficient				±30		ppm/°C
Power-Supply Rejection		Offset (V_{DD} ±5%)		±0.2		LSB
		Gain (V_{DD} ±5%)		±0.05		
ANALOG INPUT						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±0.512		V
Common-Mode Input Voltage Range	V_{COM}			V_{DD} / 2		V
Input Resistance	R_{IN}	Switched capacitor load		720		kΩ
Input Capacitance	C_{IN}			5		pF
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		7.5			MHz
Data Latency		Channel A		5.0		Clock cycles
		Channel B		5.5		
DYNAMIC CHARACTERISTICS (differential inputs, 4096 point FFT)						
Signal-to-Noise Ratio (Note 2)	SNR	f_{IN} = 1.875MHz	47	48.7		dB
		f_{IN} = 3.75MHz		48.6		
Signal-to-Noise and Distortion (Note 2)	SINAD	f_{IN} = 1.875MHz	47	48.6		dB
		f_{IN} = 3.75		48.5		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, f_{CLK} = 7.5MHz, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range (Note 2)	SFDR	f_{IN} = 1.875MHz	59	69		dBc
		f_{IN} = 3.75MHz		68.7		
Third-Harmonic Distortion (Note 2)	HD3	f_{IN} = 1.875MHz		72.0		dBc
		f_{IN} = 3.75MHz		-70.0		
Intermodulation Distortion	IMD	f_{IN1} = 1MHz at -7dB FS, f_{IN2} = 1.01MHz at -7dB FS		-66		dBc
Third-Order Intermodulation	IM3	f_{IN1} = 1MHz at -7dB FS, f_{IN2} = 1.01MHz at -7dB FS		-70		dBc
Total Harmonic Distortion (Note 2)	THD	f_{IN} = 1.875MHz		-68.0	-57.0	dBc
		f_{IN} = 3.75MHz		-67.0		
Small-Signal Bandwidth	SSBW	Input at -20dB FS		440		MHz
Full-Power Bandwidth	FPBW	Input at -0.5dB FS		440		MHz
Aperture Delay	t_{AD}			1.5		ns
Aperture Jitter	t_{AJ}	1dB SNR degradation at Nyquist		2		ps_{RMS}
Overdrive Recovery Time		1.5 × full-scale input		2		ns
INTERNAL REFERENCE (REFIN = V_{DD}; V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFP Output Voltage		V_{REFP} - V_{COM}		0.256		V
REFN Output Voltage		V_{REFN} - V_{COM}		-0.256		V
COM Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}		0.512		V
Differential Reference Output Temperature Coefficient	V_{REFTC}			±30		ppm/°C
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
BUFFERED EXTERNAL REFERENCE (V_{REFIN} = 1.024V, V_{REFP}, V_{REFN}, and V_{COM} are generated internally)						
REFIN Input Voltage	V_{REFIN}			1.024		V
COM Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}		0.512		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, f_{CLK} = 7.5MHz, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Resistance				>500		kΩ
REFIN Input Current				-0.7		µA
UNBUFFERED EXTERNAL REFERENCE (REFIN = GND, V_{REFP}, V_{REFN}, and V_{COM} are applied						
REFP Input Voltage		V_{REFP} - V_{COM}		0.256		V
REFN Input Voltage		V_{REFN} - V_{COM}		-0.256		V
COM Input Voltage	V_{COM}			V_{DD} / 2		V
Differential Reference Input Voltage	V_{REF}	V_{REFP} - V_{REFN}		0.512		V
REFP Input Resistance	R_{REFP}	Measured between REFP and COM		4		kΩ
REFN Input Resistance	R_{REFN}	Measured between REFN and COM		4		kΩ
DIGITAL INPUTS (CLK, PD0, PD1)						
Input High Threshold	V_{IH}	CLK	0.7 x V_{DD}			V
		PD0, PD1	0.7 x OV_{DD}			
Input Low Threshold	V_{IL}	CLK			0.3 x V_{DD}	V
		PD0, PD1			0.3 x OV_{DD}	
Input Hysteresis	V_{HYST}			0.1		V
Digital Input Leakage Current	DI_{IN}	CLK at GND or V_{DD}			±5	µA
		PD0 and PD1 at OGND or OV_{DD}			±5	
Digital Input Capacitance	DC_{IN}			5		pF
DIGITAL OUTPUTS (D7–D0, A/$\overline{B}$)						
Output Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}				±5	µA
Tri-State Output Capacitance	C_{OUT}			5		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Digital Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), $C_L \approx$ 10pF at digital outputs, f_{CLK} = 7.5MHz, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	I_{DD}	Normal operating mode, f_{IN} = 1.875MHz at -0.5dB FS, CLK input from GND to V_{DD}		4.0	5.0	mA
		Idle mode (tri-state), f_{IN} = 1.875MHz at -0.5dB FS, CLK input from GND to V_{DD}		4.0		
		Standby mode, CLK input from GND to V_{DD}		2.2		
		Shutdown mode, CLK = GND or V_{DD}, PD0 = PD1 = OGND		0.1	5.0	µA
Digital Output Supply Current (Note 3)	I_{ODD}	Normal operating mode, f_{IN} = 1.875MHz at -0.5dB FS, $C_L \approx$ 10pF		1.0		mA
		Idle mode (tri-state), DC input, CLK = GND or V_{DD}, PD0 = OV_{DD}, PD1 = OGND		0.1	5.0	µA
		Standby mode, DC input, CLK = GND or V_{DD}, PD0 = OGND, PD1 = OV_{DD}		0.1		
		Shutdown mode, CLK = GND or V_{DD}, PD0 = PD1 = OGND		0.1	5.0	
TIMING CHARACTERISTICS						
CLK Rise to CHA Output Data Valid	t_{DOA}	50% of CLK to 50% of data, Figure 5 (Note 4)	1	6	8.5	ns
CLK Fall to CHB Output Data Valid	t_{DOB}	50% of CLK to 50% of data, Figure 5 (Note 4)	1	6	8.5	ns
CLK Rise/Fall to A/$\overline{B}$ Rise/Fall Time	$t_{DA/\overline{B}}$	50% of CLK to 50% of A/$\overline{B}$, Figure 5 (Note 4)	1	6	8.5	ns
PD1 Rise to Output Enable	t_{EN}	PD0 = OV_{DD}		5		ns
PD1 Fall to Output Disable	t_{DIS}	PD0 = OV_{DD}		5		ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±10		%
Wake-Up Time from Shutdown Mode	$t_{WAKE, SD}$	(Note 5)		20		µs
Wake-Up Time from Standby Mode	$t_{WAKE, ST}$	(Note 5)		5.5		µs
Digital Output Rise/Fall Time		20% to 80%		2		ns
INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		$f_{IN,X}$ = 1.875MHz at -0.5dB FS, $f_{IN,Y}$ = 0.3MHz at -0.5dB FS (Note 6)		-75		dB
Amplitude Matching		f_{IN} = 1.875MHz at -0.5dB FS (Note 7)		±0.03		dB
Phase Matching		f_{IN} = 1.875MHz at -0.5dB FS (Note 7)		±0.03		Degrees

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, f_{CLK} = 7.5MHz, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

Note 1: Specifications ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.

Note 2: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dB FS referenced to the amplitude of the digital output. SNR and THD are calculated using HD2 through HD6.

Note 3: The power consumption of the output driver is proportional to the load capacitance (C_L).

Note 4: Guaranteed by design and characterization. Not production tested.

Note 5: SINAD settles to within 0.5dB of its typical value.

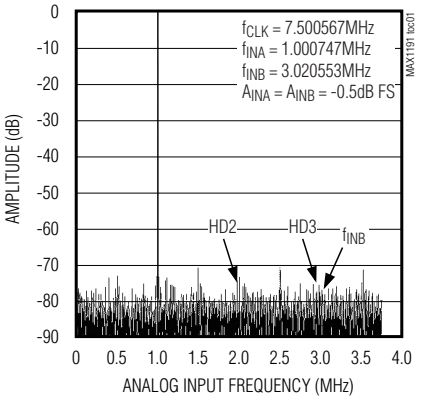
Note 6: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as power ratio of the first and second channel FFT test tone bins.

Note 7: Amplitude/phase matching is measured by applying the same signal to each channel, and comparing the magnitude and phase of the fundamental bin on the calculated FFT.

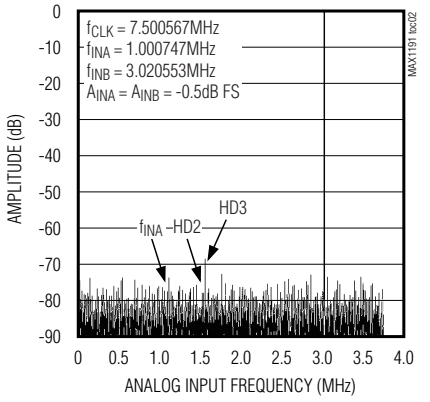
Typical Operating Characteristics

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

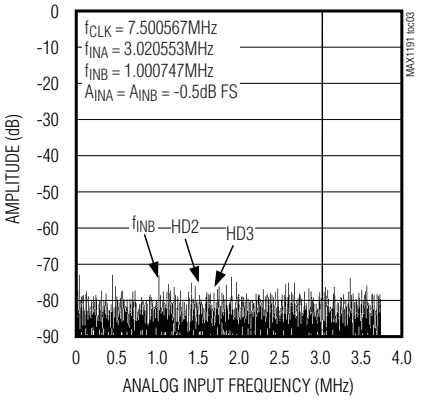
FFT PLOT CHANNEL A (DIFFERENTIAL INPUTS, 8192-POINT DATA RECORD)



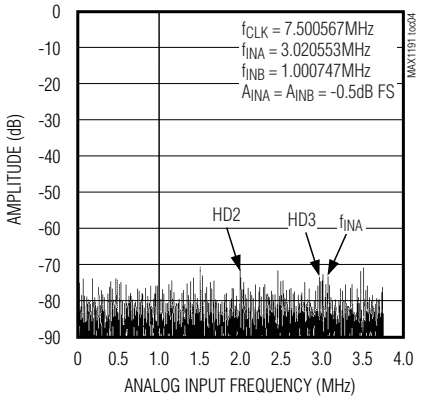
FFT PLOT CHANNEL B (DIFFERENTIAL INPUTS, 8192-POINT DATA RECORD)



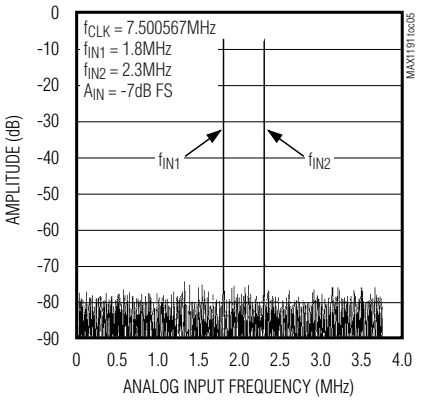
FFT PLOT CHANNEL A (DIFFERENTIAL INPUTS, 8192-POINT DATA RECORD)



FFT PLOT CHANNEL B (DIFFERENTIAL INPUTS, 8192-POINT DATA RECORD)



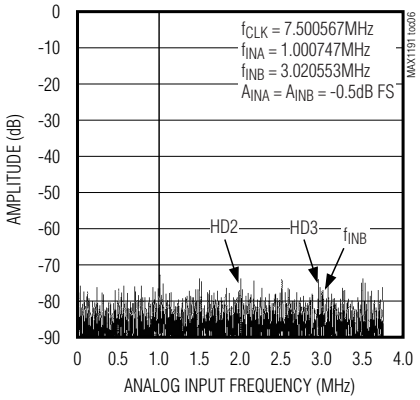
TWO-TONE IMD PLOT (DIFFERENTIAL INPUTS, 8192-POINT DATA RECORD)



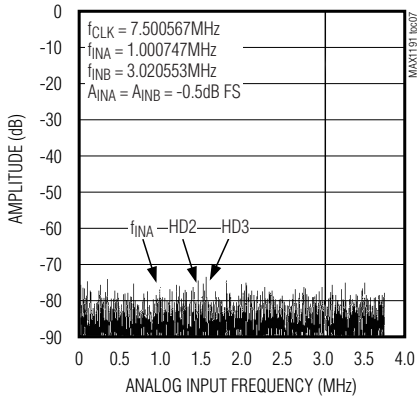
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

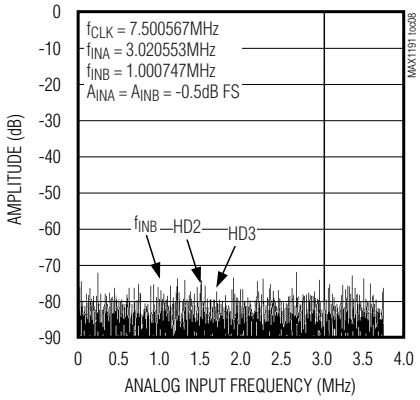
FFT PLOT CHANNEL A (SINGLE-ENDED INPUTS, 8192-POINT DATA RECORD)



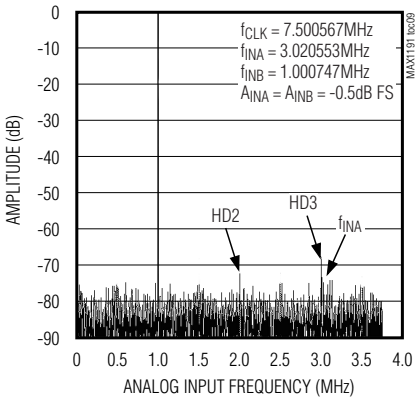
FFT PLOT CHANNEL B (SINGLE-ENDED INPUTS, 8192-POINT DATA RECORD)



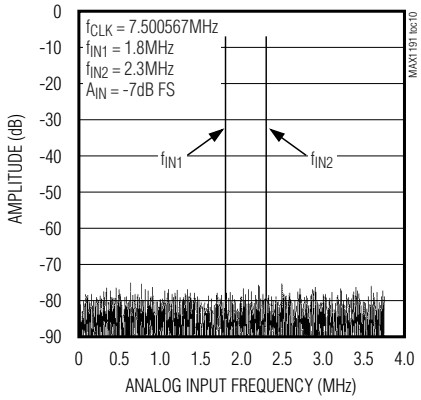
FFT PLOT CHANNEL A (SINGLE-ENDED INPUTS, 8192-POINT DATA RECORD)



FFT PLOT CHANNEL B (SINGLE-ENDED INPUTS, 8192-POINT DATA RECORD)



TWO-TONE IMD PLOT (SINGLE-ENDED INPUTS, 8192-POINT DATA RECORD)

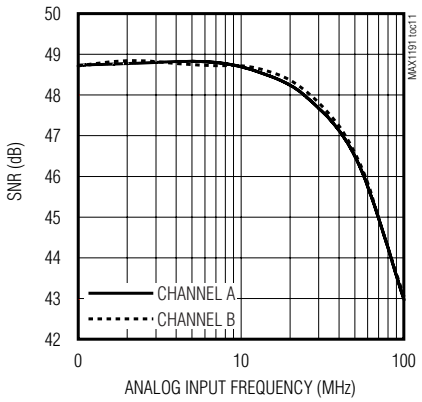


Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

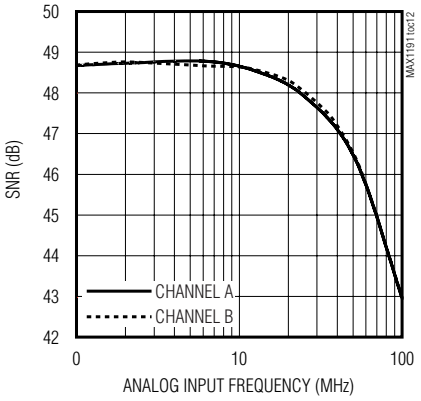
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

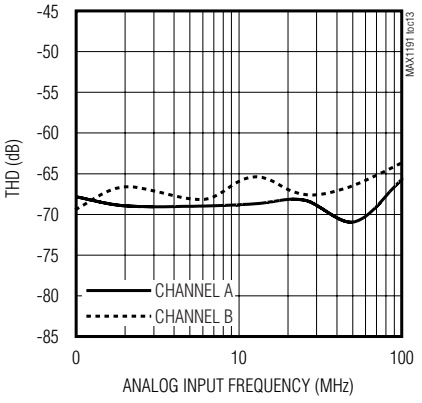
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



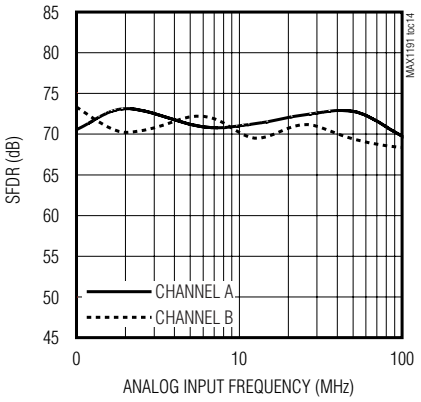
SIGNAL-TO-NOISE AND DISTORTION vs. ANALOG INPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



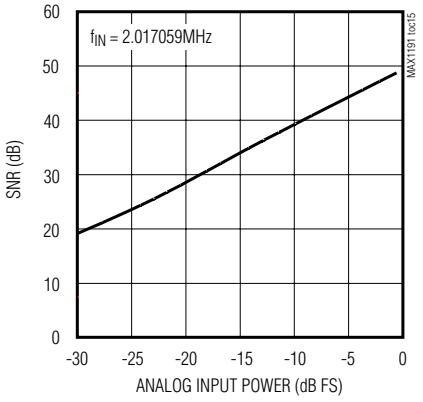
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



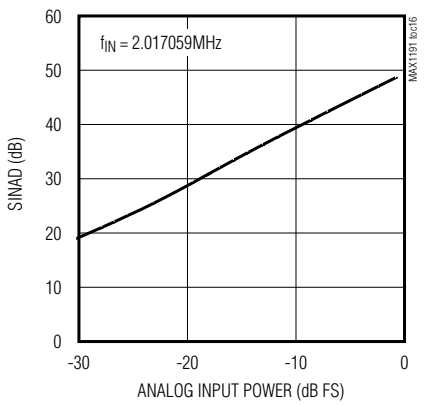
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

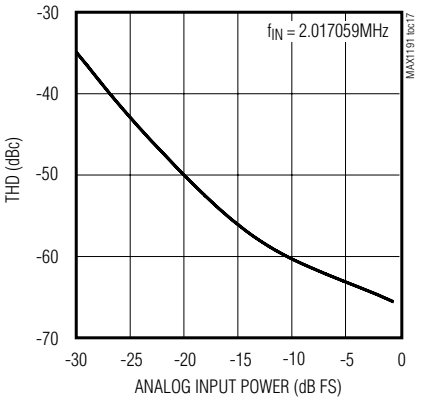
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT POWER



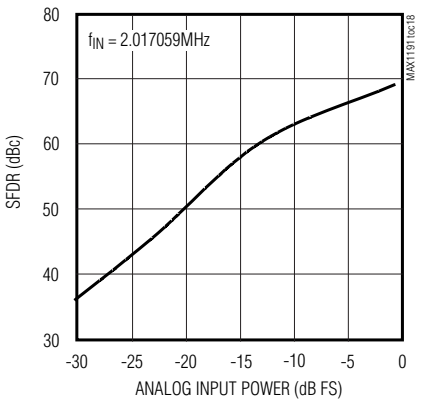
SIGNAL-TO-NOISE AND DISTORTION vs. ANALOG INPUT POWER



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT POWER



SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER

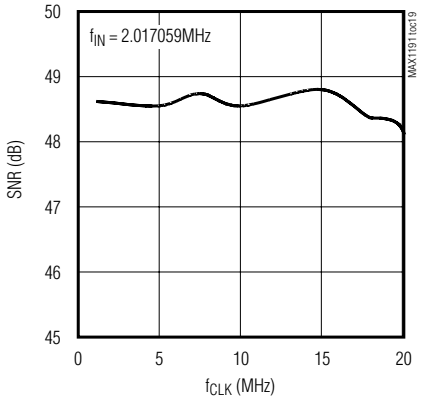


Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

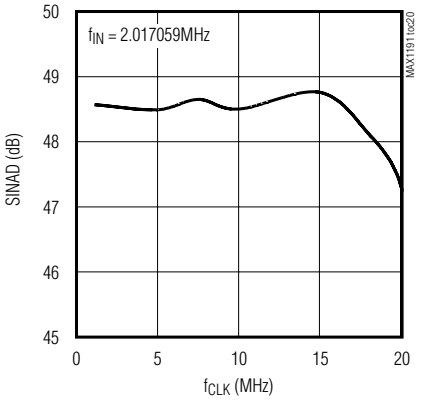
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

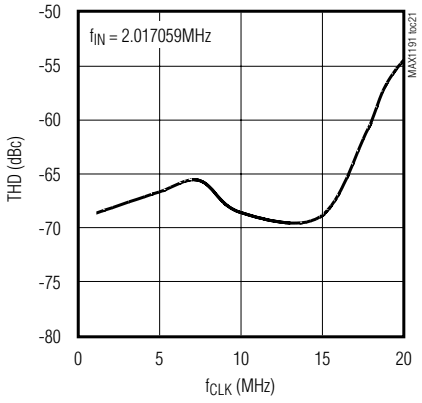
SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



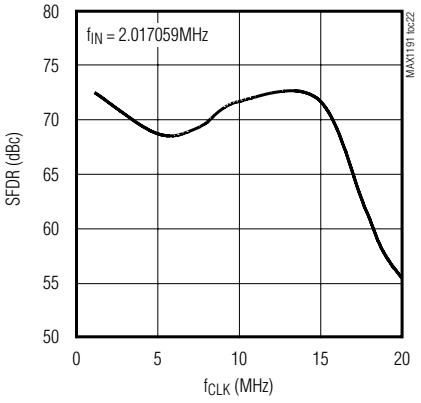
SIGNAL-TO-NOISE AND DISTORTION vs. SAMPLING RATE



TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



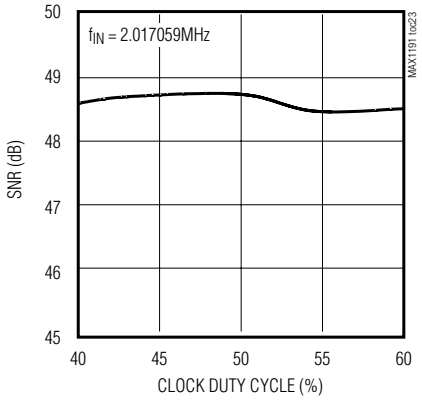
SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



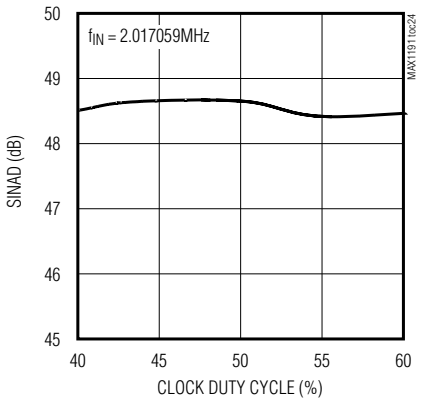
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

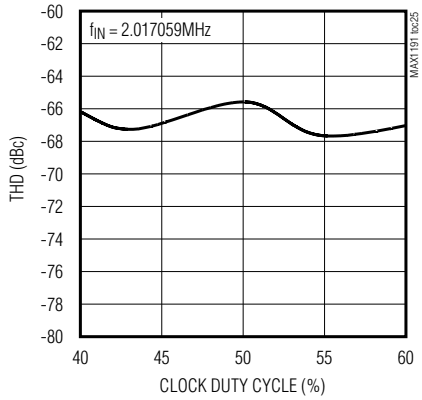
SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



SIGNAL-TO-NOISE AND DISTORTION vs. CLOCK DUTY CYCLE



TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



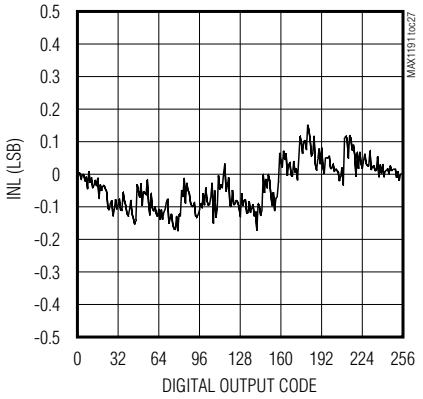
SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

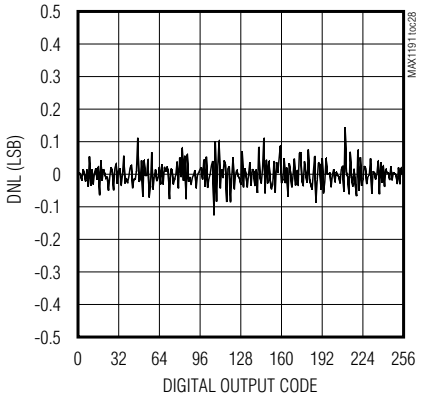
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

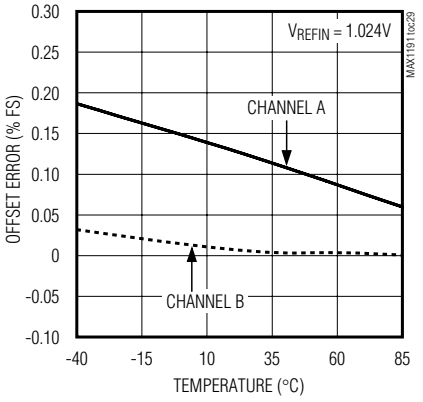
INTEGRAL NONLINEARITY



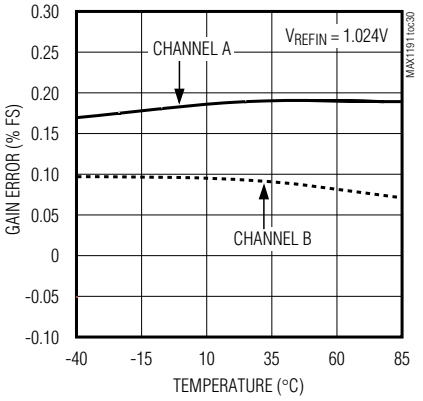
DIFFERENTIAL NONLINEARITY



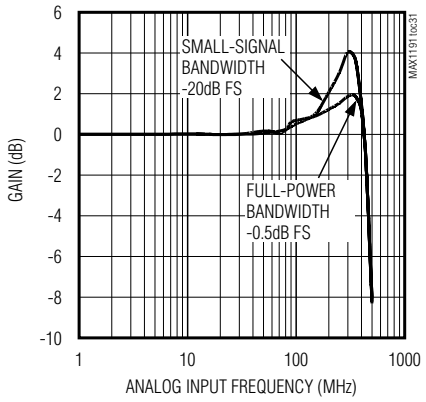
OFFSET ERROR vs. TEMPERATURE



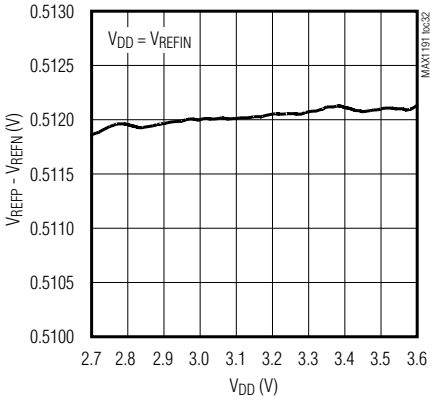
GAIN ERROR vs. TEMPERATURE



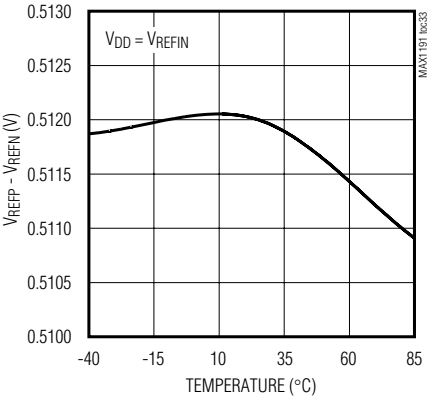
INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY



REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



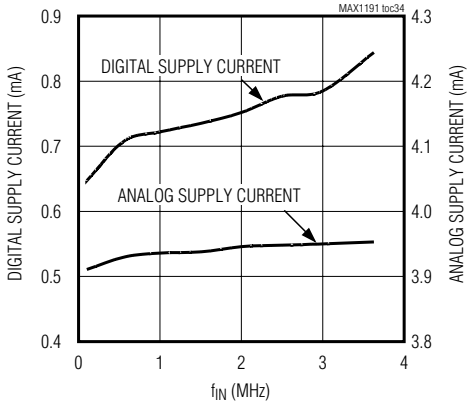
REFERENCE VOLTAGE vs. TEMPERATURE



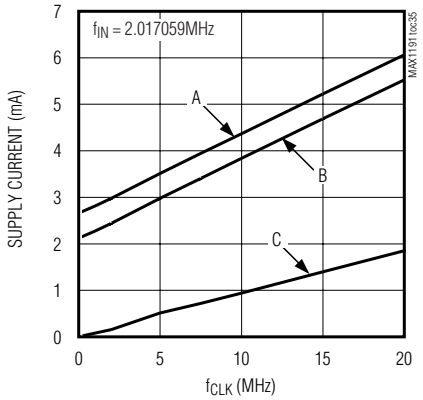
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 1.8V, V_{REFIN} = V_{DD} (internal reference), C_L ≈ 10pF at digital outputs, differential input at -0.5dB FS, f_{CLK} = 7.500567MHz at 50% duty cycle, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. INPUT FREQUENCY



SUPPLY CURRENT vs. SAMPLING RATE



A: ANALOG SUPPLY CURRENT (I_{DD}) - INTERNAL AND BUFFERED EXTERNAL REFERENCE MODES
B: ANALOG SUPPLY CURRENT (I_{DD}) - UNBUFFERED EXTERNAL REFERENCE MODE
C: DIGITAL SUPPLY CURRENT (I_{ODD}) - ALL REFERENCE MODES

Pin Description

PIN	NAME	FUNCTION
1	INA-	Channel A Negative Analog Input. For single-ended operation, connect INA- to COM.
2	INA+	Channel A Positive Analog Input. For single-ended operation, connect signal source to INA+.
3, 5, 10	GND	Analog Ground. Connect all GND pins together.
4	CLK	Converter Clock Input
6	INB+	Channel B Positive Analog Input. For single-ended operation, connect signal source to INB+.
7	INB-	Channel B Negative Analog Input. For single-ended operation, connect INB- to COM.
8, 9, 28	V_{DD}	Converter Power Input. Connect to a 2.7V to 3.6V power supply. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
11	OGND	Output Driver Ground
12	OV_{DD}	Output Driver Power Input. Connect to a 1.8V to V_{DD} power supply. Bypass OV_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
13	D7	Tri-State Digital Output. D7 is the most significant bit (MSB).
14	D6	Tri-State Digital Output
15	D5	Tri-State Digital Output
16	D4	Tri-State Digital Output
17	A/$\overline{B}$	Channel Data Indicator. This digital output indicates channel A data (A/$\overline{B}$ = 1) or channel B data (A/$\overline{B}$ = 0) is present on the output.
18	D3	Tri-State Digital Output
19	D2	Tri-State Digital Output
20	D1	Tri-State Digital Output
21	D0	Tri-State Digital Output. D0 is the least significant bit (LSB).
22	PD1	Power-Down Digital Input 1. See Table 3.

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

Pin Description (continued)

PIN	NAME	FUNCTION
23	PD0	Power-Down Digital Input 0. See Table 3.
24	REFIN	Reference Input. Internally pulled up to V_{DD}.
25	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
26	REFN	Negative Reference I/O. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.33µF capacitor.
27	REFP	Positive Reference I/O. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFP to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Internally connected to pin 3. Externally connect EP to GND.

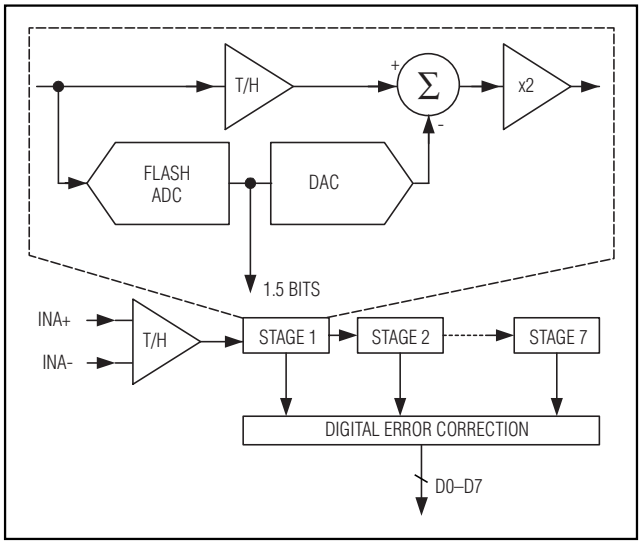


Figure 1. Pipeline Architecture—Stage Blocks

Detailed Description

The MAX1191 uses a seven-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half-clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel A and 5.5 clock cycles for channel B.

At each stage, flash ADCs convert the held input voltages into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage where the process is repeated until the signal has been processed by all stages. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. Figure 2 shows the MAX1191 functional diagram.

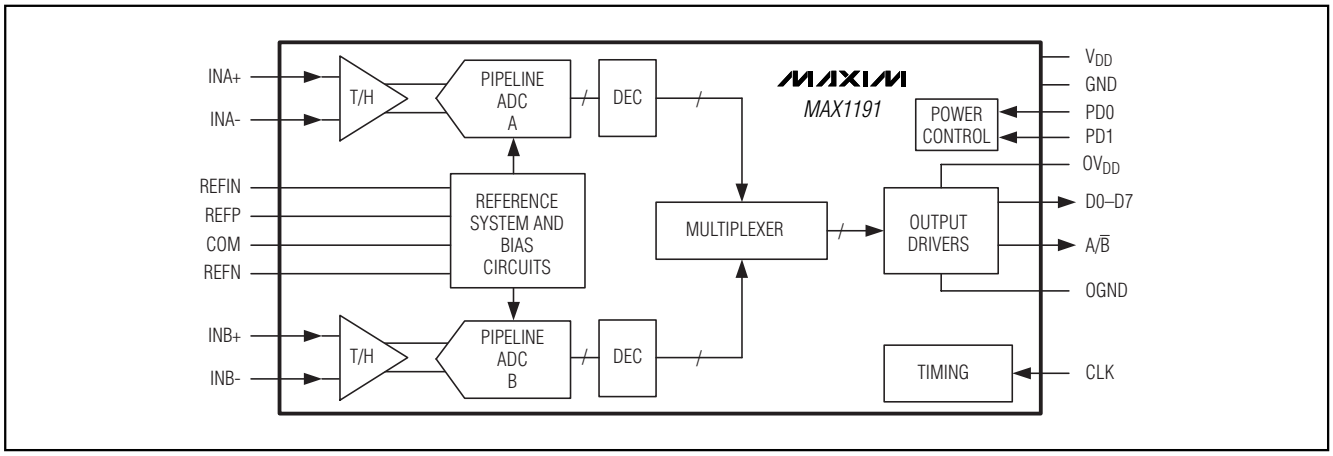


Figure 2. MAX1191 Functional Diagram

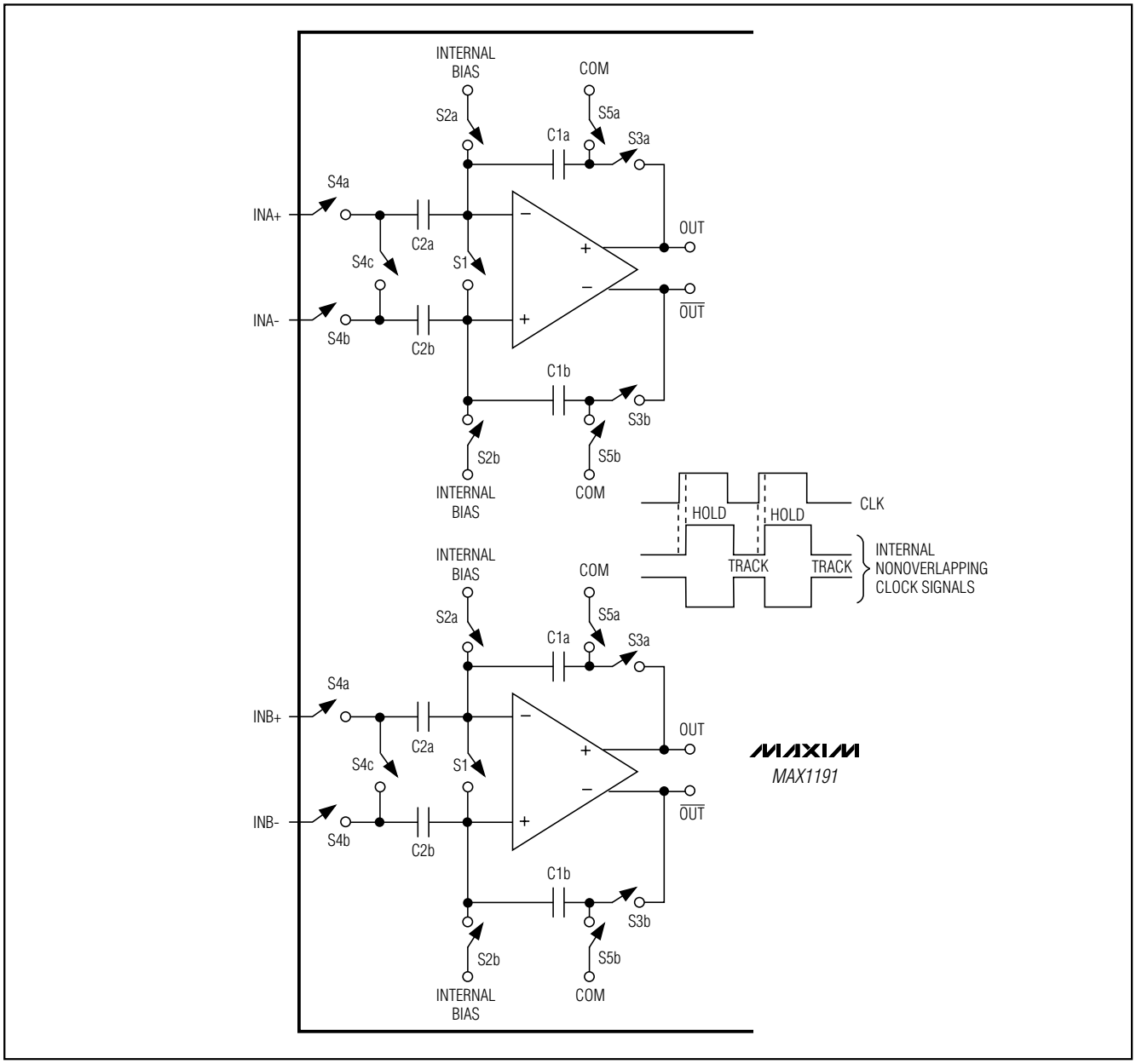


Figure 3. Internal T/H Circuits

Input Track-and-Hold (T/H) Circuits

Figure 3 displays a simplified functional diagram of the input T/H circuits. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the amplifier input, and open simultaneously with S1, sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers charge capacitors C1a and C1b to the same

Table 1. Reference Modes

V_{REFIN}	REFERENCE MODE
>0.8 x V_{DD}	Internal reference mode. V_{REF} is internally generated to be 0.512V. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.
1.024V ±10%	Buffered external reference mode. An external 1.024V ±10% reference voltage is applied to REFIN. V_{REF} is internally generated to be $V_{REFIN}/2$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.
<0.3V	Unbuffered external reference mode. REFP, REFN, and COM are driven by external reference sources. V_{REF} is the difference between the externally applied V_{REFP} and V_{REFN}. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.

values originally held on C2a and C2b. These values are then presented to the first stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input bandwidth T/H amplifiers allow the MAX1191 to track and sample/hold analog inputs of high frequencies (>Nyquist). Both ADC inputs (INA+, INB+, INA-, and INB-) can be driven either differentially or single ended. Match the impedance of INA+ and INA-, as well as INB+ and INB-, and set the common-mode voltage to midsupply ($V_{DD}/2$) for optimum performance.

Analog Inputs and Reference Configurations

The MAX1191 full-scale analog input range is ±V_{REF} with a common-mode input range of $V_{DD}/2$ ±0.2V. V_{REF} is the difference between V_{REFP} and V_{REFN}. The MAX1191 provides three modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 1).

In internal reference mode, connect REFIN to V_{DD} or leave REFIN unconnected. V_{REF} is internally generated to be 0.512V ±3%. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD}/2$, $V_{REFP} = V_{DD}/2 + V_{REF}/2$, and $V_{REFN} = V_{DD}/2 - V_{REF}/2$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.

In buffered external reference mode, apply a 1.024V ±10% at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD}/2$, $V_{REFP} = V_{DD}/2 + V_{REFIN}/4$, and $V_{REFN} = V_{DD}/2 - V_{REFIN}/4$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

In unbuffered external reference mode, connect REFIN to GND. This deactivates the on-chip reference buffers for COM, REFP, and REFN. With their buffers shut down, these nodes become high-impedance inputs (Figure 4) and can be driven through separate, external reference sources. Drive V_{COM} to $V_{DD}/2$ ±10%, drive

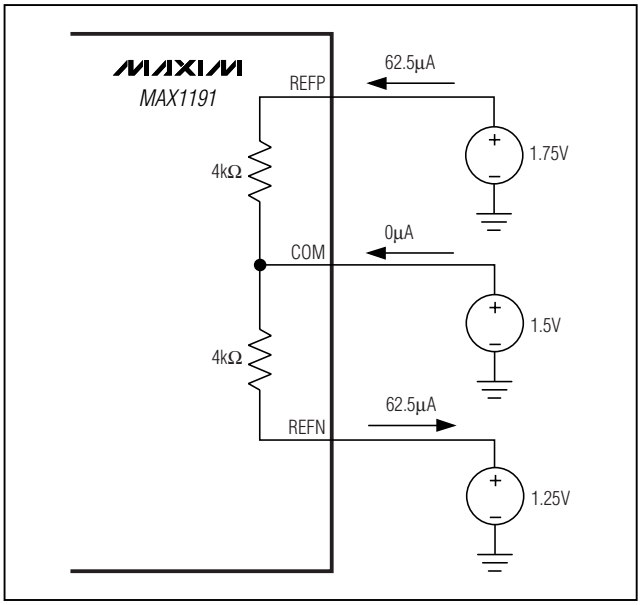


Figure 4. Unbuffered External Reference Mode Impedance

V_{REFP} to ($V_{DD}/2$ +0.256V) ±10%, and drive V_{REFN} to ($V_{DD}/2$ - 0.256V) ±10%. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.

For detailed circuit suggestions and how to drive this dual ADC in buffered/unbuffered external reference mode, see the *Applications Information* section.

Clock Input (CLK)

CLK accepts a CMOS-compatible signal level. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). In particular, sampling occurs on the rising edge of the clock signal, requiring this edge to

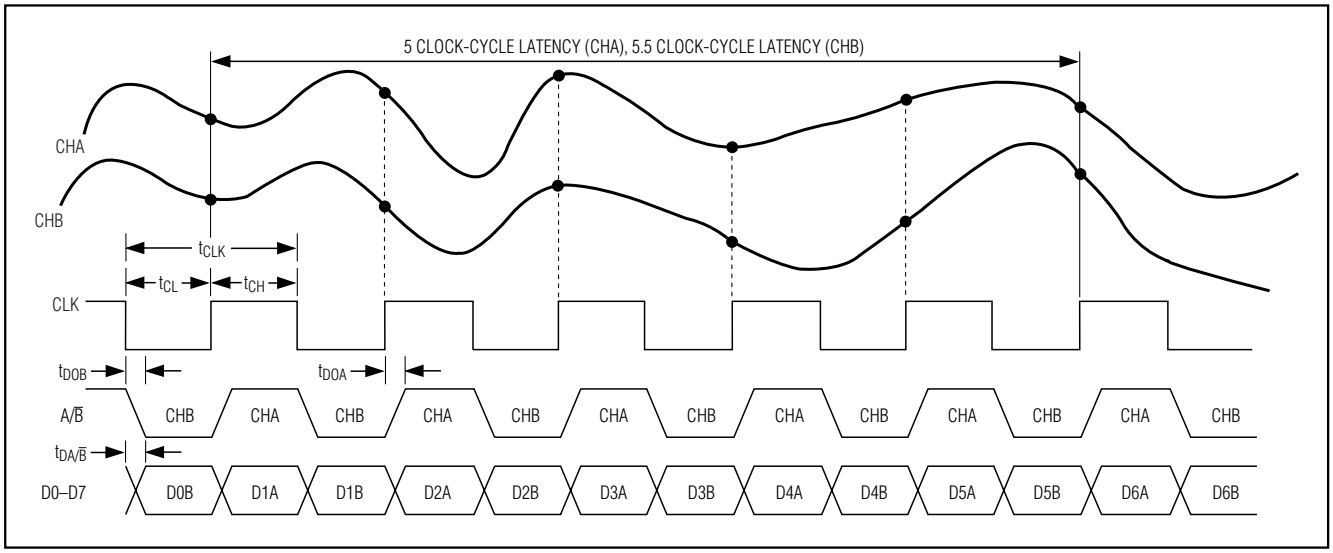


Figure 5. System Timing Diagram

provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the on-chip ADCs as follows:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}}\right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be considered as an analog input and routed away from any analog input or other digital signal lines. The MAX1191 clock input operates with a $V_{DD}/2$ voltage threshold and accepts a 50% ±10% duty cycle (see *Typical Operating Characteristics*).

System Timing Requirements

Figure 5 shows the relationship between the clock, analog inputs, A/$\overline{B}$ indicator, and the resulting output data. Channel A (CHA) and channel B (CHB) are simultaneously sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the output. CHA data is updated on the rising edge and CHB data is updated on the falling edge of the CLK. The A/$\overline{B}$ indicator follows CLK with a typical delay time of 6ns and remains high when CHA data is updated and low when CHB data is updated. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for CHA and 5.5 clock cycles for CHB.

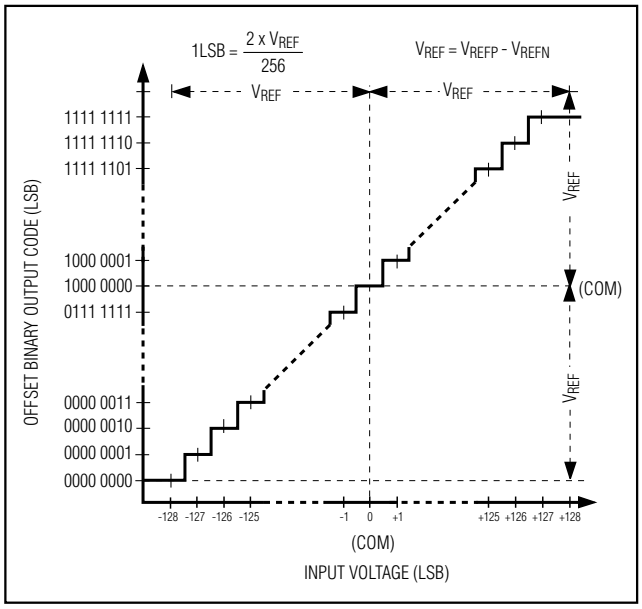


Figure 6. Transfer Function

Digital Output Data (D0–D7), Channel Data Indicator (A/$\overline{B}$)

D0–D7 and A/$\overline{B}$ are TTL/CMOS-logic compatible. The digital output coding is offset binary (Table 2, Figure 6). The capacitive load on the digital outputs D0–D7 should be kept as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX1191 and degrading its dynamic performance. Buffers on the digital outputs isolate them from

Table 2. Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE (IN+ - IN-)	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (D7–D0)	OUTPUT DECIMAL CODE
$V_{REF} \times \frac{127}{128}$	+127 (+ full scale – 1 LSB)	1111 1111	255
$V_{REF} \times \frac{126}{128}$	+126 (+ full scale – 2 LSB)	1111 1110	254
$V_{REF} \times \frac{1}{128}$	+1	1000 0001	129
$V_{REF} \times \frac{0}{128}$	0 (bipolar zero)	1000 0000	128
$-V_{REF} \times \frac{1}{128}$	-1	0111 1111	127
$-V_{REF} \times \frac{127}{128}$	-127 (- full scale + 1 LSB)	0000 0001	1
$-V_{REF} \times \frac{128}{128}$	-128 (- full scale)	0000 0000	0

Table 3. Power Logic

PD0	PD1	POWER MODE	ADC	INTERNAL REFERENCE	CLOCK DISTRIBUTION	OUTPUTS
0	0	Shutdown	Off	Off	Off	Tri-state
0	1	Standby	Off	On	On	Tri-state
1	0	Idle	On	On	On	Tri-state
1	1	Normal operating	On	On	On	On

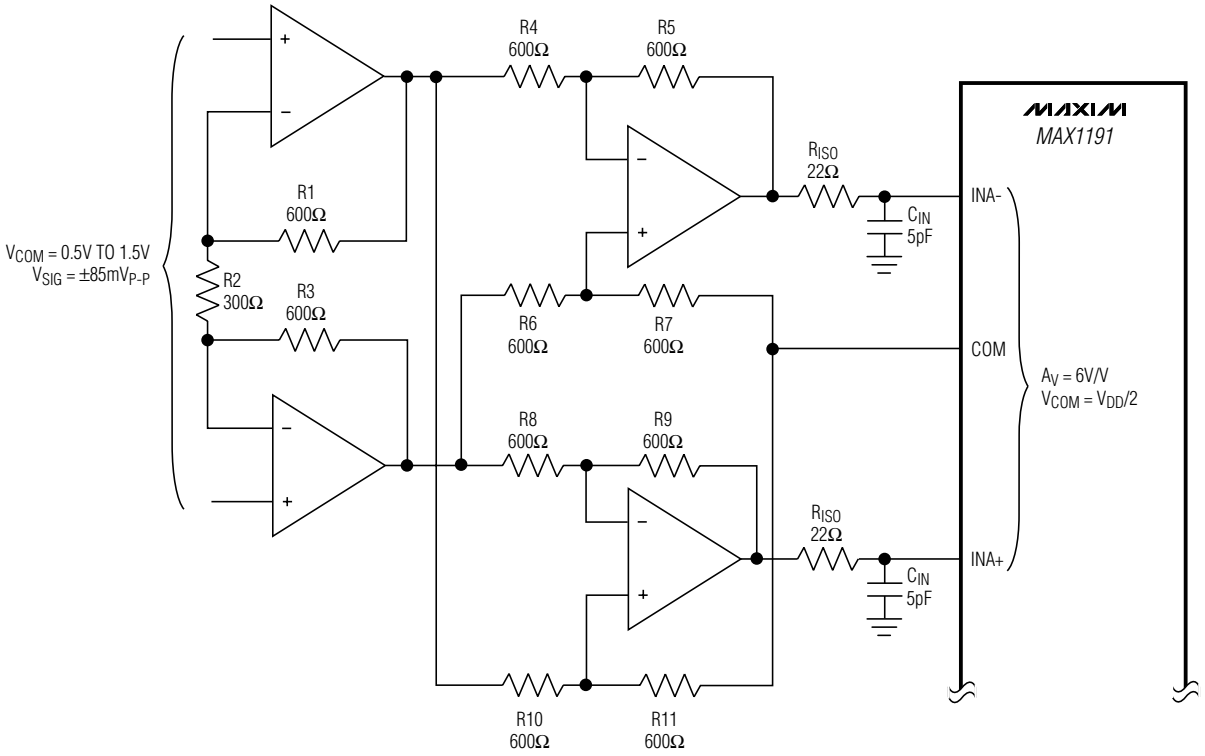
heavy capacitive loads. To improve the dynamic performance of the MAX1191, add 100Ω resistors in series with the digital outputs close to the MAX1191. Refer to the MAX1193 Evaluation Kit schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

Power Modes (PD0, PD1)

The MAX1191 has four power modes that are controlled with PD0 and PD1. Four power modes allow the MAX1191 to efficiently use power by transitioning to a low-power state when conversions are not required (Table 3).

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections of the MAX1191 and placing the outputs in tri-state. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 20µs. When operating in the unbuffered external reference mode, the wake-up time is dependent on the external reference drivers. When the outputs transition from tri-state to on, the last converted word is placed on the digital outputs.

In standby mode, the reference and clock distribution circuits are powered up, but the pipeline ADCs are unpowered and the outputs are in tri-state. The wake-up time from standby mode is dominated by the 5.5µs required to activate the pipeline ADCs. When the outputs transition from tri-state to on, the last converted word is placed on the digital outputs.



OPERATIONAL AMPLIFIERS
CHOOSE EITHER OF THE MAX4452/MAX4453/MAX4454 SINGLE/DUAL/QUAD +3V, 200MHz OP AMPS FOR USE WITH THIS CIRCUIT. CONNECT THE POSITIVE SUPPLY RAIL (V_{CC}) TO 3V. CONNECT THE NEGATIVE SUPPLY RAIL (V_{EE}) TO GROUND. DECOUPLE V_{CC} WITH A 0.1µF CAPACITOR TO GROUND.

RESISTOR NETWORKS
RESISTOR NETWORKS ENSURE PROPER THERMAL AND TOLERANCE MATCHING. FOR R1, R2, AND R3 USE A NETWORK SUCH AS VISHAY'S 3R MODEL NUMBER 300192. FOR R4–R11, USE A NETWORK SUCH AS VISHAY'S 4R MODEL NUMBER 300197.

Figure 7. DC-Coupled Differential Input Driver

In idle mode, the pipeline ADCs, reference, and clock distribution circuits are powered, but the outputs are forced to tri-state. The wake-up time from idle mode is dominated by the 5ns required for the output drivers to start from tri-state. When the outputs transition from tri-state to on, the last converted word is placed on the digital outputs.

In the normal operating mode, all sections of the MAX1191 are powered.

Applications Information

The circuit of Figure 7 operates from a single 3V supply and accommodates a wide 0.5V to 1.5V input common-mode voltage range for the analog interface between an RF quadrature demodulator (differential, DC-coupled signal source) and a high-speed ADC. Furthermore, the circuit provides required SINAD and SFDR to demodulate a wideband (BW = 3.84MHz), QAM-16 communication link. R_{ISO} isolates the op amp output from the ADC capacitive input to prevent ringing and oscillation. C_{IN} filters high-frequency noise.

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

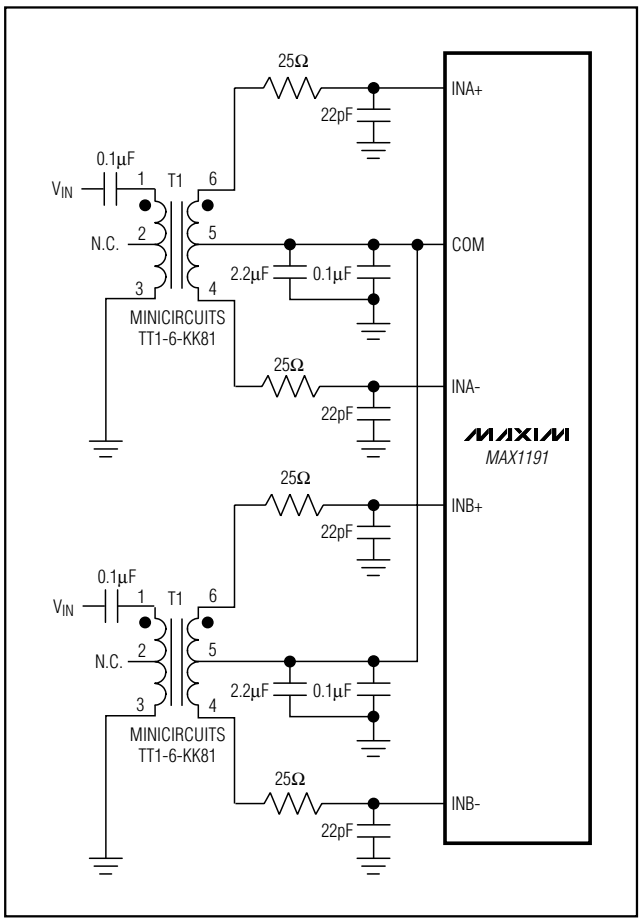


Figure 8. Transformer-Coupled Input Drive

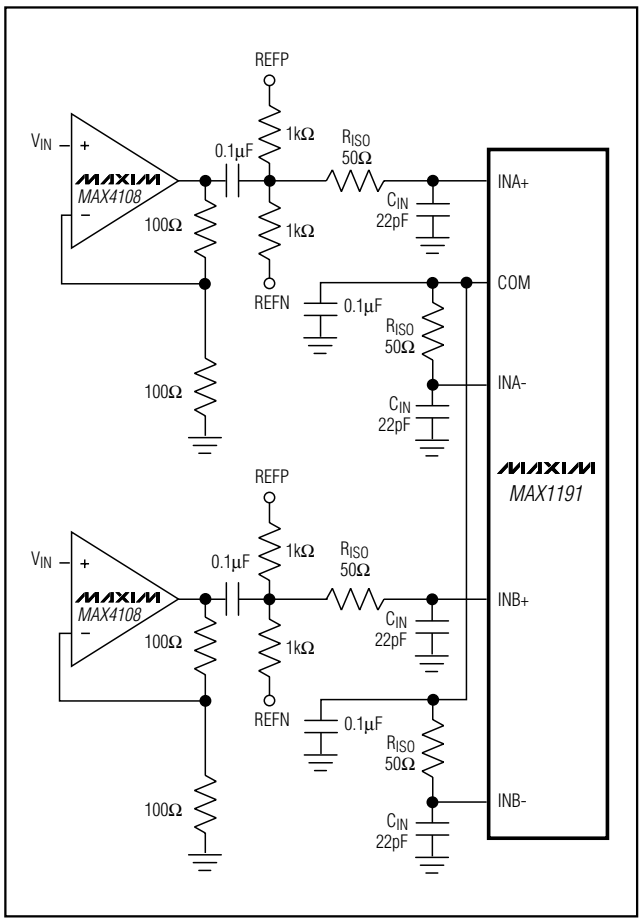


Figure 9. Using an Op Amp for Single-Ended, AC-Coupled Input Drive

Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX1191 for optimum performance. Connecting the center tap of the transformer to COM provides a $V_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion.

In general, the MAX1191 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for high input frequencies. In differential input mode, even-order harmonics are lower as both inputs (INA+, INA- and/or INB+, INB-) are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended mode.

Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application. Amplifiers such as the MAX4108 provide high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity.

Buffered External Reference Drives Multiple ADCs

The buffered external reference mode allows for more control over the MAX1191 reference voltage and allows multiple converters to use a common reference. To drive one MAX1191 in buffered external reference mode, the external circuit must sink 0.7µA, allowing one reference circuit to easily drive the REFIN of multiple converters to 1.024V ±10%.

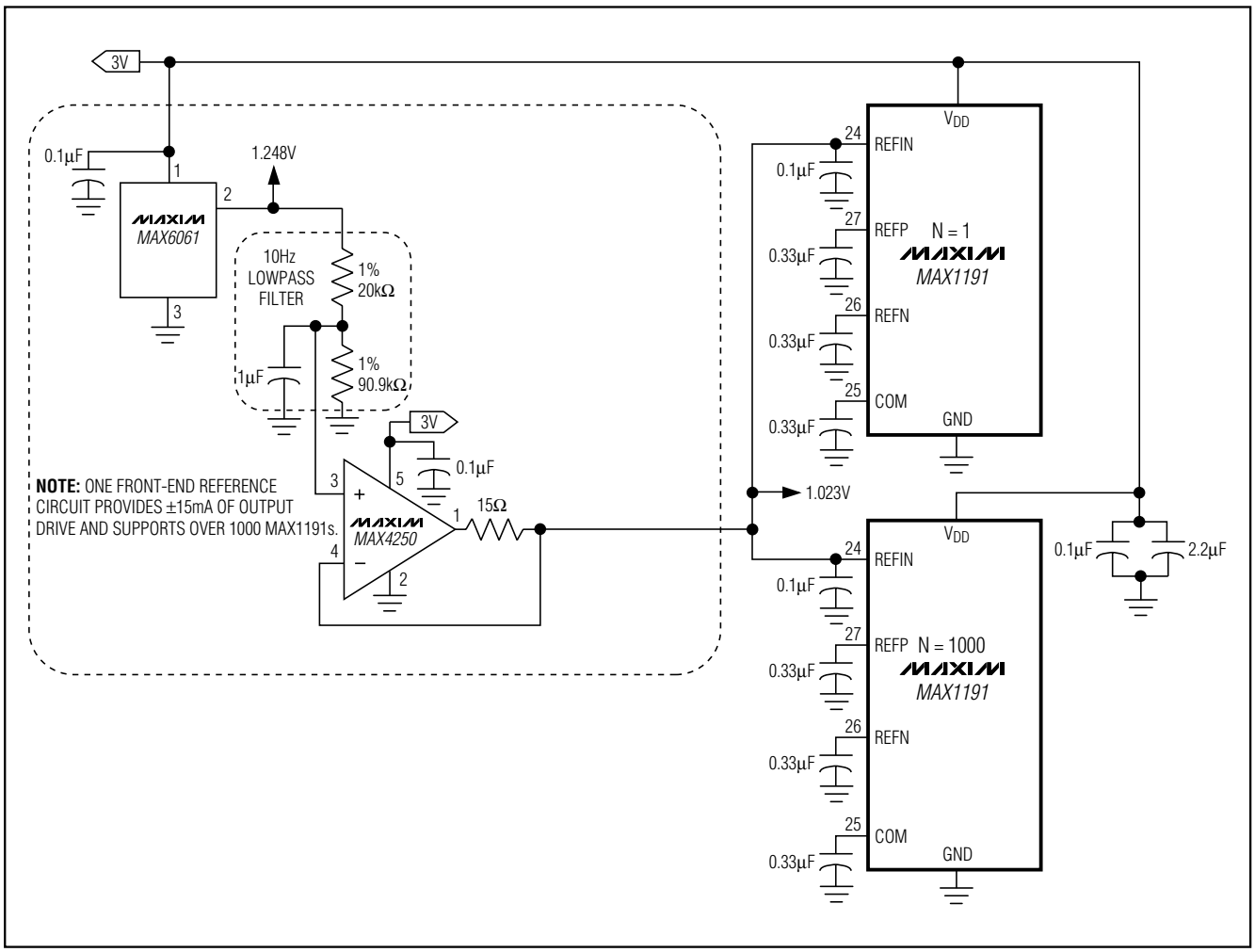


Figure 10. External Buffered (MAX4250) Reference Drive Using a MAX6062 Bandgap Reference

Figure 10 shows the MAX6061 precision bandgap reference used as a common reference for multiple converters. The 1.248V output of the MAX6061 is divided down to 1.023V as it passes through a one-pole, 10Hz, lowpass filter to the MAX4250. The MAX4250 buffers the 1.023V reference before its output is applied to the MAX1191. The MAX4250 provides a low offset voltage (for high gain accuracy) and a low noise level.

Unbuffered External Reference Drives Multiple ADCs

The unbuffered external reference mode allows for precise control over the MAX1191 reference and allows multiple converters to use a common reference. Connecting REFIN to GND disables the internal reference, allowing REFP, REFN, and COM to be driven directly by a set of external reference sources.

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

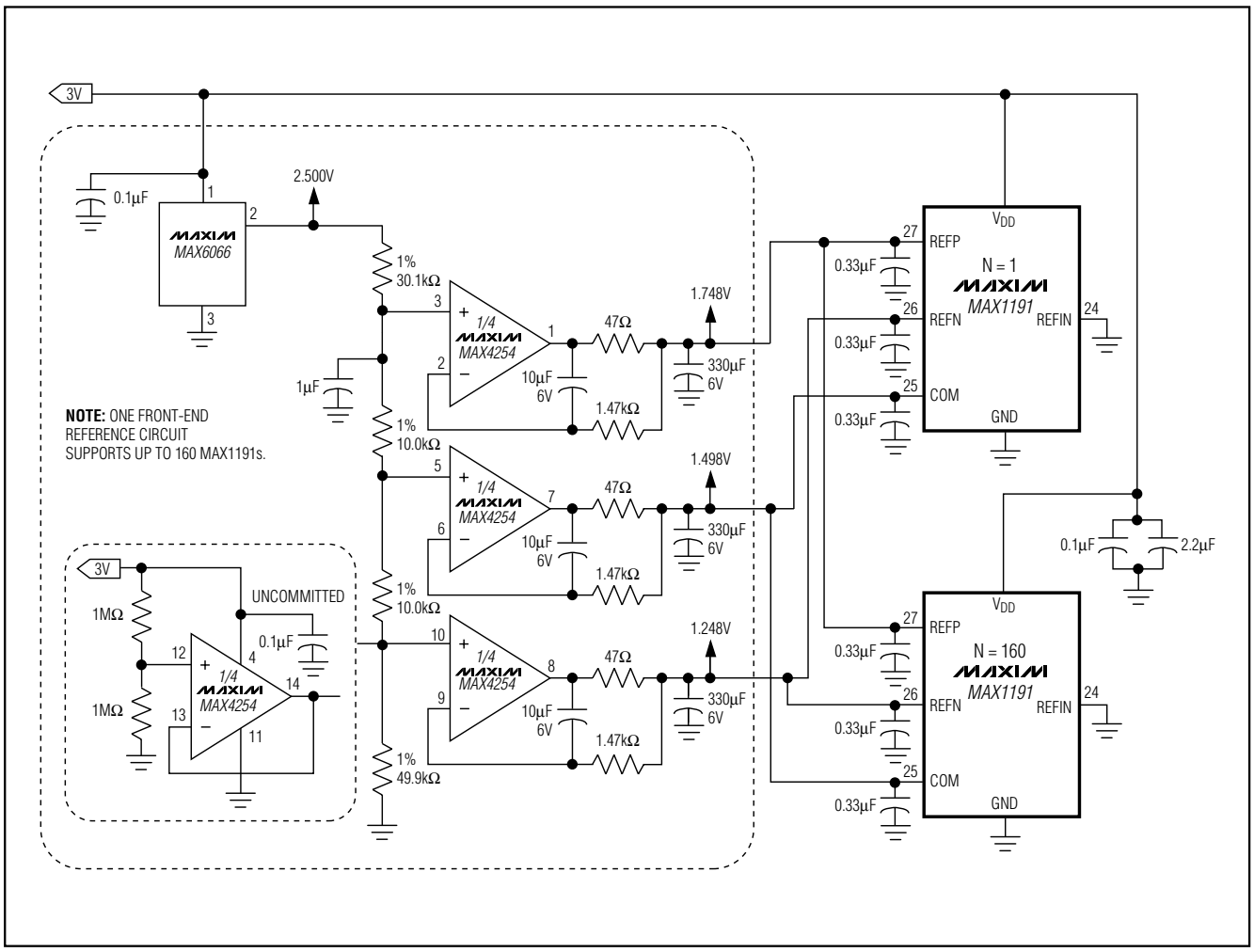


Figure 11. External Unbuffered Reference Driving 160 ADCs with MAX4254 and MAX6066

Figure 11 shows the MAX6066 precision bandgap reference used as a common reference for multiple converters. The 2.500V output of the MAX6066 is followed by a 10Hz lowpass filter and precision voltage-divider. The MAX4254 buffers the taps of this divider to provide the 1.75V, 1.5V, and 1.25V sources to drive REFP, REFN, and COM. The MAX4254 provides a low offset voltage and low noise level. The individual voltage followers are connected to 10Hz lowpass filters, which filter both the reference-voltage and amplifier noise to a level of 3nV/√Hz. The 1.75V and 1.25V reference voltages set the differential full-scale range of the associated ADCs at ±0.5V.

The common power supply for all active components removes any concern regarding power-supply sequencing when powering up or down.

With the outputs of the MAX4252 matching better than 0.1%, the buffers and subsequent lowpass filters support as many as 160 MAX1191s.

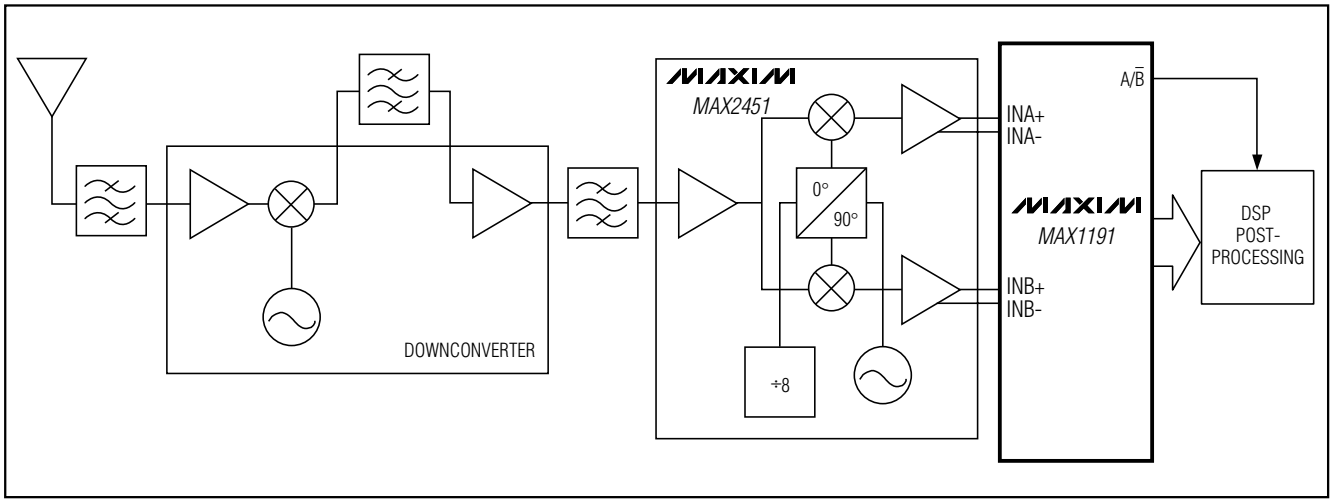


Figure 12. Typical QAM Receiver Application

Typical QAM Demodulation Application

Quadrature amplitude modulation (QAM) is frequently used in digital communications. Typically found in spread-spectrum-based systems, a QAM signal represents a carrier frequency modulated in both amplitude and phase. At the transmitter, modulating the baseband signal with quadrature outputs, a local oscillator followed by subsequent upconversion can generate the QAM signal. The result is an in-phase (I) and a quadrature (Q) carrier component, where the Q component is 90° phase shifted with respect to the in-phase component. At the receiver, the QAM signal is demodulated into analog I and Q components. Figure 12 displays the demodulation process performed in the analog domain using the MAX1191 dual-matched, 3V, 8-bit ADC and the MAX2451 quadrature demodulator to recover and digitize the I and Q baseband signals. Before being digitized by the MAX1191, the mixed-down signal components can be filtered by matched analog filters, such as Nyquist or pulse-shaping filters. The filters remove unwanted images from the mixing process, thereby enhancing the overall signal-to-noise (SNR) performance and minimizing intersymbol interference.

Grounding, Bypassing, and Board Layout

The MAX1191 requires high-speed board layout design techniques. Refer to the MAX1193 Evaluation Kit data sheet for a board layout reference. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF bipolar capacitor. Bypass OV_{DD} to OGND with a 0.1µF ceramic capacitor in parallel with a 2.2µF bipolar capacitor. Bypass REFP, REFN, and COM each to GND with a 0.33µF ceramic capacitor.

Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Use a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package. Connect the MAX1191 exposed backside paddle to GND. Join the two ground planes at a single point such that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally at a point along the gap between the two ground planes, which produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane).

Route high-speed digital signal traces away from the sensitive analog traces of either channel. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

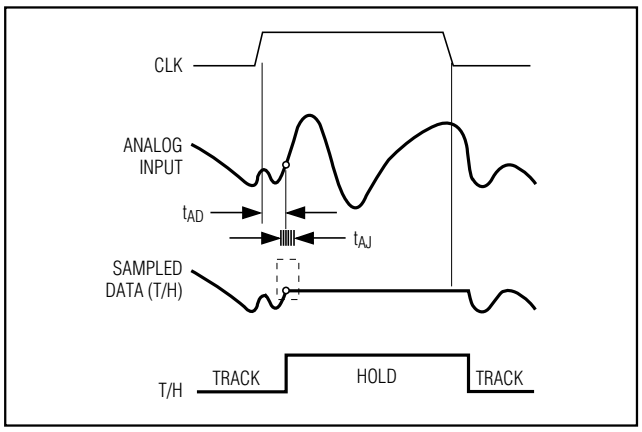


Figure 13. T/H Aperture Timing

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1191 are measured using the end-point method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Ideally, the midscale MAX1191 transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

Gain Error

Ideally, the full-scale MAX1191 transition occurs at 1.5 LSB below full-scale. The gain error is the amount of deviation between the measured transition point and the ideal transition point with the offset error removed.

Dynamic Parameter Definitions

Aperture Jitter

Figure 13 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 13).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02 \times N + 1.76$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right]$$

where V_1 is the fundamental amplitude, and V_2–V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Third Harmonic Distortion (HD3)

HD3 is defined as the ratio of the RMS value of the third harmonic component to the fundamental input signal.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the intermodulation products relative to the total input power when two tones, f1 and f2, are present at the inputs. The intermodulation products are (f1 ±f2), (2 x f1), (2 x f2), (2 x f1 ±f2), (2 x f2 ±f1). The individual input tone levels are at -7dB FS.

Third-Order Intermodulation (IM3)

IM3 is the power of the worst third-order intermodulation product relative to the input power of either input tone when two tones, f1 and f2, are present at the inputs. The third-order intermodulation products are (2 x f1 ±f2), (2 x f2 ±f1). The individual input tone levels are at -7dB FS.

Power-Supply Rejection

Power-supply rejection is defined as the shift in offset and gain error when the power supplies are moved ±5%.

Small-Signal Bandwidth

A small -20dB FS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. Note that the track/hold (T/H) performance is usually the limiting factor for the small-signal input bandwidth.

Full-Power Bandwidth

A large -0.5dB FS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by -3dB. This point is defined as full-power input bandwidth frequency.

Chip Information

TRANSISTOR COUNT: 7925

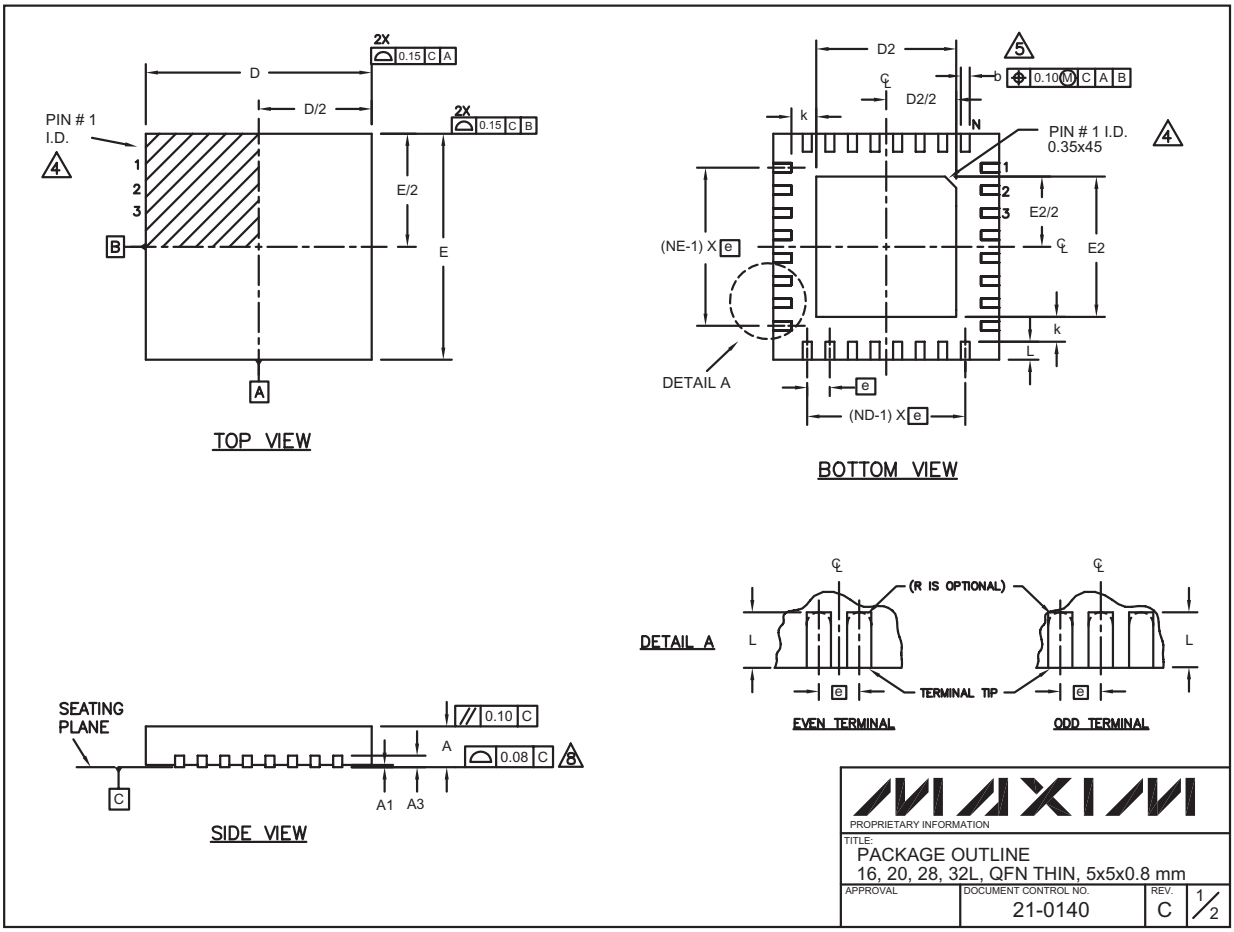
PROCESS: CMOS

Ultra-Low-Power, 7.5Msps, Dual 8-Bit ADC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	C	2/2