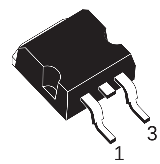
STB120NH03L

N-CHANNEL 30V - 0.005 Ω - 60A D²PAK
STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB120NH03L	30 V	<0.0055 Ω	60 A(#)

- TYPICAL R_{DS}(on) = 0.005 Ω @ 10 V
- $R_{DS(ON)}$ * Qg INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")



D²PAK
TO-263
(Suffix "T4")

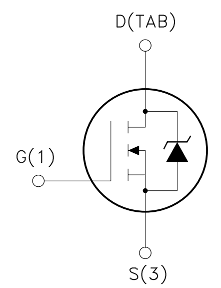
DESCRIPTION

The STB120NH03L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC-DC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB120NH03LT4	B120NH03L	TO-252	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 20	V
I_D(#)	Drain Current (continuous) at T_C = 25°C	60	A
I_D(#)	Drain Current (continuous) at T_C = 100°C	60	A
I_{DM}(•)	Drain Current (pulsed)	240	A
P_{tot}	Total Dissipation at T_C = 25°C	115	W
	Derating Factor	0.77	W/°C
E_{AS}(1)	Single Pulse Avalanche Energy	700	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.
(#) Value limited by wire bonding
(1) Starting T_j = 25 ºC, I_D = 30A, V_{DD} = 15V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.30	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.8	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 30 A V_{GS} = 5 V I_D = 30 A		0.005 0.006	0.0055 0.0105	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 10 V I_D = 30 A		40		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 15V f = 1 MHz V_{GS} = 0		4100 680 70		pF pF pF
R_G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.3		Ω

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 15 V I_D = 30 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		16 95		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V I_D=60A V_{GS}=10V		57 11.8 7.3	77	nC nC nC
Q_{oss}(1)	Output Charge	V_{DS}= 16 V V_{GS}= 0 V		27		nC
Q_{gls}(2)	Third-quadrant Gate Charge	V_{DS}< 0 V V_{GS}= 10 V		55		nC

SWITCHING OFF(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15 V I_D = 30 A R_G = 4.7Ω, V_{GS} = 10 V		48 23		ns ns

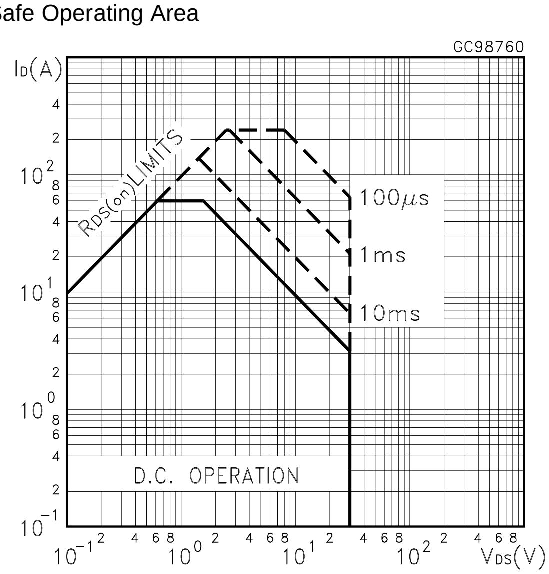
SOURCE DRAIN DIODE(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				60 240	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 30 A V_{GS} = 0			1.4	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 60 A di/dt = 100A/µs V_{DD} = 30 V T_j = 150°C (see test circuit, Figure 5)		46 64 2.8	62 86	ns nC A

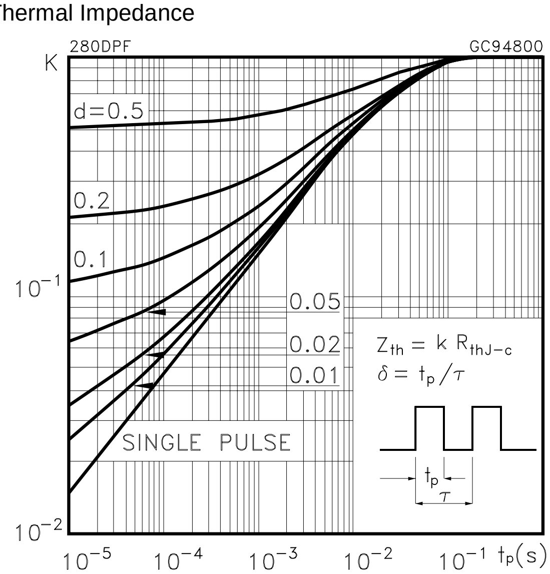
(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by T_{jmax}

(1) $Q_{oss} = C_{oss} * \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A
(2) Gate charge for synchronous operation

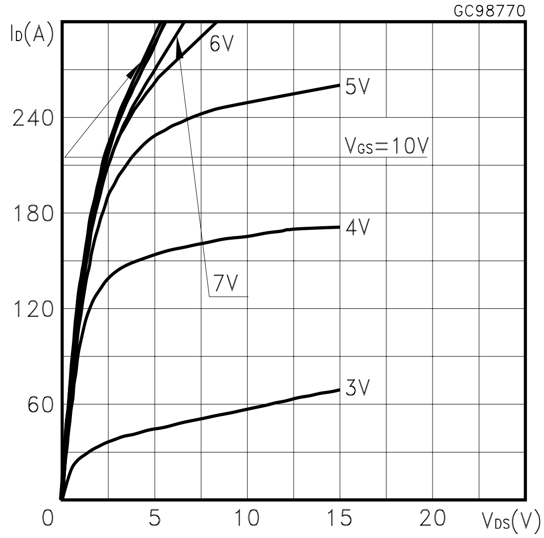
Safe Operating Area



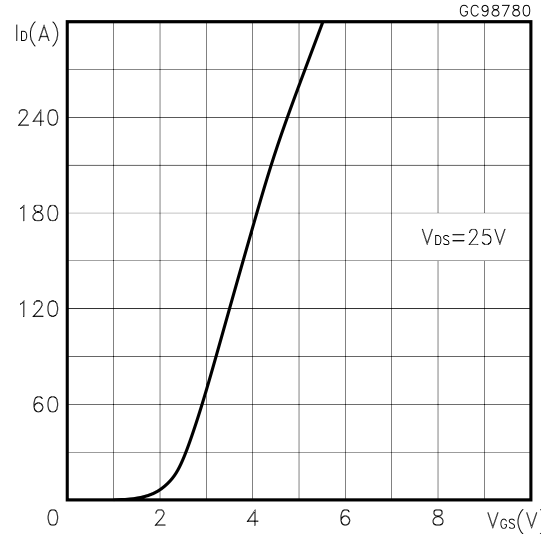
Thermal Impedance



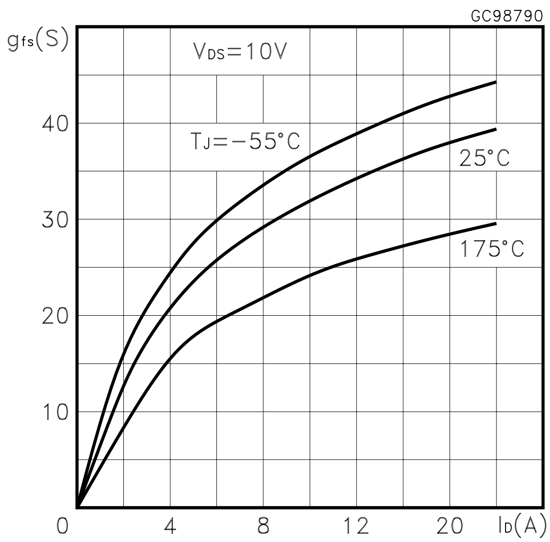
Output Characteristics



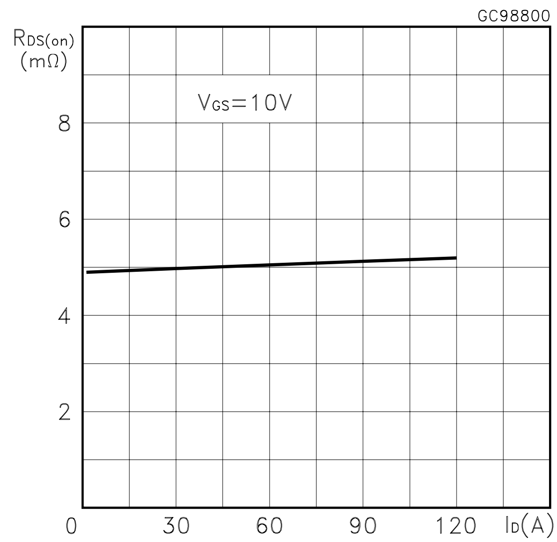
Transfer Characteristics



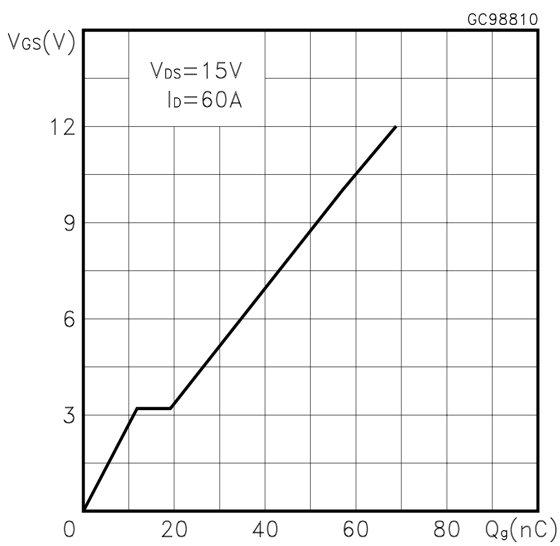
Transconductance



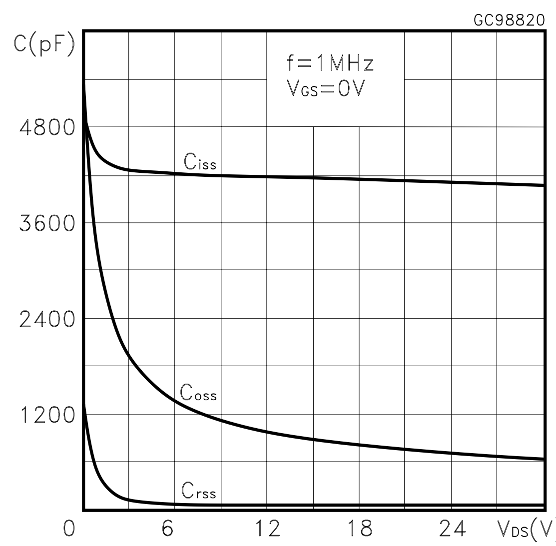
Static Drain-source On Resistance



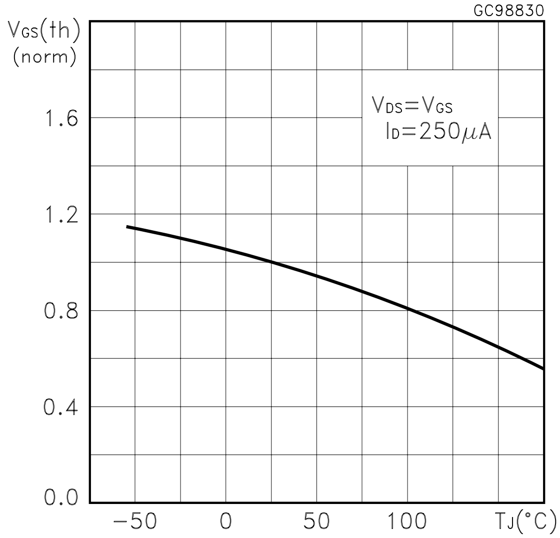
Gate Charge vs Gate-source Voltage



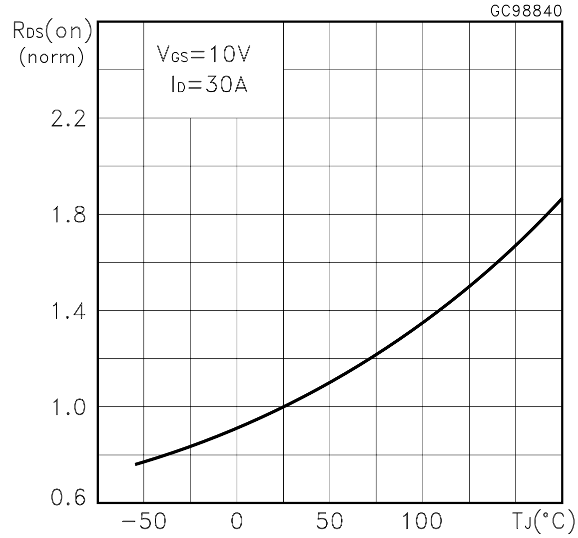
Capacitance Variations



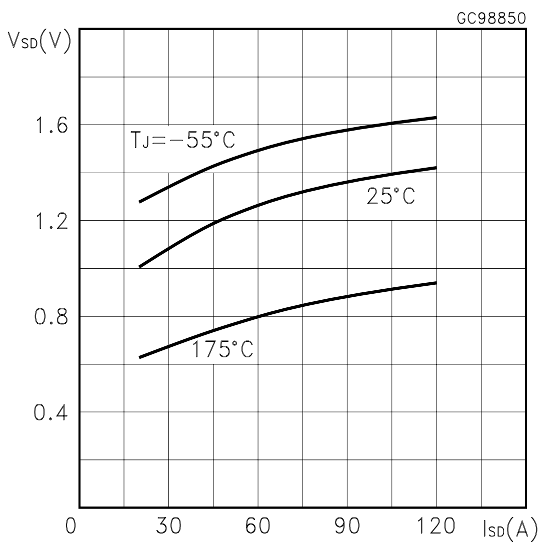
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

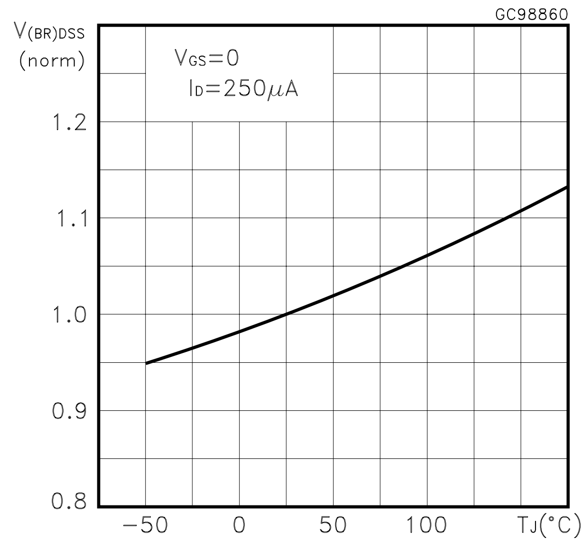


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Fig. 1: Unclamped Inductive Load Test Circuit

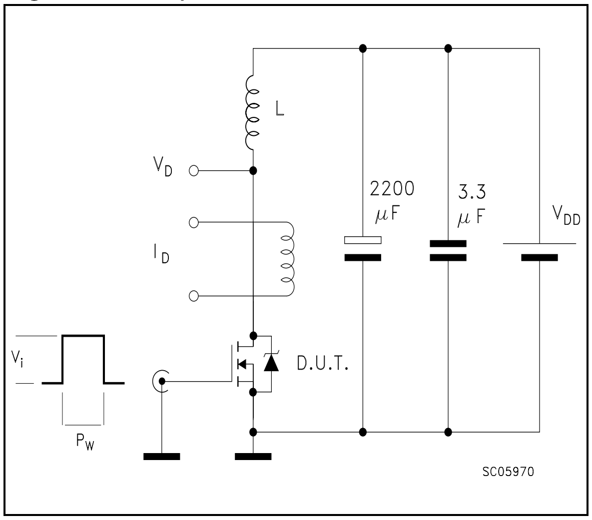


Fig. 2: Unclamped Inductive Waveform

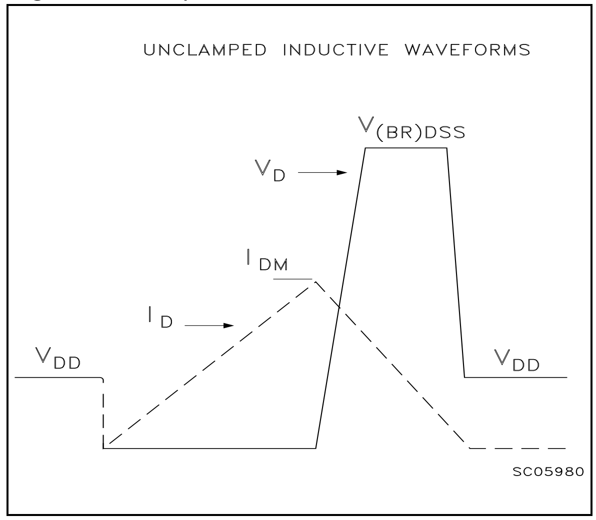


Fig. 3: Switching Times Test Circuits For Resistive Load

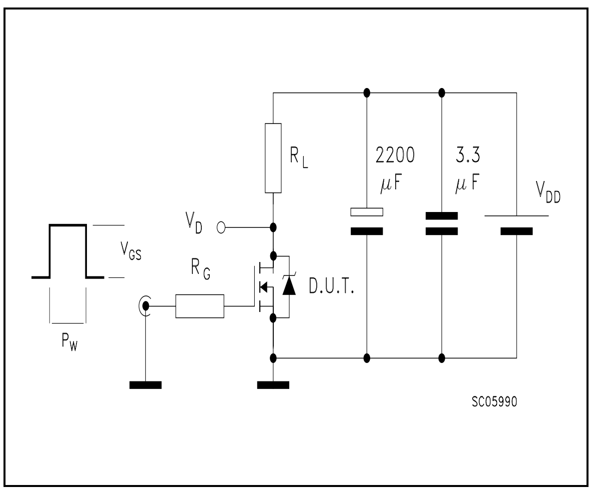


Fig. 4: Gate Charge test Circuit

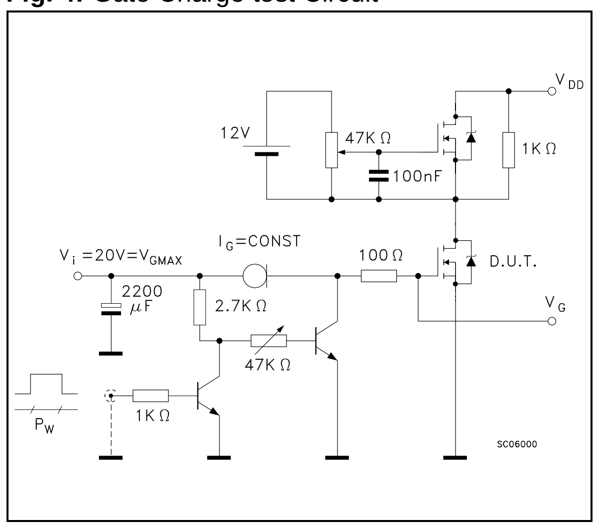
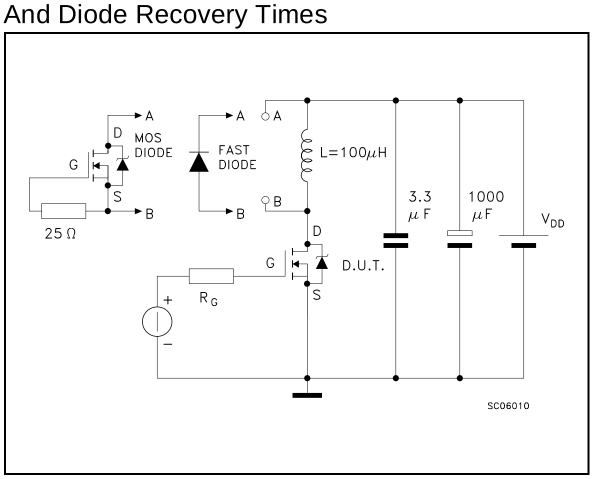
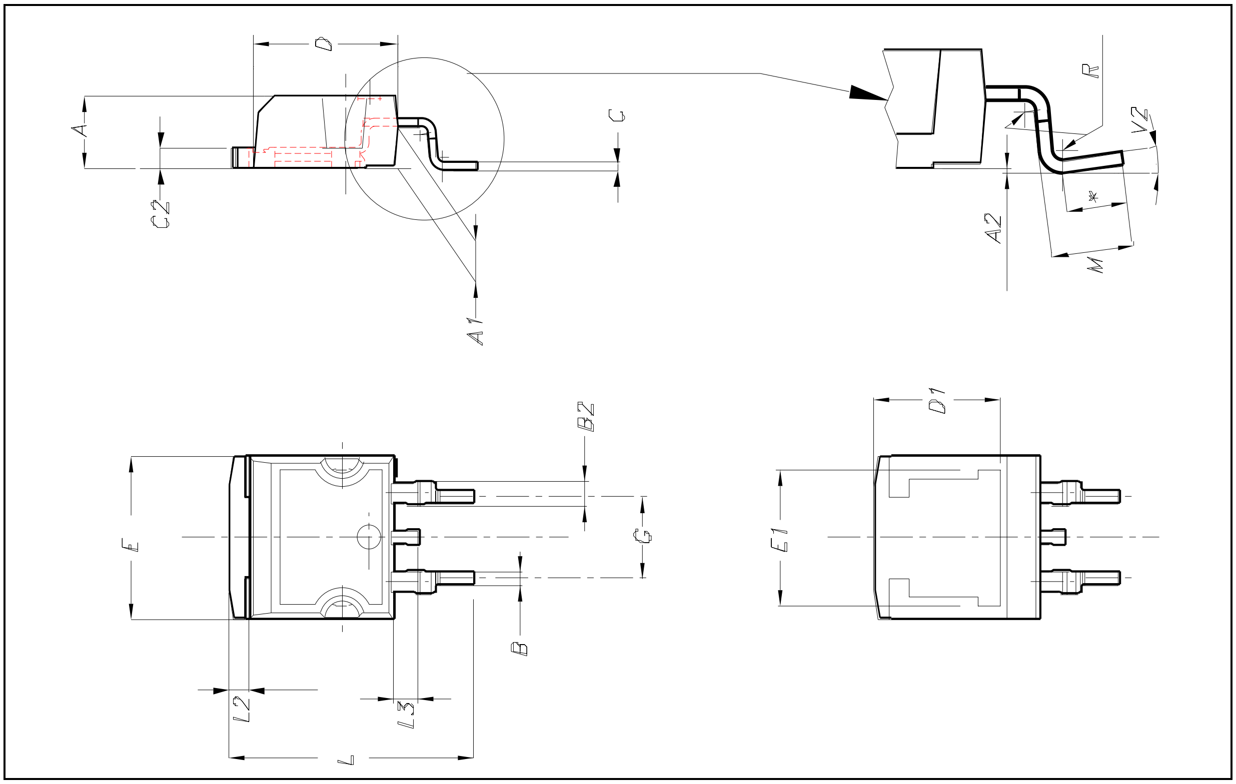


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

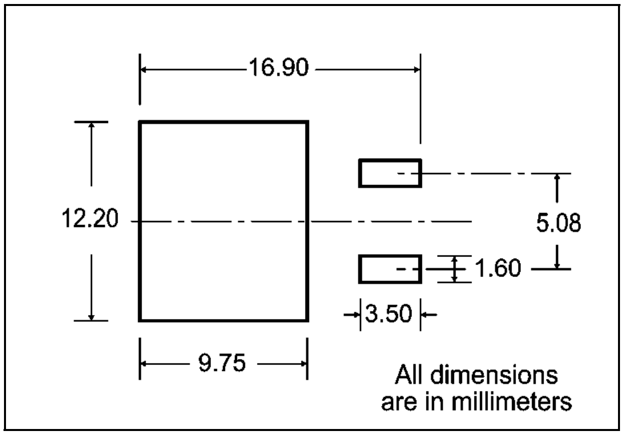


D^2PAK MECHANICAL DATA

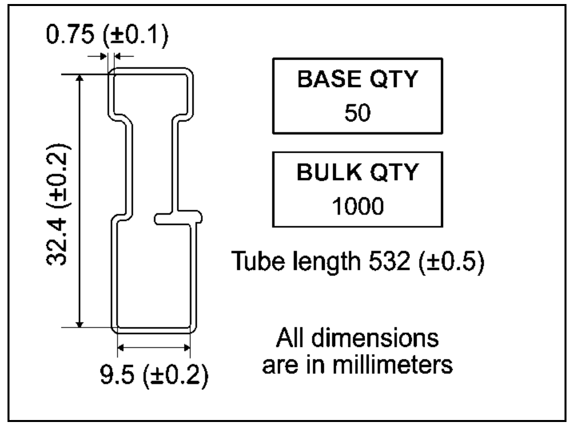
DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



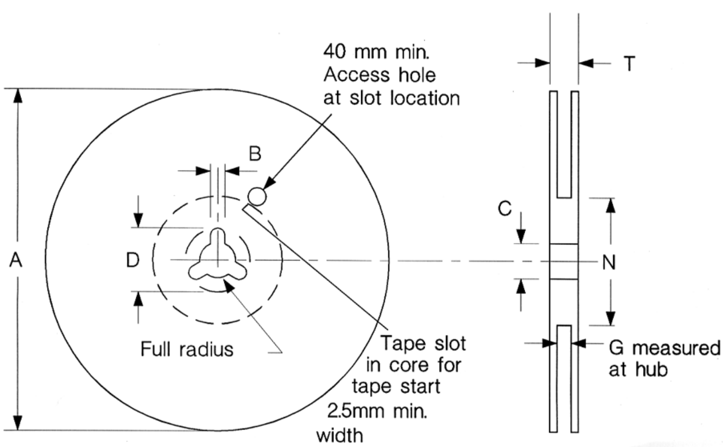
D^2PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix ”T4”)*



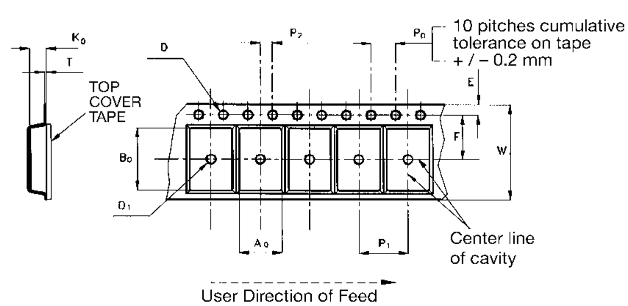
REEL MECHANICAL DATA

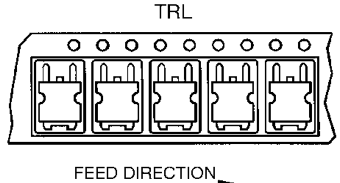
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

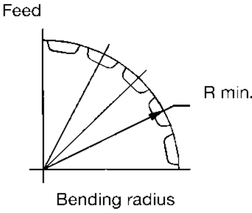
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0075	0.082
R	50		1.574	
T	0.25	0.35	.0.0098	0.0137
W	23.7	24.3	0.933	0.956

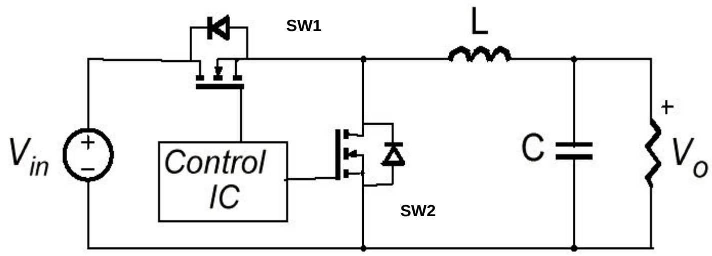






* on sales type

APPENDIX A
Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.
The low side (**SW2**) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW_1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (**SW1)** device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * d$	$R_{DS(on)SW2} * I_L^2 * (1-d)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	[1] $V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$\mathbf{Q_{gls(SW2)} * V_{gg} * f}$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

[1] Dissipated by SW1 during turn-on