Ordering number : ENN7002

N-Channel Silicon MOSFET

FTD2008

DC / DC Converter Applications

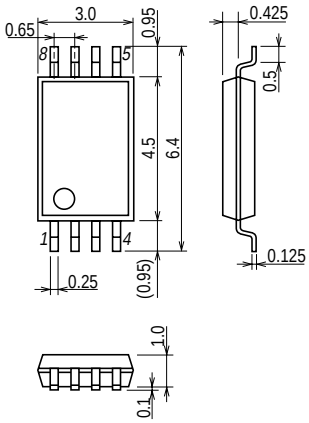
Features

- Low ON-resistance.
- 4V drive.
- Mounting height 1.1mm.
- Composite type, facilitating high-density mounting.

Package Dimensions

unit : mm
2155A

[FTD2008]



1 : Drain1
2 : Source1
3 : Source1
4 : Gate1
5 : Gate2
6 : Source2
7 : Source2
8 : Drain2

SANYO : TSSOP8

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		60	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		1.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	6	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (1000mm²×0.8mm) 1unit	0.8	W
Total Dissipation	P_T	Mounted on a ceramic board (1000mm²×0.8mm)	1.0	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.0		2.4	V
Forward Transfer Admittance	$\|yfs\|$	V_{DS}=10V, I_D=0.8A	1.4	2.0		S

Marking : D2008

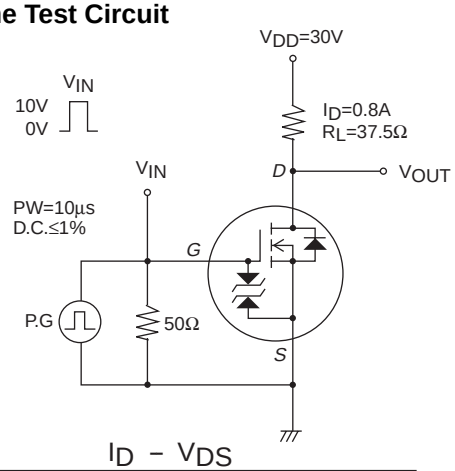
Continued on next page.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

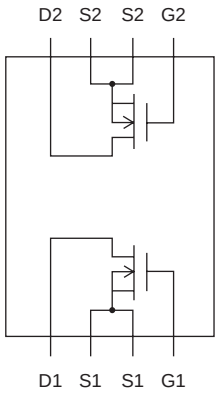
Continued from preceding page.

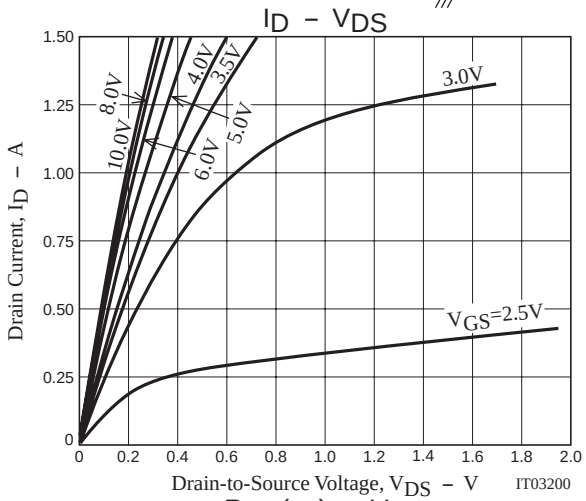
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=0.8A, V_{GS}=10V		240	320	mΩ
	$R_{DS}(on)2$	I_D=0.8A, V_{GS}=4V		320	440	mΩ
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		110		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		35		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		10		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit		7		ns
Rise Time	t_r	See specified Test Circuit		4		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit		24		ns
Fall Time	t_f	See specified Test Circuit		11		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_D=1.5A		4.5		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_D=1.5A		0.9		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_D=1.5A		0.8		nC
Diode Forward Voltage	V_{SD}	I_S=1.5A, V_{GS}=0		0.82	1.2	V

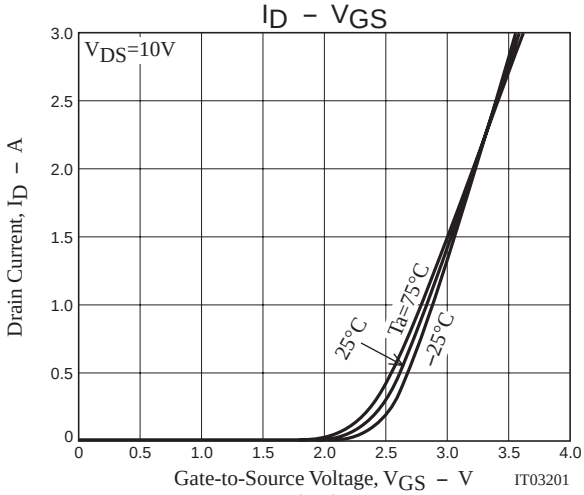
Switching Time Test Circuit

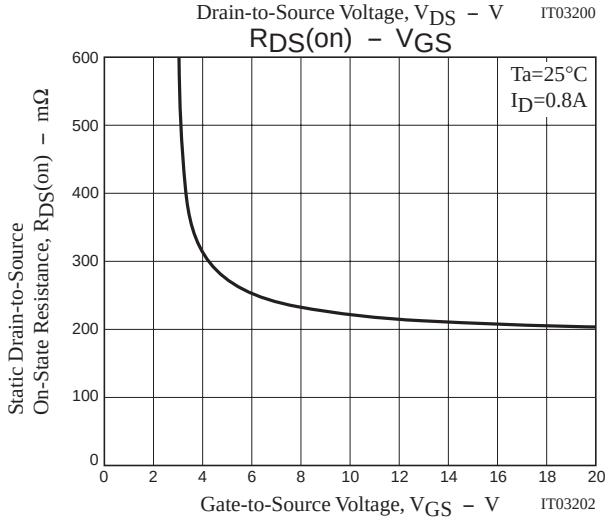


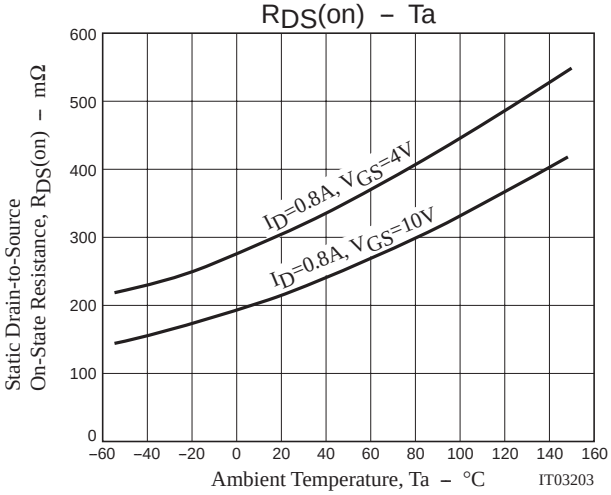
Electrical Connection

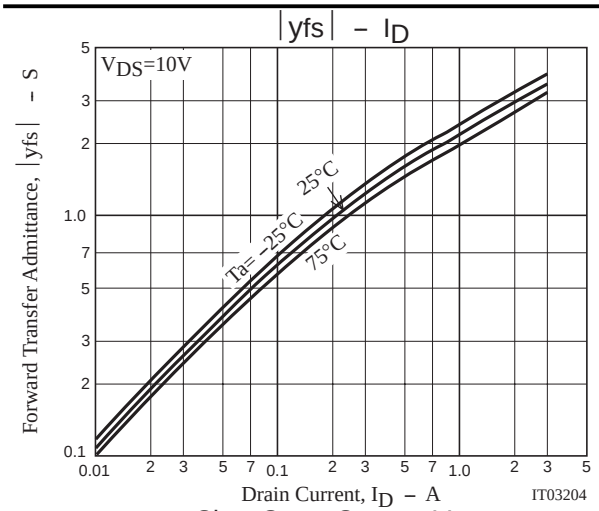


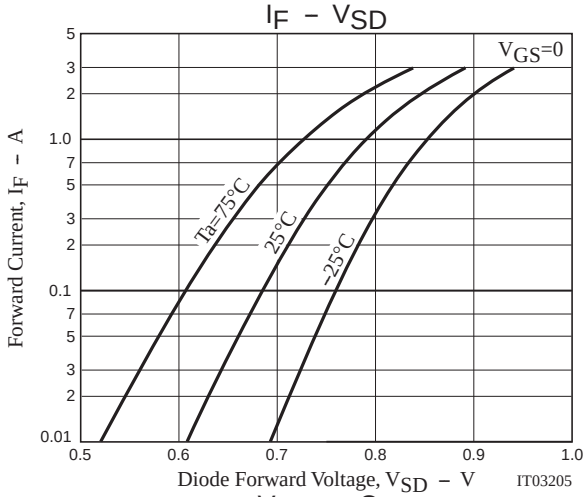


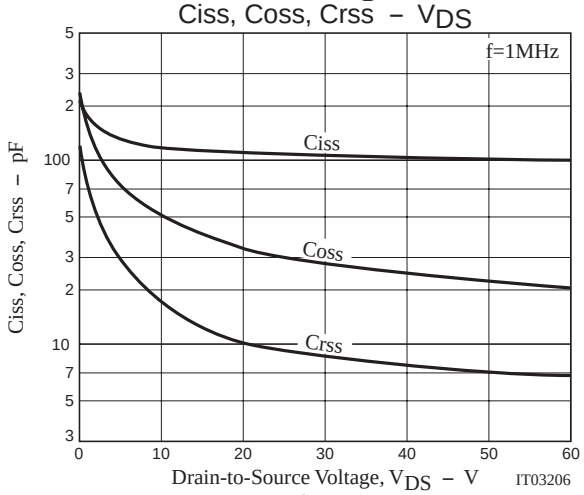


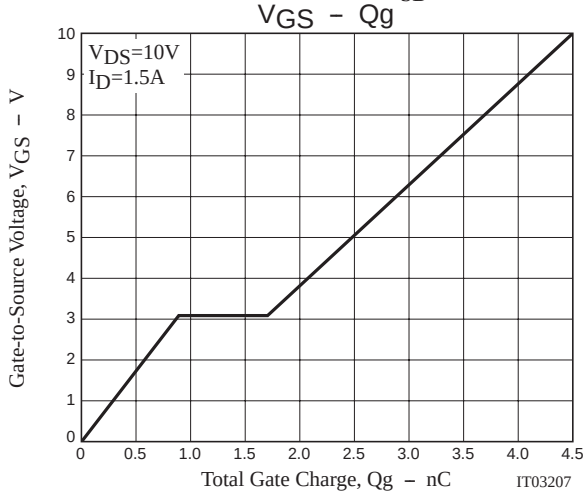


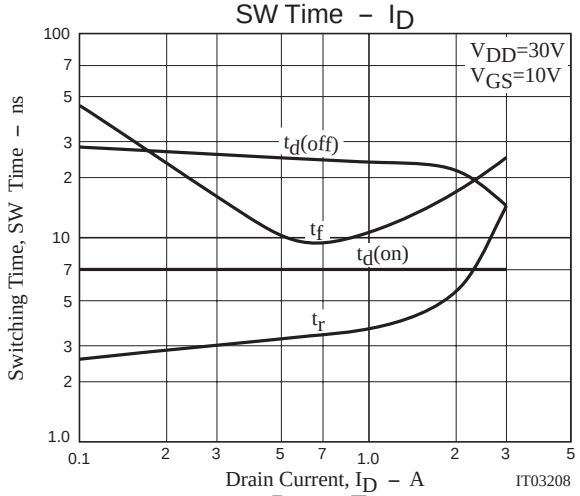


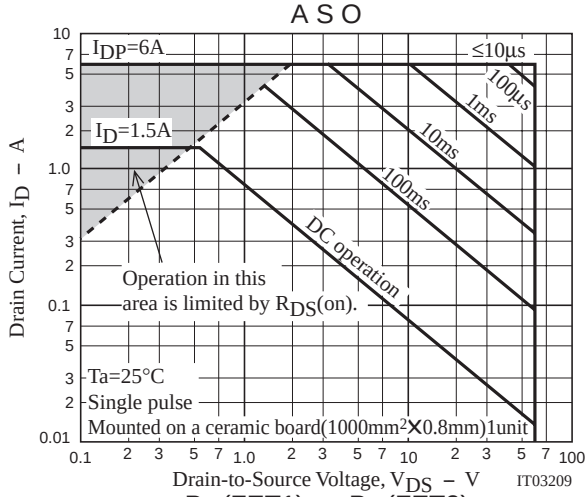

|yfs| – ID
VDS=10V
25°C
Ta=–25°C
75°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT03204

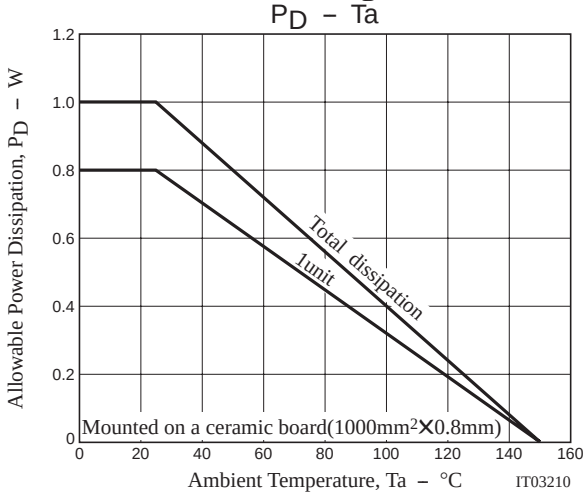

IF – VSD
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT03205

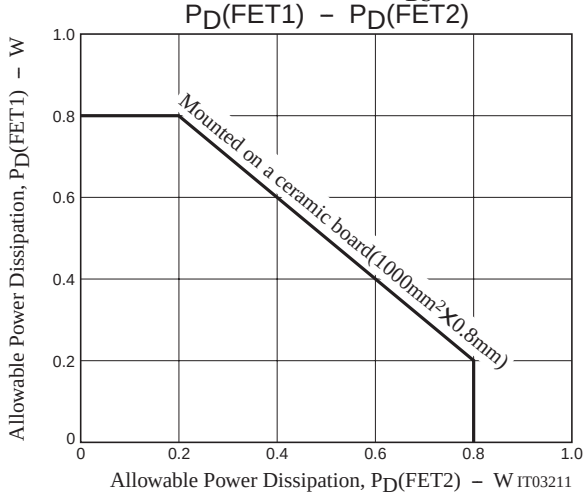

Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT03206


VGS – Qg
VDS=10V
ID=1.5A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT03207


SW Time – ID
VDD=30V
VGS=10V
td(off)
tf
td(on)
tr
Switching Time, SW Time – ns
Drain Current, ID – A
IT03208


A S O
IDP=6A
ID=1.5A
≤10µs
100µs
1ms
10ms
100ms
DC operation
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board(1000mm²×0.8mm)1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT03209


PD – Ta
Total dissipation
1unit
Mounted on a ceramic board(1000mm²×0.8mm)
Allowable Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT03210


PD(FET1) – PD(FET2)
Mounted on a ceramic board(1000mm²×0.8mm)
Allowable Power Dissipation, PD(FET1) – W
Allowable Power Dissipation, PD(FET2) – W
IT03211