

Document Title

1M x16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	August 22, 2000	Preliminary
0.1	Revise - Change package type : from FBGA to TBGA	November 21, 2000	Preliminary

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1M x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 1M x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output
- Package Type: 48-TBGA-9.00x12.00

GENERAL DESCRIPTION

The K6F1616U6M families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

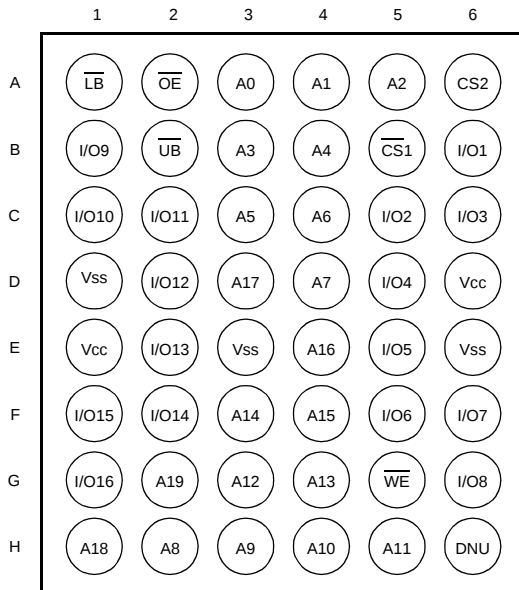
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Typ.)	Operating (Icc1, Max)	
K6F1616U6M-F	Industrial(-40~85°C)	2.7~3.3V	55 ¹⁾ /70ns	2μA	4mA	48-TBGA-9.00x12.00

1. The parameter is measured with 30pF test load.

2. Typical value are measured at Vcc=3.0V, TA=25°C and not 100% tested.

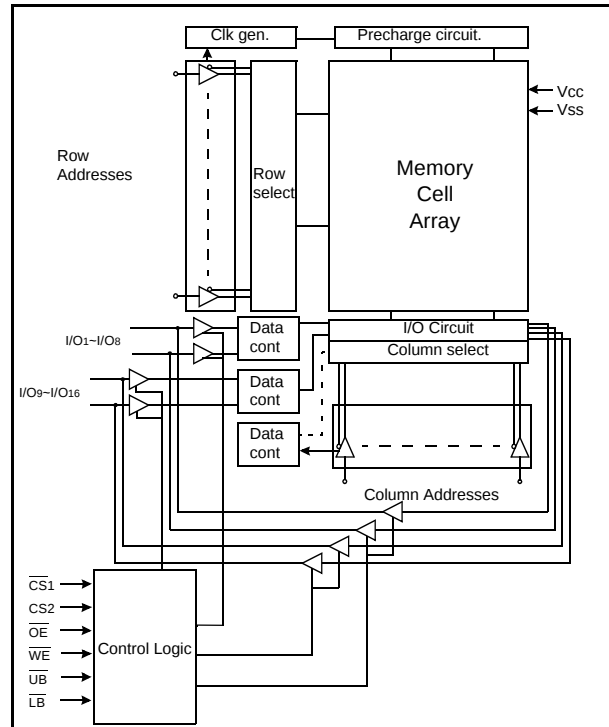
PIN DESCRIPTION



48-TBGA: Top View (Ball Down)

Name	Function	Name	Function
CS1, CS2	Chip Select Inputs	Vcc	Power
OE	Output Enable Input	Vss	Ground
WE	Write Enable Input	UB	Upper Byte(I/O9~16)
A0~A19	Address Inputs	LB	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F1616U6M-EF55	48-TBGA, 55ns, 3.0V
K6F1616U6M-EF70	48-TBGA, 70ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6	V
Power Dissipation	P _d	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.

3. Undershoot: -2.0V in case of pulse width ≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$, $CS_2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	70ns	-	-	35	mA
		55ns	-	-	40		
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V	
Standby Current (CMOS)	I _{SB1}	Other input =0~V _{CC} 1) $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ ($\overline{CS}_1$ controlled) or 2) $0V \leq \overline{CS}_2 \leq 0.2V$ (CS ₂ controlled) or $\overline{LB}=\overline{UB}$ 3) $\overline{LB}=\overline{UB} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ ($\overline{LB}/\overline{UB}$ controlled)	-	2.0	40	μA	

1. Typical value are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

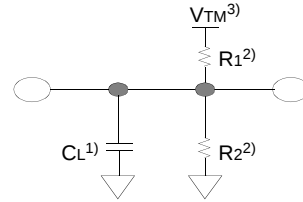
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=30\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

2. $R_1=3070\Omega$, $R_2=3150\Omega$ 3. $V_{TM}=2.8\text{V}$ AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.3\text{V}$, $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	ns
	Address access time	tAA	-	55	-	70	ns
	Chip select to output	tCO1, tCO2	-	55	-	70	ns
	Output enable to valid output	tOE	-	25	-	35	ns
	$\overline{LB}$, $\overline{UB}$ valid to data output	tBA	-	55	-	70	ns
	Chip select to low-Z output	tLZ1, tLZ2	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ enable to low-Z output	tBLZ	10	-	10	-	ns
	Output hold from address change	tOH	10	-	10	-	ns
	Chip disable to high-Z output	tHZ1, tHZ2	0	20	0	25	ns
	$\overline{OE}$ disable to high-Z output	tOHZ	0	20	0	25	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	tBHZ	0	20	0	25	ns
Write	Write cycle time	tWC	55	-	70	-	ns
	Chip select to end of write	tcw1, tcw2	45	-	60	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	ns
	Write pulse width	tWP	40	-	50	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	ns
	Data to write time overlap	tdW	25	-	30	-	ns
	Data hold from write time	tdH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to end of write	tBW	45	-	60	-	ns

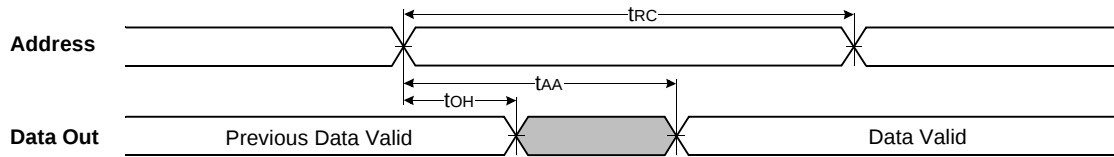
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$, $V_{IN} \geq 0\text{V}$	1.5	-	3.3	V
Data retention current	IDR	$V_{CC}=1.5\text{V}$, $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$, $V_{IN} \geq 0\text{V}$	-	1.0 ⁽²⁾	15	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

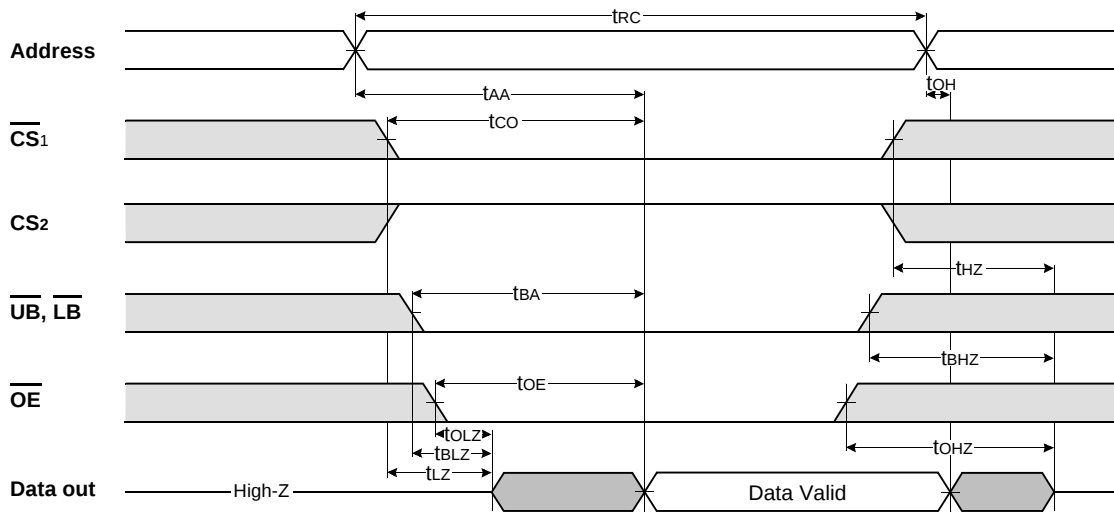
1. 1) $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, $CS_2 \geq V_{CC}-0.2\text{V}$ ($\overline{CS}_1$ controlled) or2) $0 \leq CS_2 \leq 0.2\text{V}$ (CS_2 controlled) or3) $\overline{LB}=\overline{UB} \geq V_{CC}-0.2\text{V}$, $CS_2 \geq V_{CC}-0.2\text{V}$ ($\overline{LB}/\overline{UB}$ controlled)2. Typical value are measured at $T_A=25^\circ\text{C}$ and not 100% tested.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)



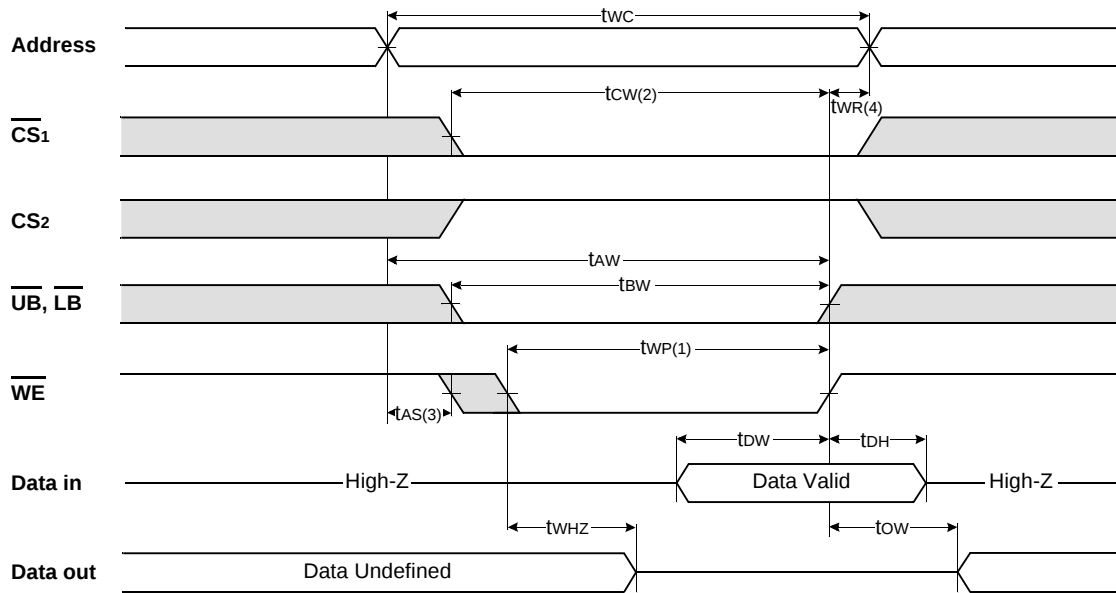
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



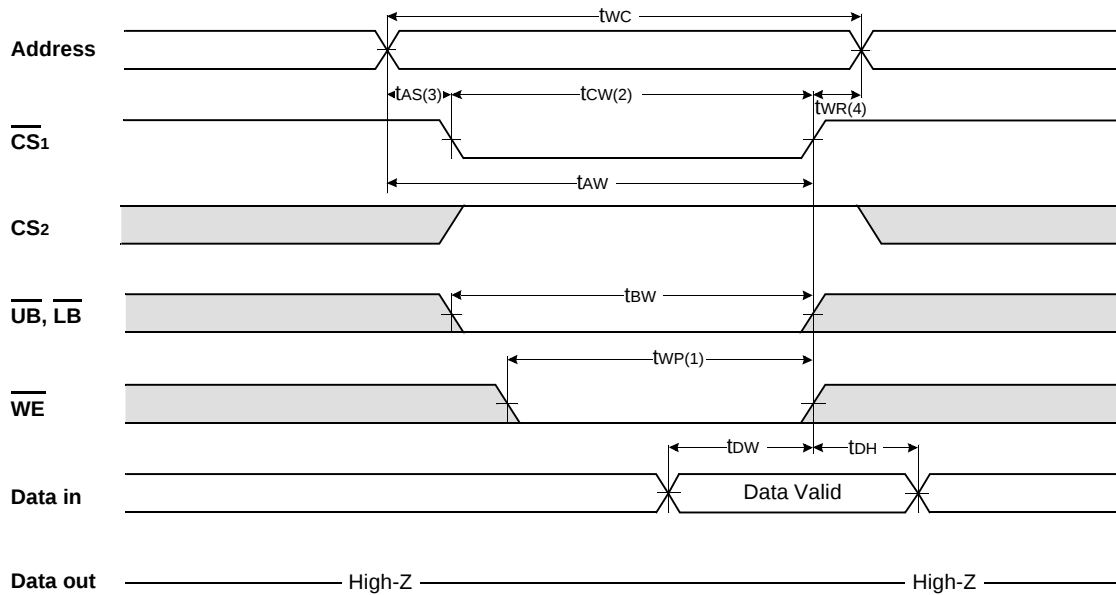
NOTES (READ CYCLE)

1. t_{thZ} and t_{tHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{thZ}(\text{Max.})$ is less than $t_{tHZ}(\text{Min.})$ both for a given device and from device to device interconnection.

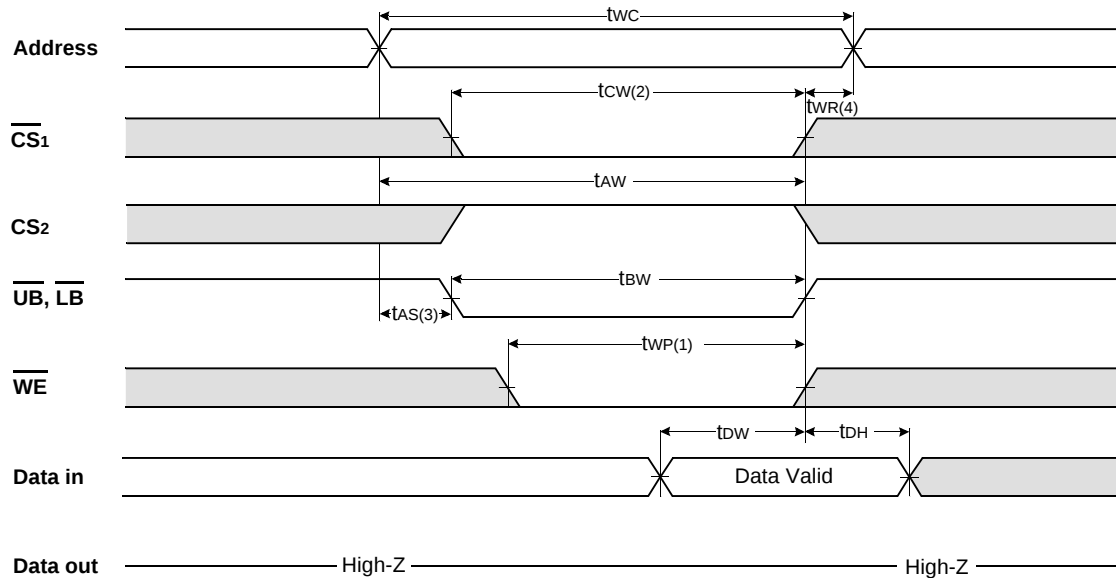
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{\text{WE}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{CS1}}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

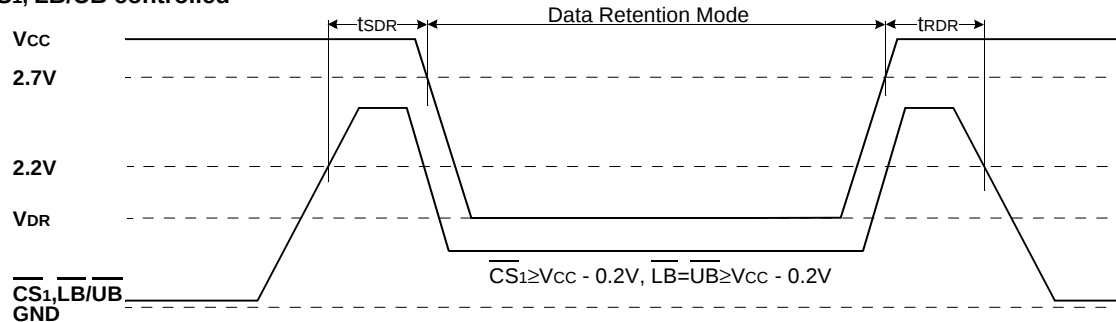


NOTES (WRITE CYCLE)

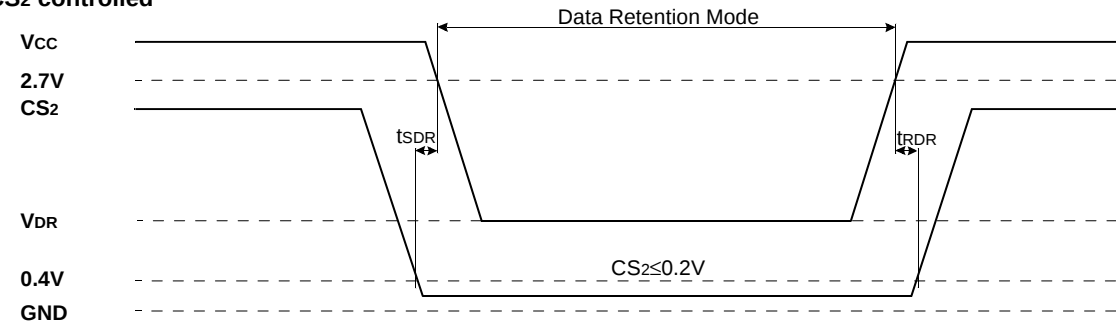
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low $\overline{WE}$. A write begins when $\overline{CS1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$, $\overline{LB}/\overline{UB}$ controlled



$\overline{CS2}$ controlled



PACKAGE DIMENSION

Unit: millimeters

48 BALL TAPE BALL GRID ARRAY(0.75mm ball pitch)

