

CFK0301

High Dynamic Range
Dual, Low-Noise GaAs FET



Product Specifications

April 1998

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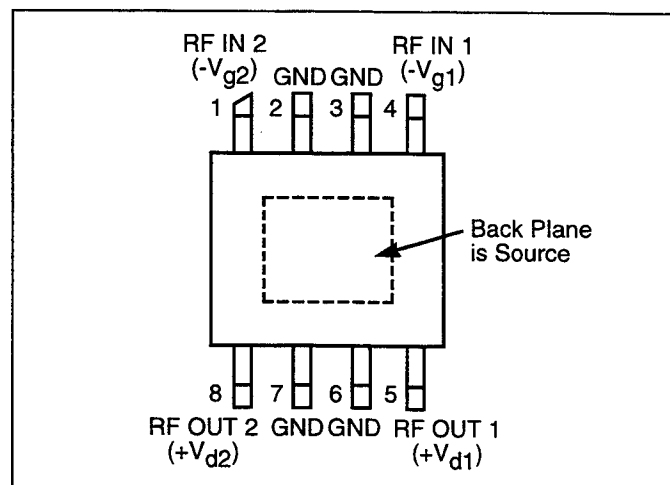
High Dynamic Range Dual, Low-Noise GaAs FET

Features

- ☐ Dual 600 μm GaAs FETs in a Single Package
- ☐ Guaranteed Low-Noise Figure: 0.8 to 2.0 GHz
- ☐ Excellent Gain and Phase Matching
- ☐ High Intercept Point
- ☐ Easily Matched for Low Noise Figure
- ☐ Surface Mount SO-8 Package

Applications

- ☐ Cellular Base Stations
- ☐ PCS Base Stations
- ☐ Industrial Data Networks



Description

Celeritek's CFK0301 contains two independent GaAs FETs in one surface-mount package. Each device is an 600 μm gate width and 1/4 μm gate length MESFET and provide low-noise figure and high intercept point. As the two GaAs FET die are selected from adjacent areas of the

processed wafer, they are matched in gain and phase.

The CFK0301 is suitable as balanced front-end FETs of a low-noise amplifier of base stations for PCS, Japanese PHS, AMPS, GSM and other communications systems.

The CFK0301 is packaged in a SO-8 package which is surface-mountable and available in tape and reel.

Electrical Specifications of a single GaAs FET (TA = 25°C, 2 GHz)

RF Characteristics (Celeritek 1.9 GHz test fixture ¹)		900 MHz			1.9 GHz			Units
Parameters	Conditions	Min	Typ	Max	Min	Typ	Max	
V_d = 4V, I_d = 30 mA								
Noise Figure			0.6			0.75	0.85	dB
Associated Gain	@ Noise Figure		22		15.5	16.5		dB
P _{out}	P ₋₁		17.5		17.5	18.5		dBm
IP ₃	+5 dBm P _{OUT} /Tone		27		27	28		dBm
I _d	@ P ₋₁ per FET		43			42		mA
V_d = 4V, I_d = 70 mA								
Noise Figure			0.6			0.8		dB
Associated Gain	@ Noise Figure		23.5			17.5		dB
P _{out}	P ₋₁		19.5			19		dBm
IP ₃	+5 dBm P _{OUT} /Tone		31			28		dBm
I _d	@ P ₋₁ per FET		72			71		mA
DC Characteristics								
Transconductance	V _{ds} = 2 V, V _{gs} = 0 V	70	140					mmho
Saturated Drain Current	V _{ds} = 2 V, V _{gs} = 0 V	120	150	180				mA
Pinchoff Voltages	V _{ds} = 2 V, I _{ds} = 1 mA	-2.5	-1.3	-0.5				V
Thermal Resistance ²	@ T _{case} = 150°C liquid crystal test		42					°C/W

Notes: 1. Input matched for low noise.

2. For both FETs.

Typical Noise Parameters ($V_{ds} = 4\text{ V}$, $I_{ds} = 30\text{ mA}$)

Frequency (GHz)	F_{min} (dB)	Gamma Opt		RN/50
		Mag	Ang	
0.6	0.3	0.9169	30	0.20
0.8	0.3	0.8840	33	0.19
1.0	0.4	0.8490	36	0.17
1.2	0.5	0.8390	40	0.18
1.4	0.5	0.7753	44	0.18
1.6	0.5	0.7419	47	0.17
1.8	0.6	0.7257	50	0.16
2.0	0.6	0.7120	53	0.16

Typical Performance

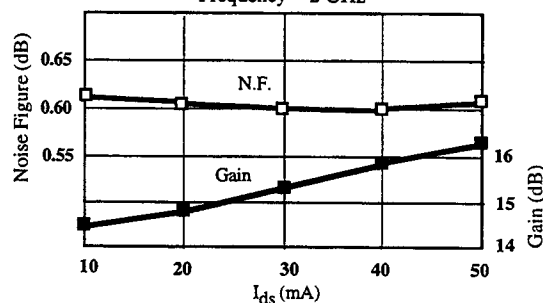
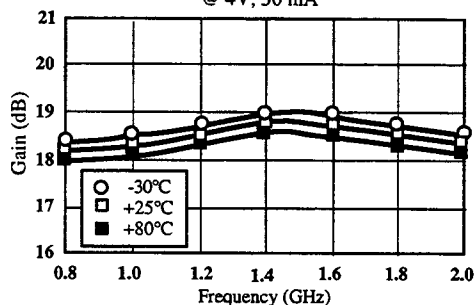
(In Celeritek PB-CFK0301-P3-00 Evaluation Board)

Absolute Maximum Ratings

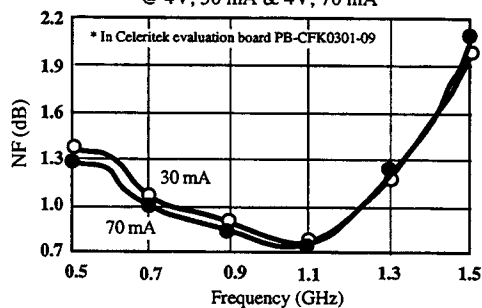
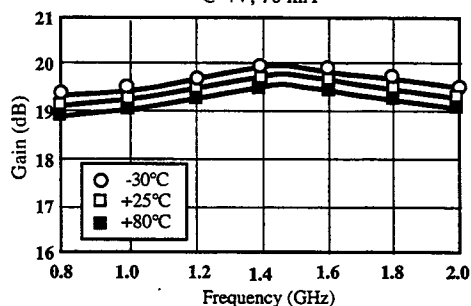
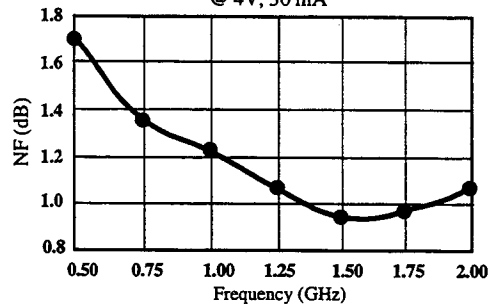
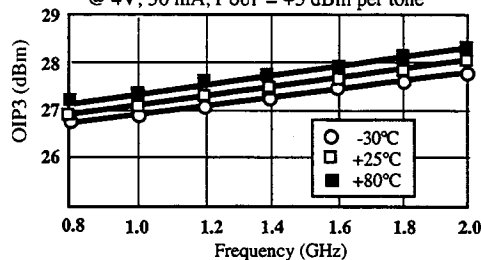
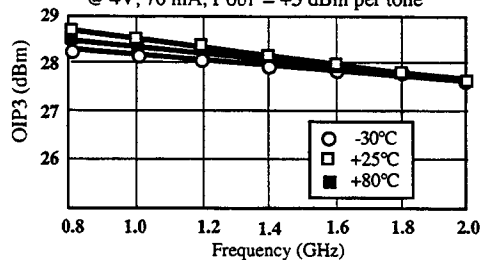
Parameter	Symbol	Rating
Drain-Source Voltage	V_{ds} 1, 2	+6V
Gate-Source Voltage	V_{gs} 1, 2	-4V
Drain Current of Each Device	I_{ds}	I_{dss}
Continuous Dissipation	P_t	1.5 W
Channel Temperature	T_{ch}	175°C
Storage Temperature	T_{stg}	-65°C to +150°C

Noise Figure & Gain vs I_{ds}

Frequency = 2 GHz

Gain vs Frequency Over Temperature
@ 4V, 30 mANoise Figure vs Frequency*
@ 4V, 30 mA & 4V, 70 mA

* In Celeritek evaluation board PB-CFK0301-09

Gain vs Frequency Over Temperature
@ 4V, 70 mANoise Figure vs Frequency
@ 4V, 30 mAOIP3 vs Frequency Over Temperature
@ 4V, 30 mA, $P_{out} = +5\text{ dBm}$ per toneOIP3 vs Frequency Over Temperature
@ 4V, 70 mA, $P_{out} = +5\text{ dBm}$ per tone

**Product Specifications - April 1998**

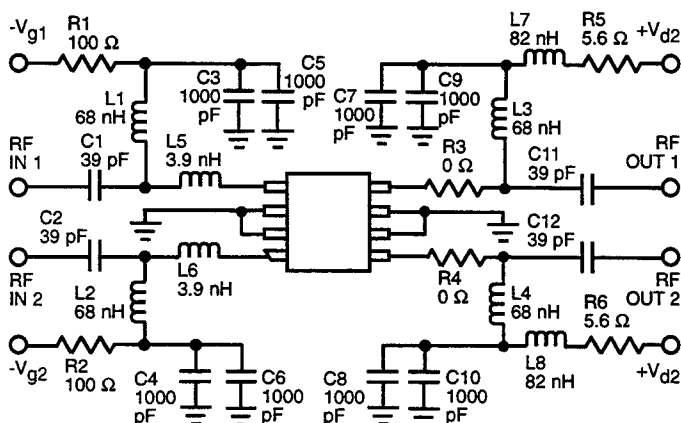
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Typical Scattering Parameters ($T_A = 25^\circ\text{C}$, $V_{DS} = 4\text{ V}$, $I_{DS} = 30\text{ mA}$) Information is available on disk.

Frequency (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag (dB)	Ang	MAG (dB)	ANG	MAG	ANG
0.5	0.99	-27.9	17.37	157.0	0.01	69.3	0.37	-22.3
0.7	0.98	-39.3	17.24	147.9	0.02	61.6	0.37	-31.4
0.8	0.98	-44.9	17.15	143.3	0.02	58.9	0.37	-36.1
0.9	0.97	-50.4	17.00	138.6	0.03	54.1	0.37	-40.4
1.0	0.97	-55.8	16.91	134.3	0.03	50.5	0.37	-44.7
1.3	0.96	-71.4	16.54	121.5	0.03	39.2	0.36	-57.6
1.5	0.95	-81.1	16.25	113.2	0.04	32.0	0.36	-65.7
1.8	0.93	-94.3	15.80	101.5	0.04	22.6	0.35	-76.8
1.9	0.92	-98.4	15.66	97.9	0.05	19.1	0.34	-80.5
2.0	0.91	-102.2	15.52	94.4	0.05	14.8	0.33	-83.4
2.5	0.87	-122.0	15.06	77.3	0.06	1.6	0.32	-99.7
3.0	0.86	-145.0	14.71	58.5	0.06	-13.1	0.31	-117.4
3.5	0.84	-131.9	14.03	40.4	0.07	-27.9	0.31	-129.4
4.0	0.85	68.8	13.07	24.8	0.07	-39.8	0.29	-136.6

Typical Scattering Parameters ($T_A = 25^\circ\text{C}$, $V_{DS} = 4\text{ V}$, $I_{DS} = 70\text{ mA}$) Information is available on disk.

Frequency (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag (dB)	Ang	MAG (dB)	ANG	MAG	ANG
0.5	0.99	-29.9	19.10	156.0	0.01	68.8	0.34	-22.2
0.7	0.98	-42.0	18.94	146.4	0.02	62.0	0.34	-31.3
0.8	0.98	-48.0	18.83	141.0	0.02	58.8	0.34	-36.1
0.9	0.97	-53.9	18.65	136.7	0.02	-54.3	0.33	-40.5
1.0	0.97	-59.5	18.54	132.3	0.02	50.3	0.33	-44.6
1.3	0.95	-75.9	18.13	119.2	0.03	39.4	0.33	-57.3
1.5	0.94	-85.9	17.78	110.7	0.03	32.1	0.32	-65.2
1.8	0.92	-99.7	17.28	98.9	0.03	22.8	0.31	-75.9
1.9	0.91	-104.0	17.13	95.1	0.04	20.0	0.31	-79.6
2.0	0.90	-107.8	16.95	91.7	0.04	15.0	0.30	-82.0
2.5	0.86	-128.4	16.42	74.1	0.04	2.7	0.28	-97.8
3.0	0.85	-152.1	15.96	55.3	0.05	-11.3	0.27	-114.7
3.5	0.82	-67.2	15.20	37.2	0.05	-25.0	0.28	-125.6
4.0	0.83	134.1	14.19	21.8	0.05	-36.0	0.26	-131.3

Test Circuit - 900 MHz**Evaluation Board Parts List**

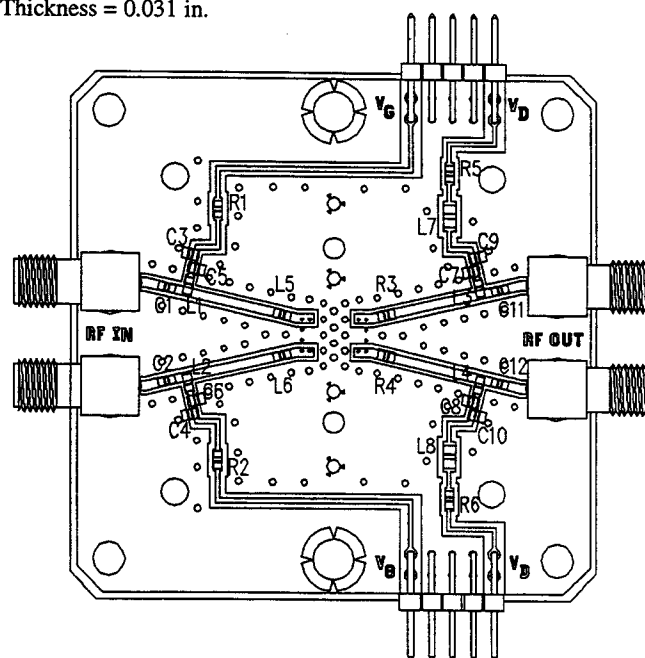
Item	Reference Designator	Description	Quantity
1	C1, C2, C11, C12	Capacitor, 39 pF	4
2	C3, C4, C5, C6, C7, C8, C9, C10	Capacitor, 1000 pF	8
3	R5, R6	Resistor, 5.6 Ω, 5%	2
4	R1, R2	Resistor, 100 Ω, 5%	2
5	L1, L2, L3, L4	Inductor, 68 nH	4
6	L5, L6	Inductor, 3.9 nH	2
7	L7, L8	Inductor, 82 nH	2
8	R3, R4	Resistor, 0 Ω	2

PB-CFK0301-P1-00 Evaluation Board

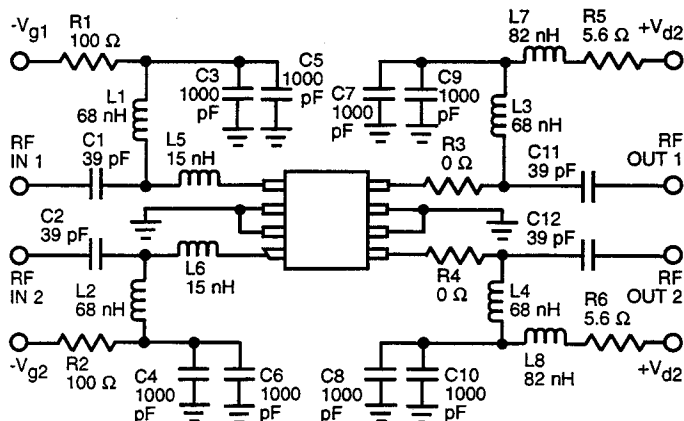
Evaluation Board Substrate:

ER = 4.65

Thickness = 0.031 in.



Test Circuit - 1.9 GHz



Evaluation Board Parts List

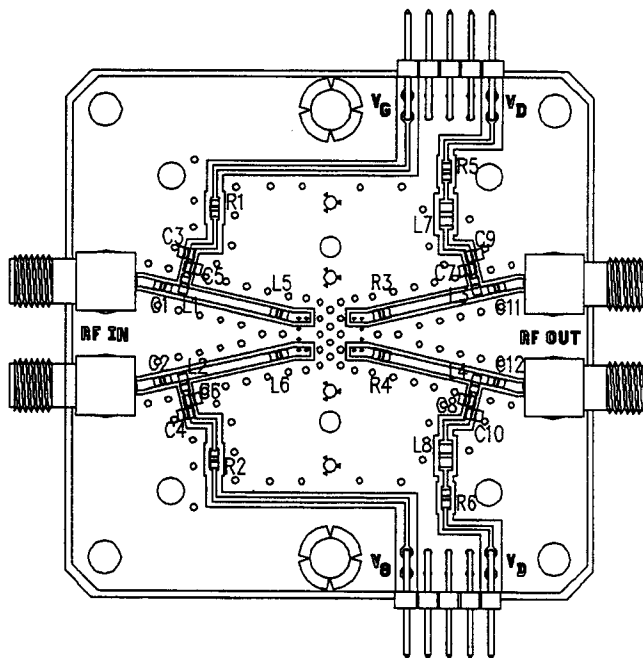
Item	Reference Designator	Description	Quantity
1	C1, C2, C11, C12	Capacitor, 39 pF	4
2	C3, C4, C5, C6, C7, C8, C9, C10	Capacitor, 1000 pF	8
3	R5, R6	Resistor, 5.6 Ω, 5%	2
4	R1, R2	Resistor, 100 Ω, 5%	2
5	L1, L2, L3, L4	Inductor, 68 nH	4
6	L5, L6	Inductor, 15 nH	2
7	L7, L8	Inductor, 82 nH	2
8	R3, R4	Resistor, 0 Ω	2

PB-CFK0301-P3-00 Evaluation Board

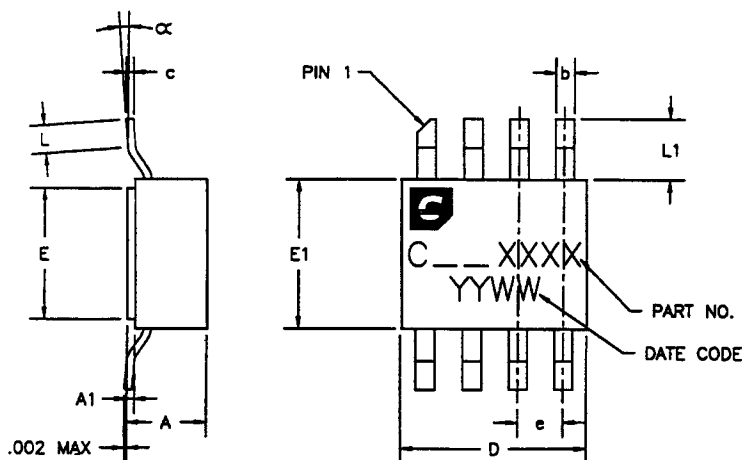
Evaluation Board Substrate:

ER = 4.65

Thickness = 0.031 in.



SO-8 Power Package Physical Dimensions



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A		.086[.0034]	.100[.0039]
A1	.005[.0002]	.008[.0003]	.011[.0004]
b	.017[.0007]	.020[.0008]	.023[.0009]
c	.007[.0003]	.008[.0003]	.009[.0004]
D	.195[.0077]	.200[.0079]	.205[.0081]
E	.135[.0053]	.140[.0055]	.145[.0057]
E1	.155[.0061]	.160[.0063]	.165[.0065]
e		.050[.0020]	
L	.020[.0009]		.040[.0016]
L1	.055[.0022]	.065[.0026]	.075[.0030]
α	0°		8°

DIMENSIONS IN INCHES

Ordering Information

The CFK0301GaAs FET is available in tape and reel. An evaluation board is also available. Ordering part numbers are listed.

Part Number for Ordering

Function

Package

CFK0301-AK-0000

Dual, Low-Noise high dynamic range FET

SO-8 package

CFK0301-AK-000T

900 MHz, Dual, Low-Noise high dynamic range FET

SO-8 package in tape and reel

PB-CFK0301-P1-000

900 MHz, Evaluation Board

PB-CFK0301-P3-000

1.9 GHz, Evaluation Board

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