13-BIT 210 MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

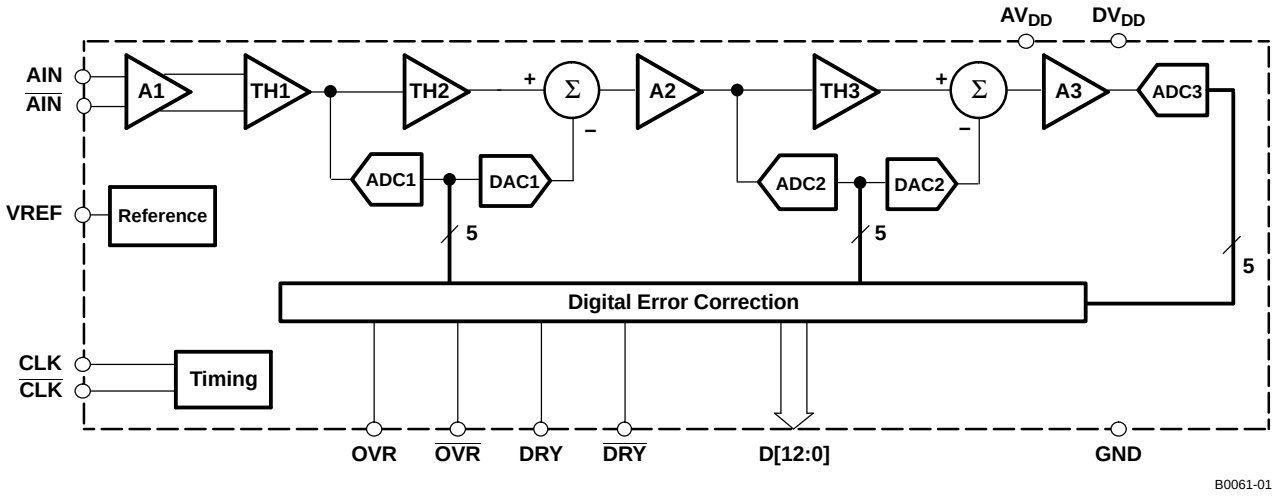
- 13-Bit Resolution
- 210 MSPS Sample Rate
- SNR = 69.1 dBc at 100-MHz IF and 210 MSPS
- SFDR = 81 dBc at 100-MHz IF and 210 MSPS
- SNR = 68.1 dBc at 230-MHz IF and 210 MSPS
- SFDR = 79 dBc at 230-MHz IF and 210 MSPS
- 2.2 V_{PP} Differential Input Voltage
- Fully Buffered Analog Inputs
- 5 V Analog Supply Voltage
- 3.3 V LVDS Compatible Outputs
- Total Power Dissipation: 2.0 W
- 2's Complement Output Format
- TQFP-80 PowerPAD™ package
- Industrial Temperature Range = –40°C to 85°C

APPLICATIONS

- Test and Measurement
- Software-Defined Radio
- Multi-channel Basestation Receivers
- Basestation TX Digital Predistortion
- Communication Instrumentation

DESCRIPTION

The ADS5440 is a 13-bit 210 MSPS analog-to-digital converter (ADC) that operates from a 5 V supply, while providing LVDS-compatible digital outputs from a 3.3 V supply. The ADS5440 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5440 has outstanding low noise and linearity over input frequency.



The ADS5440 is available in an 80-pin TQFP PowerPAD™ package. The ADS5440 is built on state of the art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full industrial temperature range (–40°C to 85°C).

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

Product	Package-Lead	Package Designator (1)	Specified Temperature Range	Package Marking	Ordering Number	Transport Media, Quantity
ADS5440	HTQFP-80(2) PowerPAD	PFP	–40°C to 85°C	ADS5440I	ADS5440IPFP	Tray, 96
					ADS5440IPFPR	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 7,5 mm x 7,5 mm (typ)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
Supply voltage	AV_{DD} to GND	6 V
	DRV_{DD} to GND	5 V
Analog input to GND		–0.3 V to AV_{DD}+0.3 V
Clock input to GND		–0.3 V to AV_{DD}+0.3 V
CLK to $\overline{CLK}$		±2.5
Digital data output to GND		–0.3 V to DRV_{DD}+0.3 V
Operating temperature range		–40°C to 85°C
Maximum junction temperature		150°C
Storage temperature range		–65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
θ_{JA}	Soldered slug, no airflow	21.7	°C/W
	Soldered slug, 250-LFPM airflow	15.4	°C/W
	Unsoldered slug, no airflow	50	°C/W
	Unsoldered slug, 250-LFPM airflow	43.4	°C/W
θ_{JC}	Bottom of package (heatslug)	2.99	°C/W

(1) Using 36 thermal vias (6 x 6 array). See the Application Section.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIES					
AV_{DD}	Analog supply voltage	4.75	5.0	5.25	V
DRV_{DD}	Output driver supply voltage	3.0	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
V_{CM}	Input common mode		2.4		V
CLOCK INPUT					
$1/t_C$	ADCLK input sample rate (sine wave)			210	MSPS
	Clock amplitude, differential sine wave		3		Vpp
	Clock duty cycle		50%		
T_A	Open free air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

MIN, TYP, and MAX values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 210 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			13		Bits
ANALOG INPUTS						
	Differential input range			2.2		V_{pp}
	Differential input resistance (DC)			1		kΩ
	Differential input capacitance			1.5		pF
	Analog input bandwidth			500		MHz
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
DYNAMIC ACCURACY						
	No missing codes			Tested		
DNL	Differential linearity error	f_{IN} = 10 MHz		±0.9		LSB
INL	Integral linearity error	f_{IN} = 10 MHz		±1.5		LSB
	Offset error		–5		5	mV
	Offset temperature coefficient					mV/°C
	Gain error		–5		5	%FS
	Gain temperature coefficient					Δ%/°C
	PSRR					mV/V
POWER SUPPLY						
I_{AVDD}	Analog supply current	V_{IN} = full scale, f_{IN} = 70 MHz, F_S = 210 MSPS		350		mA
I_{DRVDD}	Output buffer supply current			84		mA
	Power dissipation			2.0		W
	Power-up time			20		ms
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		69.5		dBc
		f_{IN} = 70 MHz		69.3		
		f_{IN} = 100 MHz		69.1		
		f_{IN} = 170 MHz		69.1		
		f_{IN} = 230 MHz		68.1		
		f_{IN} = 300 MHz		67.5		
		f_{IN} = 400 MHz		66.5		

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

MIN, TYP, and MAX values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 210 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz		88		dBc
		f_{IN} = 70 MHz		80		
		f_{IN} = 100 MHz		82		
		f_{IN} = 170 MHz		71		
		f_{IN} = 230 MHz		79		
		f_{IN} = 300 MHz		71		
		f_{IN} = 400 MHz		66		
HD2	Second harmonic	f_{IN} = 10 MHz		88		dBc
		f_{IN} = 70 MHz		83		
		f_{IN} = 100 MHz		82		
		f_{IN} = 170 MHz		71		
		f_{IN} = 230 MHz		79		
		f_{IN} = 300 MHz		74		
		f_{IN} = 400 MHz		75		
HD3	Third harmonic	f_{IN} = 10 MHz		90		dBc
		f_{IN} = 70 MHz		80		
		f_{IN} = 100 MHz		86		
		f_{IN} = 170 MHz		75		
		f_{IN} = 230 MHz		85		
		f_{IN} = 300 MHz		72		
		f_{IN} = 400 MHz		66		
	Worst other harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 70 MHz		95		
		f_{IN} = 100 MHz		90		
		f_{IN} = 170 MHz		89		
		f_{IN} = 230 MHz		85		
		f_{IN} = 300 MHz		93		
		f_{IN} = 400 MHz		70		
	SINAD	f_{IN} = 10 MHz		69.4		dBc
		f_{IN} = 70 MHz		68.8		
		f_{IN} = 100 MHz		68.6		
		f_{IN} = 170 MHz		65.8		
		f_{IN} = 230 MHz		67.4		
		f_{IN} = 300 MHz		65.4		
		f_{IN} = 400 MHz		61.6		
ENOB	Effective number of bits	f_{IN} = 70 MHz		11		Bits
	RMS idle channel noise	Inputs tied to common-mode		0.4		LSB
DIGITAL CHARACTERISTICS – LVDS DIGITAL OUTPUTS						
	Differential output voltage			0.35		V
	Output offset voltage		1.125		1.375	V

PRODUCT PREVIEW

TIMING CHARACTERISTICS

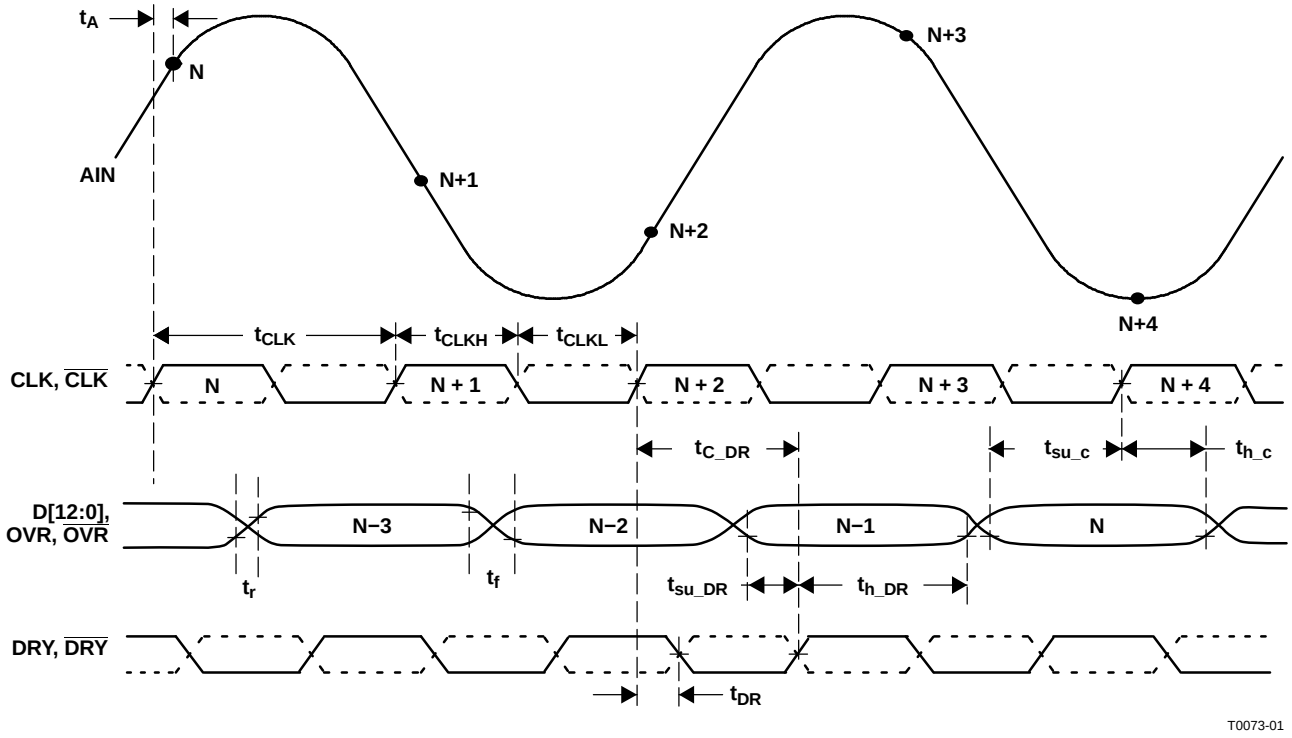


Figure 1. Timing Diagram

TIMING CHARACTERISTICS

over full temperature range, 50% clock duty cycle, sampling rate = 210 MSPS, AV_{DD} = 5 V, DRV_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay					ps
t_J	Clock slope independent aperture uncertainty (jitter)					fs
k_J	Clock slope jitter factor dependency					s/V
	Latency			4		cycles
Clock Input						
t_{CLK}	Clock period			4.76		ns
t_{CLKH}	Clock pulsewidth high			2.38		ns
t_{CLKL}	Clock pulsewidth low			2.38		ns
Clock to DataReady (DRY)						
t_{DR}	Clock rising to DataReady falling			3.06		ns
t_{C_DR}	Clock rising to DataReady rising	Clock duty cycle = 50% (1)		5.44		ns
Clock to DATA, OVR (2)						
t_r	Data V_{OL} to Data V_{OH} (rise time)					ns
t_f	Data V_{OH} to Data V_{OL} (fall time)					ns
t_{su_c}	Data valid to clock (setup time)			0.64		ns
t_{h_c}	Clock to invalid Data (hold time)			4.39		ns
DataReady (DRY)/DATA, OVR (2)						
$t_{su(DR)}$	Data valid to DRY			2.42		ns

(1) $t_{C\_DR} = t_{DR} + t_{CLKH}$ for clock duty cycles other than 50%
(2) Data is updated with clock rising edge or DRY falling edge.

PRODUCT PREVIEW

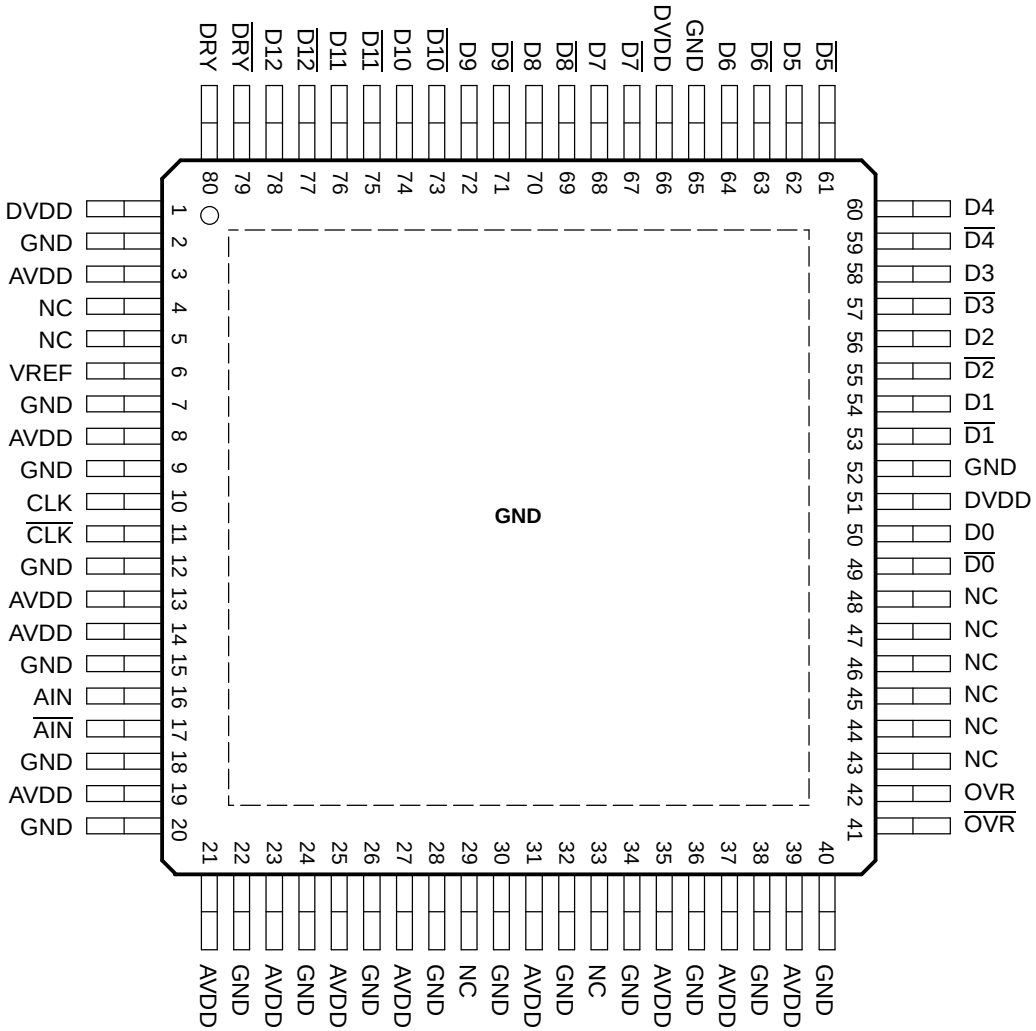
TIMING CHARACTERISTICS (continued)

over full temperature range, 50% clock duty cycle, sampling rate = 210 MSPS, AV_{DD} = 5 V, DRV_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{h(DR)}$	DRY to invalid Data			1.33		ns

DEVICE INFORMATION

PFP PACKAGE
(TOP VIEW)



P0027-01

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AVDD	3, 8, 13, 14, 19, 21, 23, 25, 27, 31, 35, 37, 39	Analog power supply
DVDD	1, 51, 66	Output driver power supply

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
GND	2, 7, 9, 12, 15, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 52, 65	Ground
VREF	6	Reference voltage
CLK	10	Differential input clock (positive). Conversion initiated on rising edge
$\overline{CLK}$	11	Differential input clock (negative)
AIN	16	Differential input signal (positive)
$\overline{AIN}$	17	Differential input signal (negative)
OVR, $\overline{OVR}$	42, 41	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, $\overline{D0}$	50, 49	LVDS digital output pair
D1–D6, $\overline{D1}$–$\overline{D6}$	53–64	LVDS digital output pairs
D7–D11, $\overline{D7}$–$\overline{D11}$	67–76	LVDS digital output pairs
D12, $\overline{D12}$	78, 77	LVDS digital output pair, most-significant bit (MSB
DRY, $\overline{DRY}$	80, 79	Data ready LVDS output pair
NC	4, 5, 29, 33, 43–48	No connect

DEFINITION OF SPECIFICATIONS

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL) The INL is the deviation of the ADCs transfer function from a best fit line determined by a least squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best fit line, measured in units of LSB.

Gain Error The gain error is the deviation of the ADCs actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by T_{MIN}– T_{MAX}.

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

PRODUCT PREVIEW

DEFINITION OF SPECIFICATIONS (continued)

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Resolution Bandwidth The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10} \frac{P_S}{P_D} \quad (3)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

TYPICAL CHARACTERISTICS

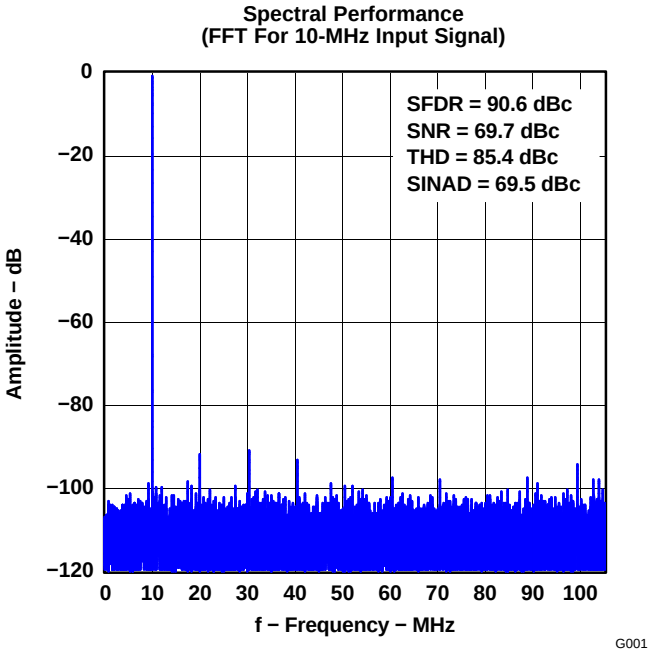


Figure 2.

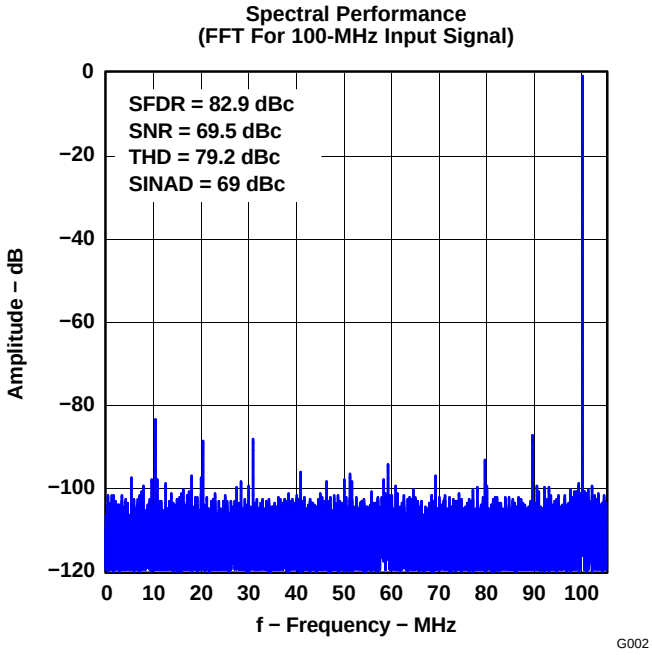


Figure 3.

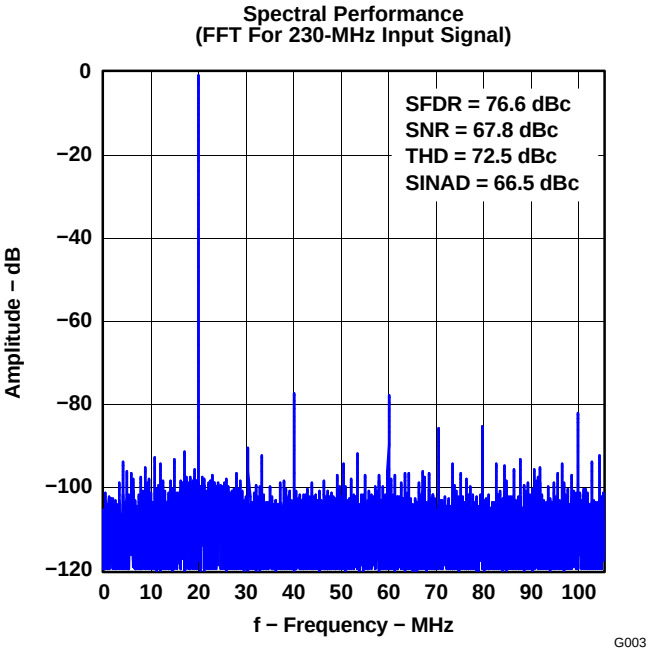


Figure 4.

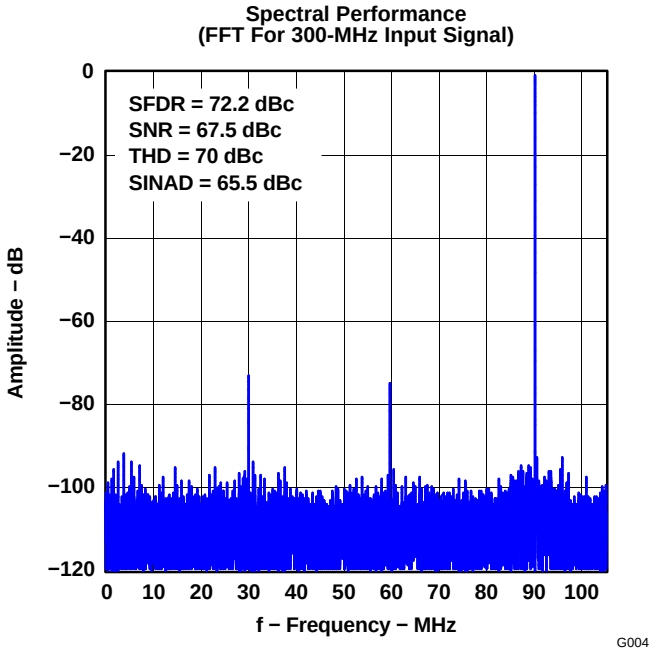
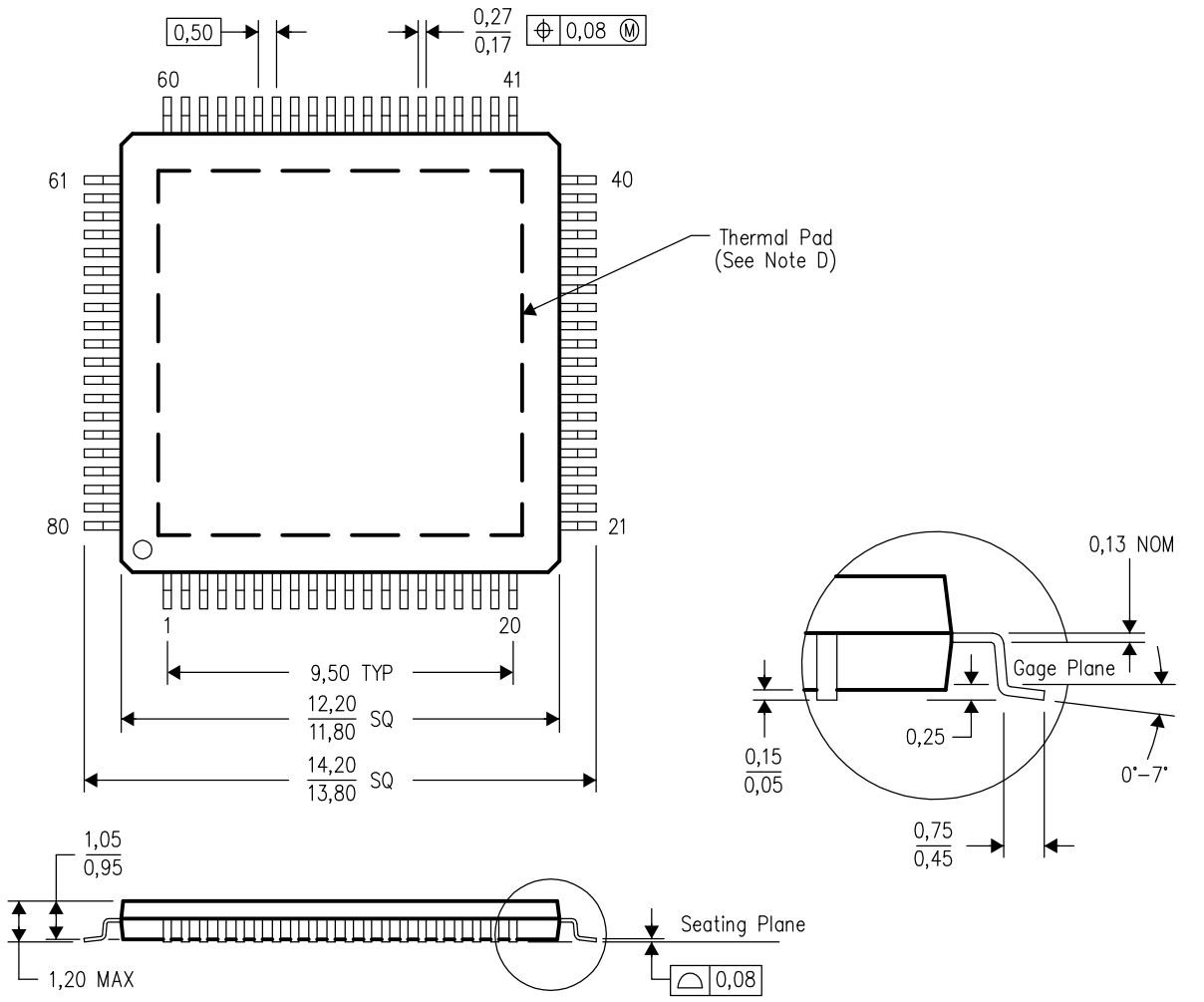


Figure 5.

PRODUCT PREVIEW

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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