



N- and P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

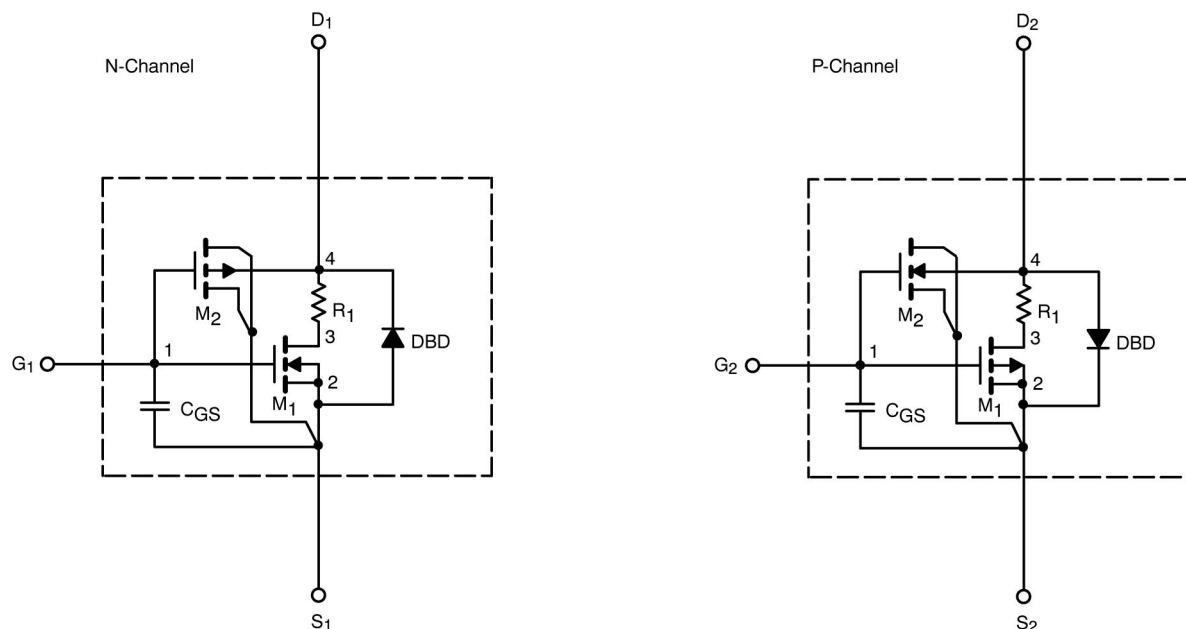
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _j = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions		Simulated Data	Measured Data	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.8		V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	2.2		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	110		A
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	62		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.9 A	N-Ch	0.042	0.044	Ω
		V _{GS} = -10 V, I _D = -3.9 A	P-Ch	0.071	0.062	
		V _{GS} = 4.5 V, I _D = 4.1 A	N-Ch	0.057	0.062	
		V _{GS} = -4.5 V, I _D = -3 A	P-Ch	0.120	0.105	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.9 A	N-Ch	9.2	11	S
		V _{DS} = -15 V, I _D = -2.5 A	P-Ch	5	5	
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch	0.70	0.80	V
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch	-0.80	-0.82	
Dynamic ^b						
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 4.9 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -3.9 A	N-Ch	7.4	8	Nc
Gate-Source Charge	Q _{gs}		P-Ch	9.6	10	
			N-Ch	1.4	1.4	
Gate-Drain Charge	Q _{gd}		P-Ch	2	2	
			N-Ch	1.2	1.2	
			P-Ch	1.9	1.9	
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} =10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch	8	12	Ns
			P-Ch	12	8	
Rise Time	t _r		N-Ch	10	10	
			P-Ch	14	9	
Turn-Off Delay Time	t _{d(off)}		N-Ch	13	23	
			P-Ch	16	21	
Fall Time	t _f		N-Ch	17	8	
			P-Ch	22	10	
Source-Drain Reverse Recovery Time	t _{rr}	I _S = 1.7 A, di/dt = 100 A/μs	N-Ch	24	25	
		I _S = -1.7 A, di/dt = 100 A/μs	P-Ch	30	27	

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2.

b. Guaranteed by design, not subject to production testing.

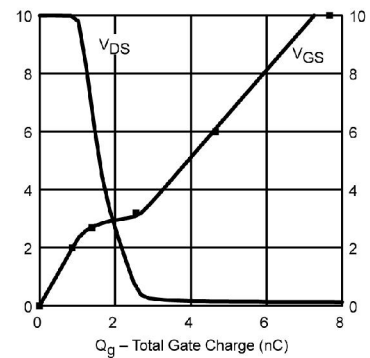
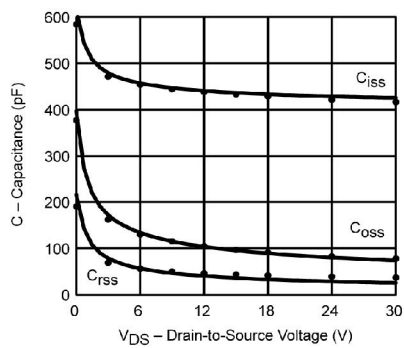
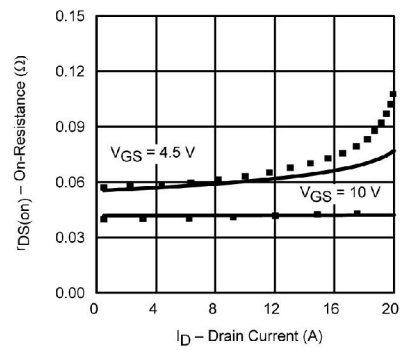
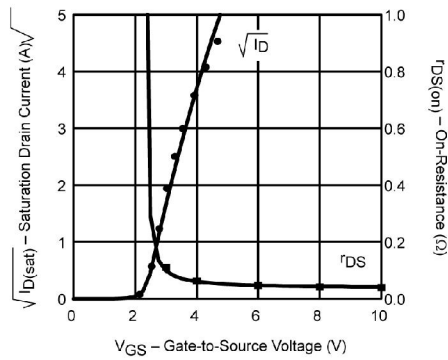
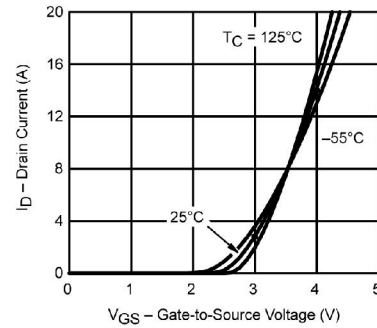
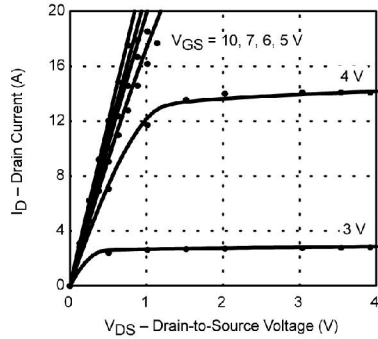


SPICE Device Model Si4532ADY

Vishay Siliconix

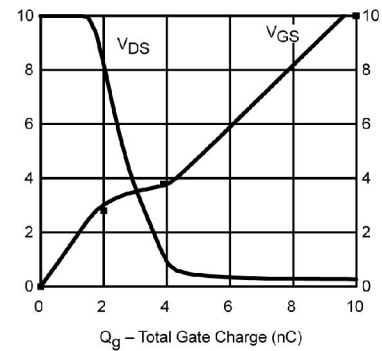
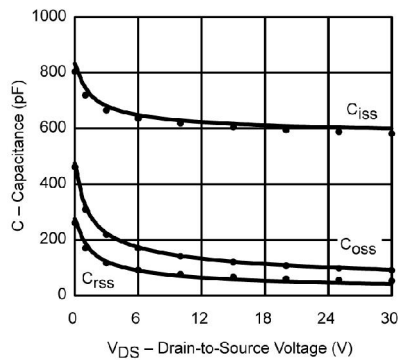
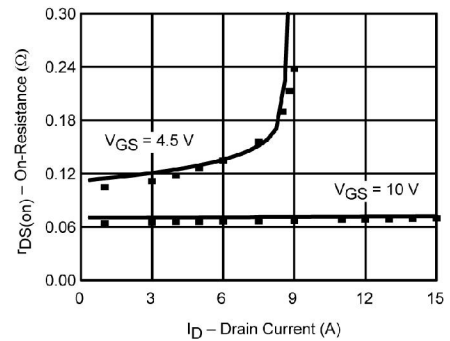
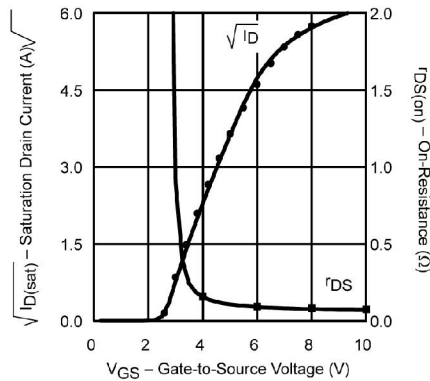
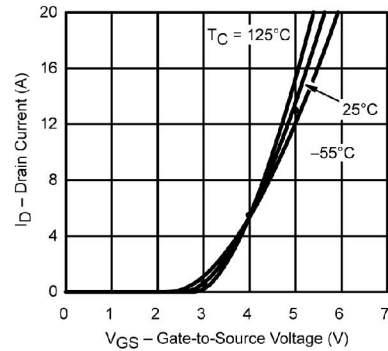
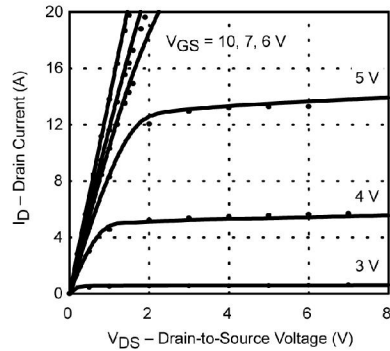
COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



Note: Dots and squares represent measured data.

P-Channel MOSFET



Note: Dots and squares represent measured data.