

TC74AC390P, TC74AC390F, TC74AC390FN

DUAL DECADE COUNTER

The TC74AC390 is an advanced high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

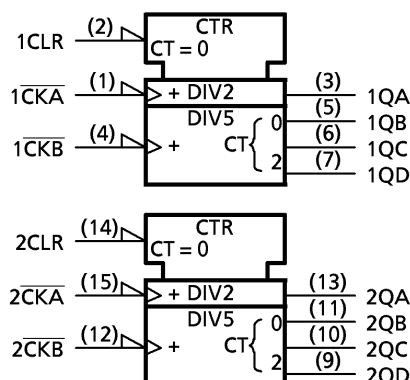
It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A ($\overline{\text{CKA}}$). The divided-by-five counter is incremented on the negative going transition of clock B ($\overline{\text{CKB}}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

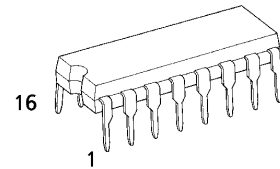
FEATURES:

- High Speed..... $f_{\text{MAX}} = 160\text{MHz}$ (typ.)
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Symmetrical Output Impedance... $|I_{\text{OH}}| = |I_{\text{OL}}| = 24\text{mA}$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays.... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74HC390

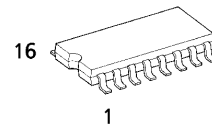
IEC LOGIC SYMBOL



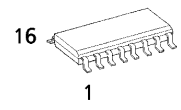
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

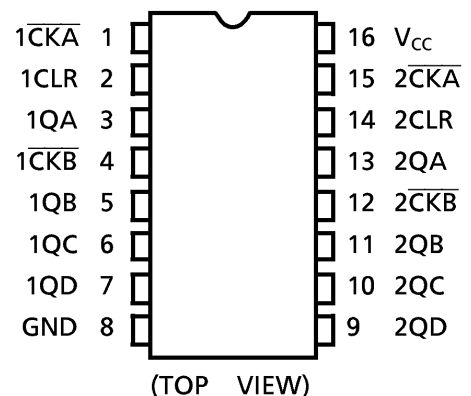


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

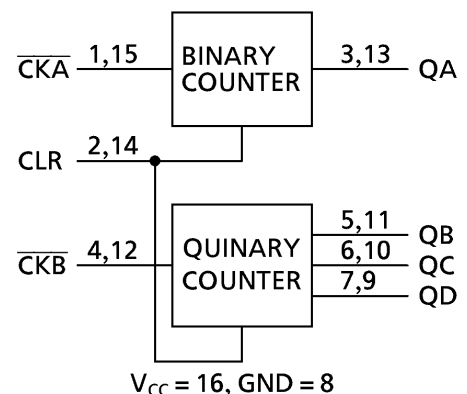


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



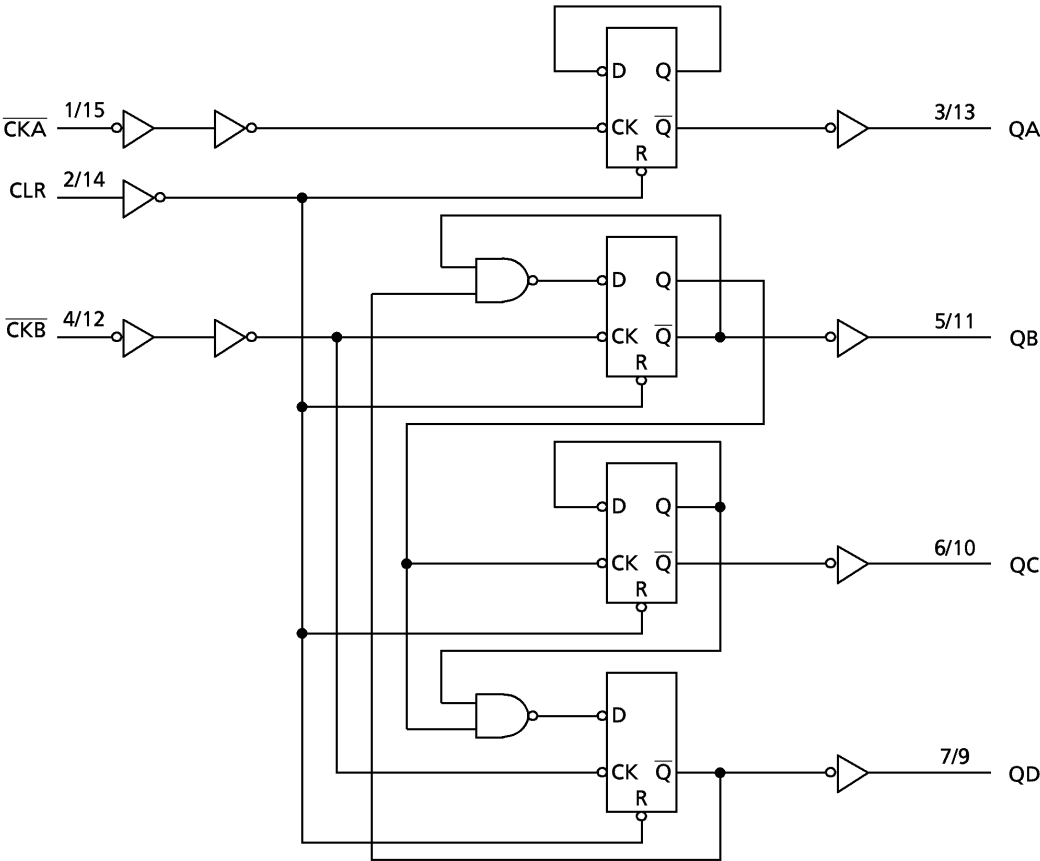
BLOCK DAIGRAM



TRUTH TABLE

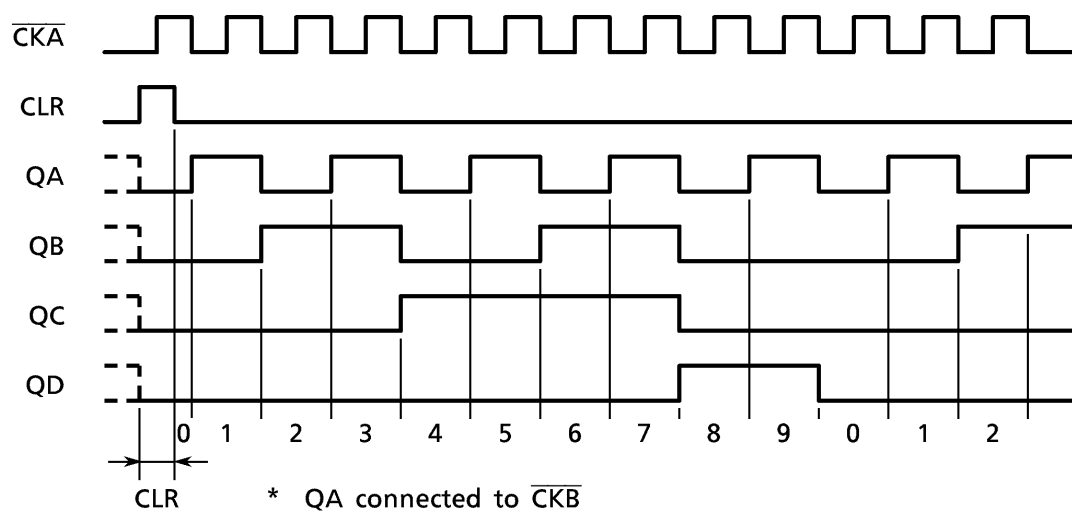
INPUTS			OUTPUTS			
$\overline{\text{CKA}}$	$\overline{\text{CKB}}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
$\overline{\text{L}}$	X	L	BINARY COUNT UP			
X	$\overline{\text{L}}$	L	QUINARY COUNT UP			

SYSTEM DIAGRAM

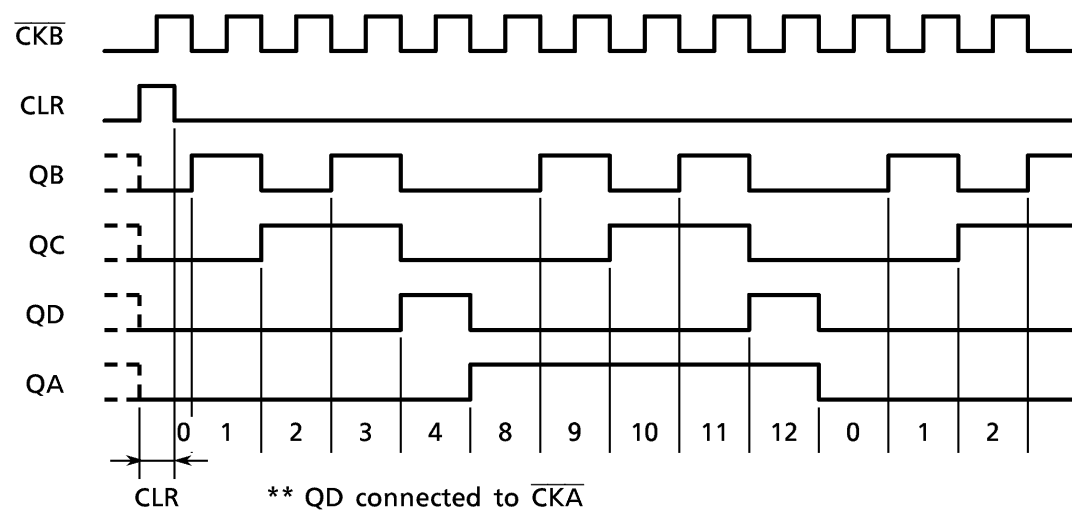


TIMING CHART

(1) BCD COUNT SEQUENCE*



(2) BI-QUINARY COUNT SEQUENCE**



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			$I_{OH} = -4\text{mA}$	3.0	2.58	—	—	2.48	
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 12\text{mA}$	3.0	—	—	0.36	—	
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	8.0	—	80.0	μA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{\text{CKA}}$, $\overline{\text{CKB}}$)	t_W (H) t_W (L)		3.3 ± 0.3	7.0	7.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	5.0	
Minimum Pulse Width (CLR)	t_W (H)		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	7.0 5.0	
Minimum Removal Time	t_{rem}		3.3 ± 0.3	7.0	7.0	7.0	
			5.0 ± 0.5	3.5	3.5	3.5	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{\text{CKA}}$ – QA)	t _{pLH} t _{pHL}		3.3 ± 0.3 5.0 ± 0.5	— —	8.2 5.5	14.0 8.4	1.0 1.0	16.0 9.6	ns
Propagation Delay Time ($\overline{\text{CKA}}$ – QC)	t _{pLH} t _{pHL}	QA connected to $\overline{\text{CKB}}$	3.3 ± 0.3 5.0 ± 0.5	— —	17.0 10.5	30.0 17.5	1.0 1.0	34.0 20.0	
Propagation Delay Time ($\overline{\text{CKB}}$ – QB, QD)	t _{pLH} t _{pHL}		3.3 ± 0.3 5.0 ± 0.5	— —	8.8 6.0	14.9 9.4	1.0 1.0	17.0 10.7	
Propagation Delay Time ($\overline{\text{CKB}}$ – QC)	t _{pLH} t _{pHL}		3.3 ± 0.3 5.0 ± 0.5	— —	11.0 7.1	18.8 11.3	1.0 1.0	21.5 12.8	
Propagation Delay Time (CLR – Qn)	t _{pHL}		3.3 ± 0.3 5.0 ± 0.5	— —	7.7 5.7	12.5 8.5	1.0 1.0	14.3 9.7	
Maximum Clock Frequency ($\overline{\text{CKA}}$)	f _{MAX}		3.3 ± 0.3 5.0 ± 0.5	60 100	120 180	— —	60 100	— —	MHz
Maximum Clock Frequency ($\overline{\text{CKB}}$)	f _{MAX}		3.3 ± 0.3 5.0 ± 0.5	45 90	90 140	— —	45 90	— —	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	40	—	—	—	

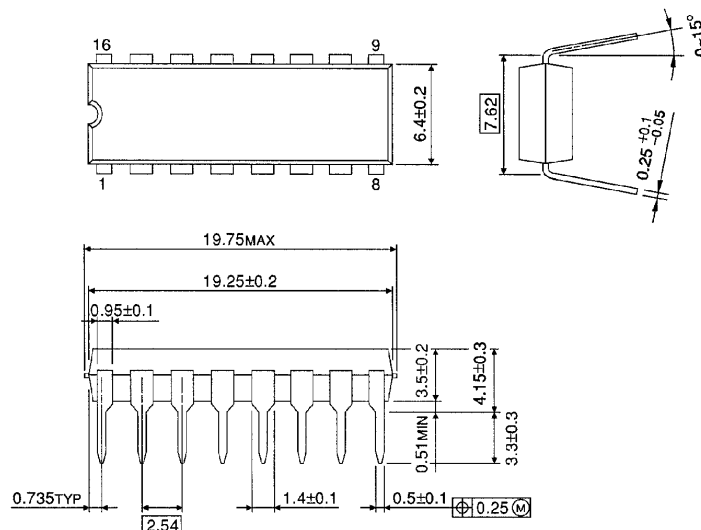
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr.}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 2 \text{ (per Counter)}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54)

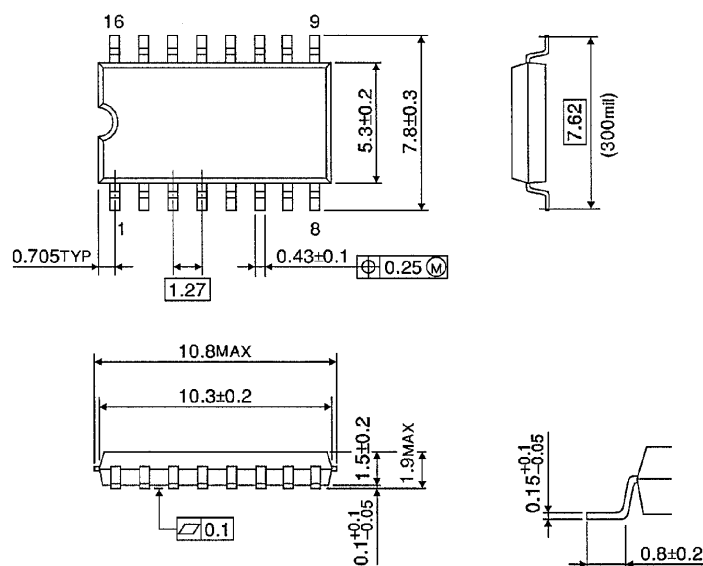
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

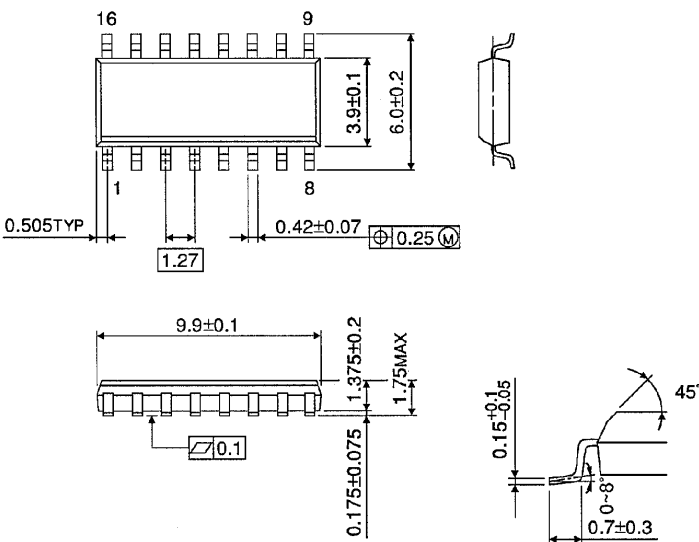


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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