# ispPAC-POWR1208 Evaluation Board PAC-POWR1208-EV

April 2004 Application Note AN6040

## Introduction

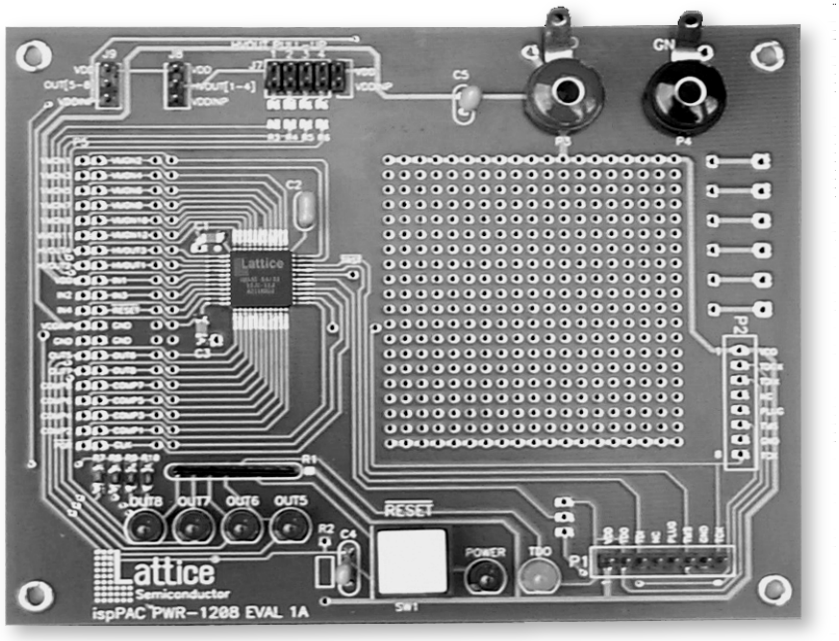
The Lattice Semiconductor ispPAC®-POWR1208 In-System-Programmable Analog Circuit allows designers to implement both the analog and digital functions of a power supply monitoring and sequencing subsystem within a single integrated circuit. By integrating analog functions such as comparators and programmable slew rate FET drivers with the digital functionality of a Programmable Logic Device (PLD), the ispPAC-POWR1208 provides the power-supply designer with a rich set of features in a single device.

ISP™ (In-System-Programmability) provides the designer with an unprecedented level of flexibility, allowing him to configure analog parameters such as threshold voltages as well as defining state machines and combinatorial logic functions. All configuration data is stored internally in $E^2$CMOS® nonvolatile memory. Programming a configuration is accomplished through an industry-standard JTAG IEEE 1149.1 interface.

## PAC-POWR1208-EV Evaluation Board

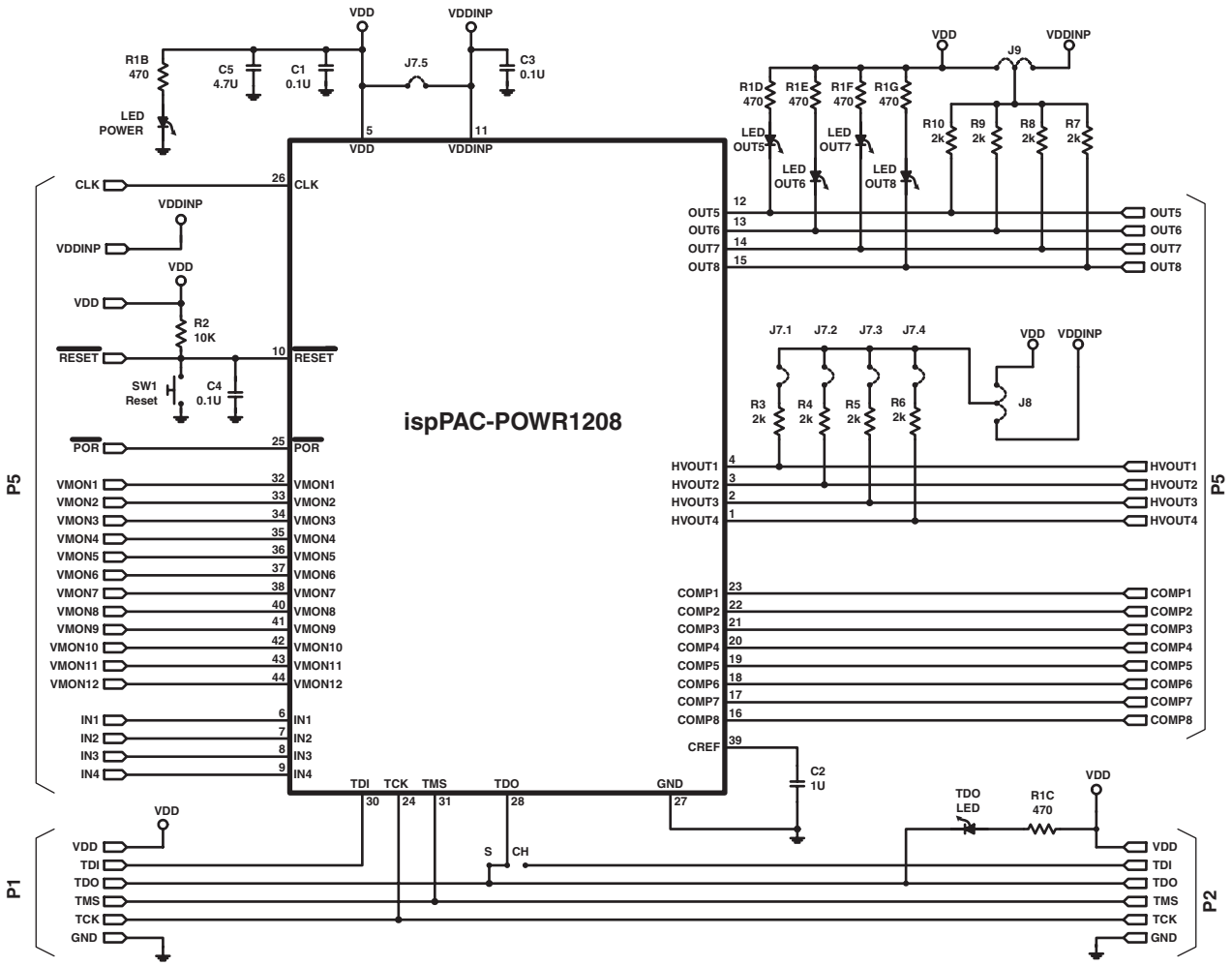
The PAC-POWR1208-EV evaluation board (Figure 1) allows the designer to quickly configure and evaluate the ispPAC-POWR1208 on a fully assembled printed-circuit board. The double-sided board supports a 44-pin TQFP package, a header for user I/O, a JTAG programming cable connector, and an uncommitted pad array for user prototyping. JTAG programming signals can be generated by using an ispDOWNLOAD® programming cable connected between the evaluation board and a PC's parallel (printer) port. Both analog and digital features of the ispPAC-POWR1208 can be easily configured using PAC-Designer® software.

***Figure 1. PAC-POWR1208-EV Evaluation Board***



A complete schematic for the evaluation board is shown in Figure 2.

***Figure 2. Schematic***




## Programming Interface

Lattice Semiconductor's ispDOWNLOAD® cable can be used to program the ispPAC-POWR1208 on the evaluation board. This cable plugs into a PC-compatible's parallel port connector, and includes active buffer circuitry inside its DB-25 connector housing. The other end of the ispDOWNLOAD cable terminates in an 8-pin 0.100" pitch header connector which plugs directly into a mating connector provided on the PAC-POWR1208-EV evaluation board.

## Prototype Area

A 19x18 grid (0.100" pitch) of uncommitted, plated through holes with annular-ring pads is provided as a user prototyping area. Adjacent to this uncommitted array are two 19-hole rows providing easy connections to both power and ground. This prototyping area allows the user to build small circuits directly on the evaluation board. In the case of larger circuits, the evaluation board can be readily connected into off-board circuitry through P5, into which can be mounted a 20 x 2 header.

## Power Supply Considerations

The ispPAC-POWR1208 operates with power supplies ranging from 2.25V to 5.5V, and allows for separate core (VDD) and I/O (VDDINP) voltages. Voltages ranging from 0 to 5.75V may be monitored at any of the 12 VMONx pins independent of the values of VDD and VDDINP. For device programming, however, VDD *MUST* be set to 3.3V.

On the evaluation board, VDD and VDDINP are normally connected together with a user-removable jumper (J7.5). This jumper can be removed to allow for independent VDD and VDDINP supplies.

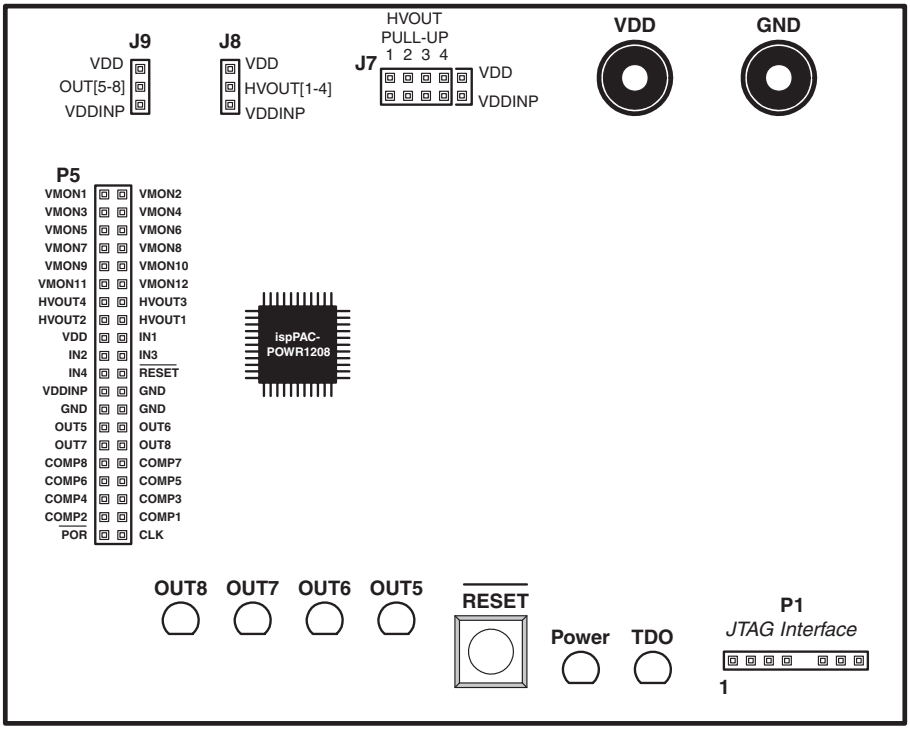
## Input/Output Connections

Connectors are provided for key functions and test points on this evaluation board, as shown In Figure 3. Power is supplied through two color coded (RED = +, BLACK = -) banana jacks in the upper right corner of the board.

The JTAG programming cable is connected to a keyed header (P1) in the lower right corner of the board. A PCB land pattern is provided for the addition of an additional JTAG interface header (P2) to allow for connecting multiple PAC-POWR1208-EV evaluation boards into a multi-device programming chain.

Access to the ispPAC-POWR1208's I/O pins is available at P5, which is a 2x20 row of pads to which one may attach test probes or a ribbon-cable connector. At this point all of the device's I/O pins (except those required for the JTAG programming interface) are accessible.

***Figure 3. I/O and Jumpers***




## Jumper Options

Several jumpers are provided on the evaluation board to make it simple to implement common circuit configurations. These jumpers are:

- **J7** - positions 1-4 connect pull-up resistors to the high voltage outputs HVOUT1-4, and allow the user to enable the pull-ups on an output-by-output basis. The pull-up voltage is selected by J8. Position 5 (the right-most position) is used to connect VDDINP to VDD, and should normally be left in place. This jumpers needs to be removed when using separate VDD and VDDINP supplies.
- **J8** - Selects a pull-up voltage to which the High-Voltage outputs (HVOUT1-4) may be pulled up to, either VDD or VDDINP.
- **J9** - Selects whether open-drain digital outputs OUT5-OUT8 are pulled up to VDD (upper position), VDDINP (lower position), or not pulled up at all. These outputs are pulled up through 2KΩ resistors.

## Controls and Indicators

A reset switch is provided on the evaluation board which pulls the $\overline{\text{RESET}}$ input pin low when it is depressed, re-initializing the ispPAC-POWR1208.

LEDs are also provided as an aid to debugging. One LED shows whether the board has power applied, while another is connected to the JTAG TDO line, and will flash when a download is being performed. Additionally, four LEDs are attached to the ispPAC-POWR1208's OUT5-OUT8 lines. By adding appropriate code to the sequencer program, these LEDs can be made to indicate the internal status of the ispPAC-POWR1208, and can be a useful debug aid.

## PCB Artwork

***Figure 4. Silk Screen***

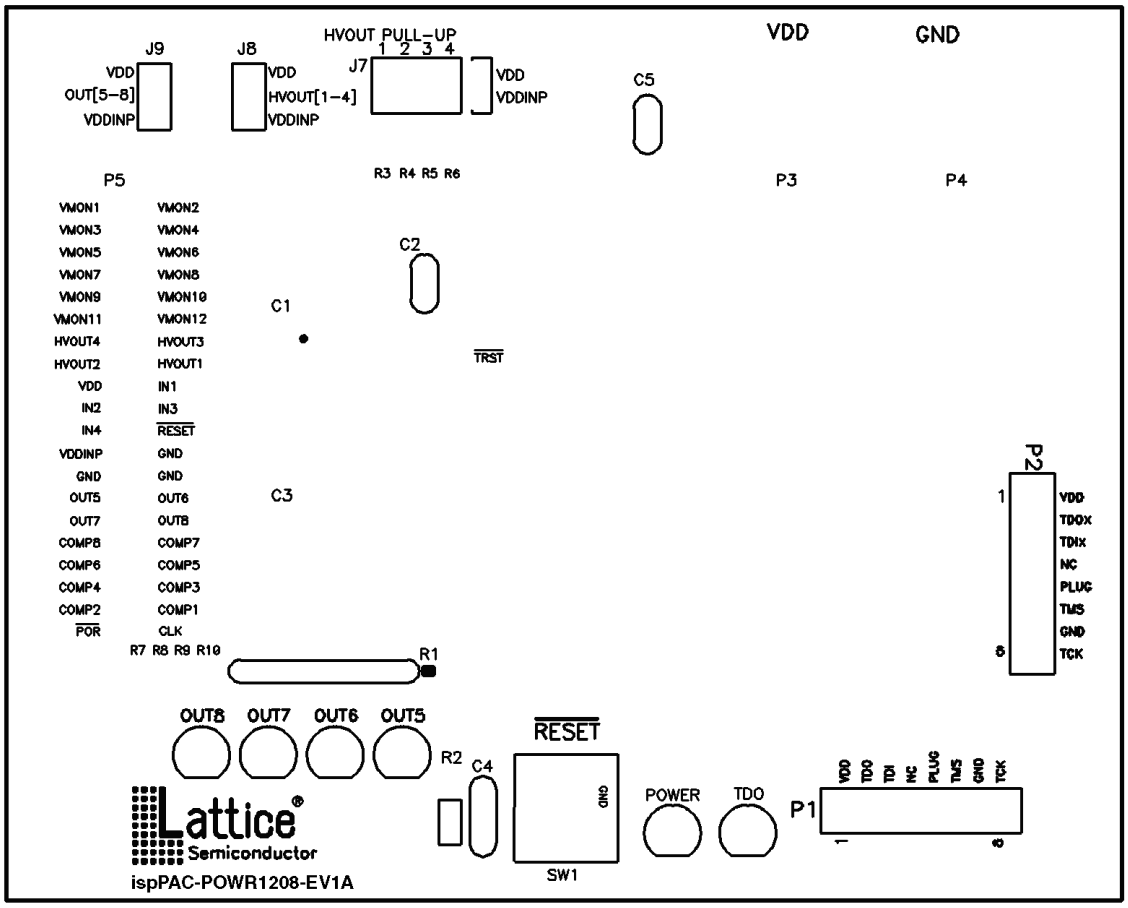


*Figure 5. Top-side Foil*

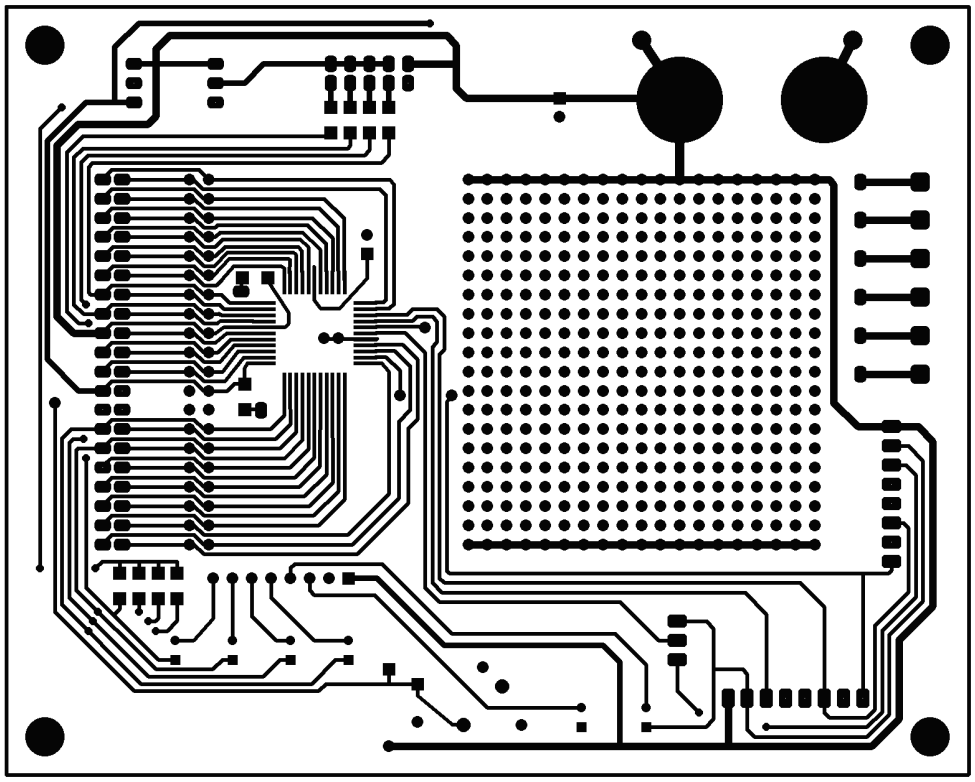
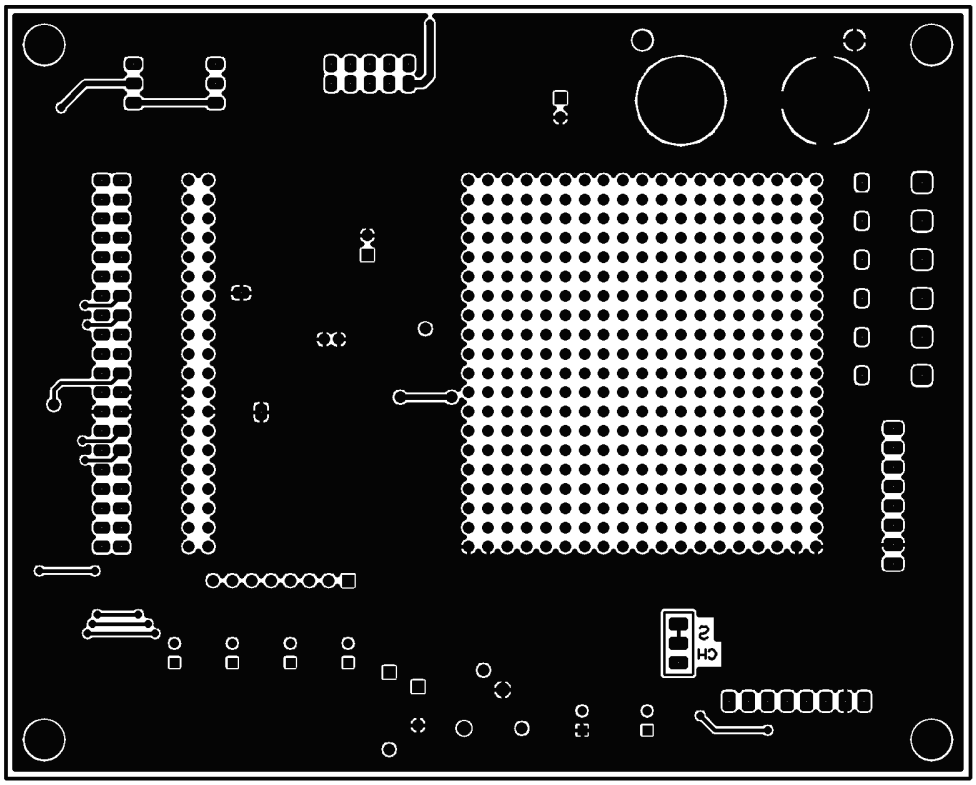


*Figure 6. Bottom-side Foil*



## Component List

| Quantity | Ref. Designators | Description |
|---|---|---|
| 2 | C1, C3 | 0.1µF capacitor |
| 1 | C2 | 1µF capacitor |
| 1 | C4 | 0.1µF capacitor |
| 1 | C5 | 4.7µF capacitor |
| 1 | J7 | 2 x 5 header strip, dual row, 0.1” spacing |
| 2 | J8,J9 | 1 x 3 header strip, single row, 0.1” spacing |
| 5 | LED_A, LED_B, LED_C, LED_D, POWER_LED | T-1-3/4 red LED |
| 1 | P1 | 1x8 header strip, single row, 0.1” spacing |
| 1 | P3 | Red banana jack |
| 1 | P4 | Black banana jack |
| 1 | R1 | 470 ohm SIP-8 resnet, 7-resistor SIP, bussed type |
| 1 | R2 | 10K resistor |
| 8 | R3, R4, R5, R6, R7, R8, R9, R10 | 2K 5% resistor |
| 1 | SW3 | Pushbutton switch |
| 1 | TDO_LED | T1-3/4 green LED |
| 1 | U1 | ispPAC-POWR1208 |

## Technical Support Assistance

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