Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.048 @ V_{GS} = –4.5 V	–6.3
	0.068 @ V_{GS} = –2.5 V	–5.3
	0.090 @ V_{GS} = –1.8 V	–4.6

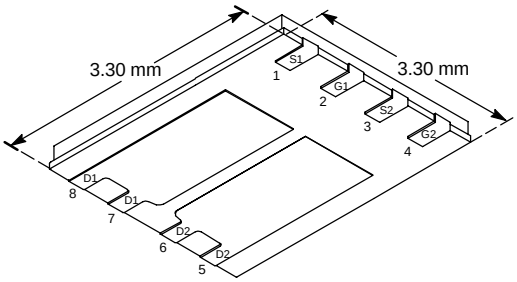
FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- ESD Protected: 4500 V
- Ultra-Low Thermal Resistance, PowerPAK™ Package with Low 1.07-mm Profile

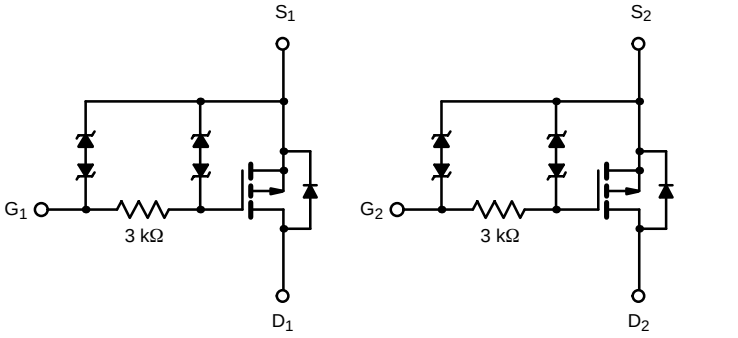
APPLICATIONS

- Bidirectional Switch

PowerPAK™ 1212-8



Bottom View



P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	–20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–6.3	–4.3	A
	T_A = 85°C		–4.5	–3.1	
Pulsed Drain Current		I_{DM}	–20		
continuous Source Current (Diode Conduction)[a]		I_S	–2.3	–1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.8	1.3	W
	T_A = 85°C		1.5	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	35	44	°C/W
	Steady State		75	94	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4	5	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

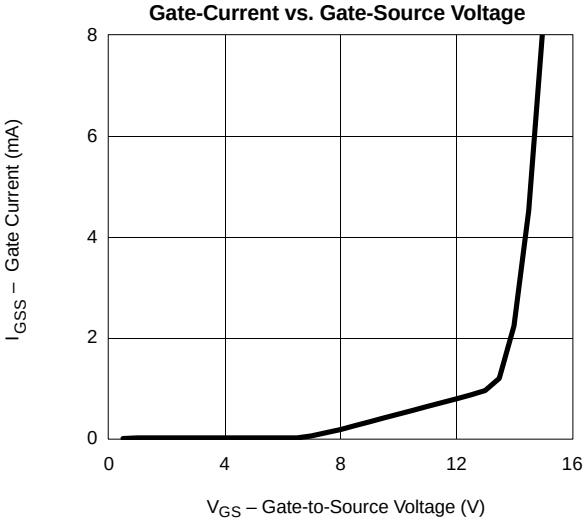
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –800 μA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1.5	νA
		V_{DS} = 0 V, V_{GS} = ±12 V			±10	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
		V_{DS} = –16 V, V_{GS} = 0 V, T_J = 85°C			–5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ –5 V, V_{GS} = –4.5 V	–20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –6.3 A		0.041	0.048	Ω
		V_{GS} = –2.5 V, I_D = –5.3 A		0.057	0.068	
		V_{GS} = –1.8 V, I_D = –1 A		0.072	0.090	
Forward Transconductance[a]	g_{fs}	V_{DS} = –15 V, I_D = –6.3 A		14		S
Diode Forward Voltage[a]	V_{SD}	I_S = –2.3 A, V_{GS} = 0 V		–0.8	–1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –6.3 A		12	18	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.9		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		2.5	4	μs
Rise Time	t_r			4	6	
Turn-Off Delay Time	$t_{d(off)}$			15	23	
Fall Time	t_f			12	18	

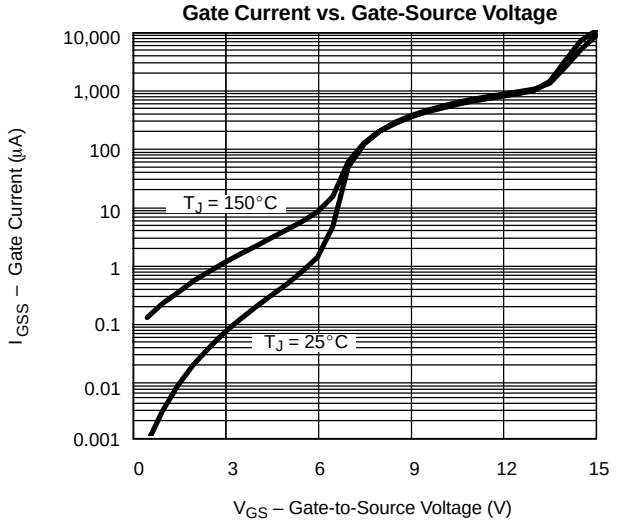
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Gate-Current vs. Gate-Source Voltage

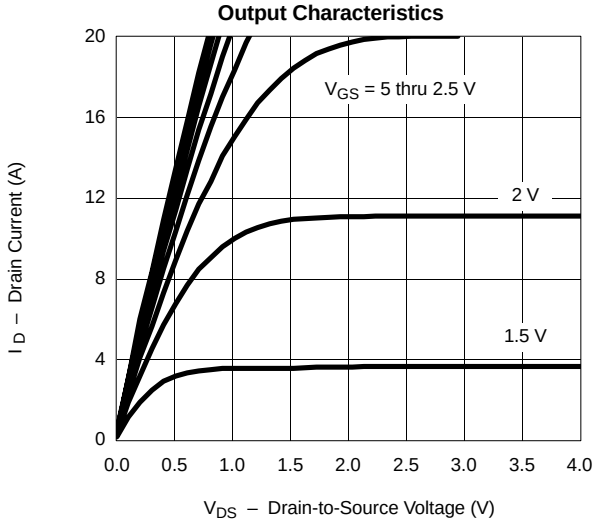


Gate Current vs. Gate-Source Voltage

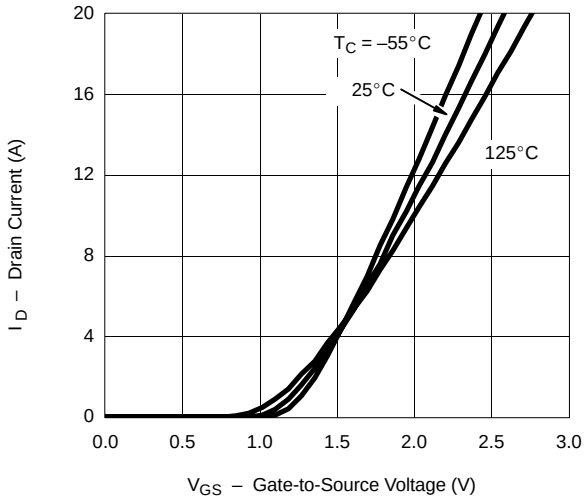


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

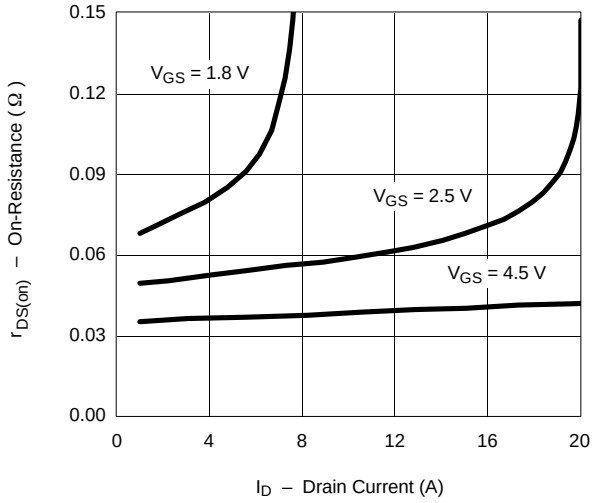
Output Characteristics



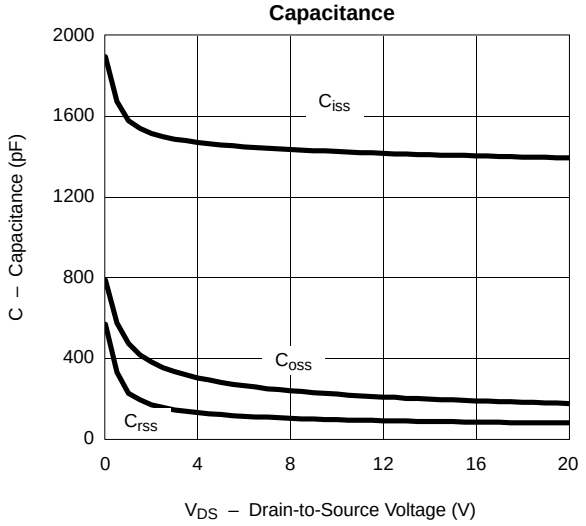
Transfer Characteristics



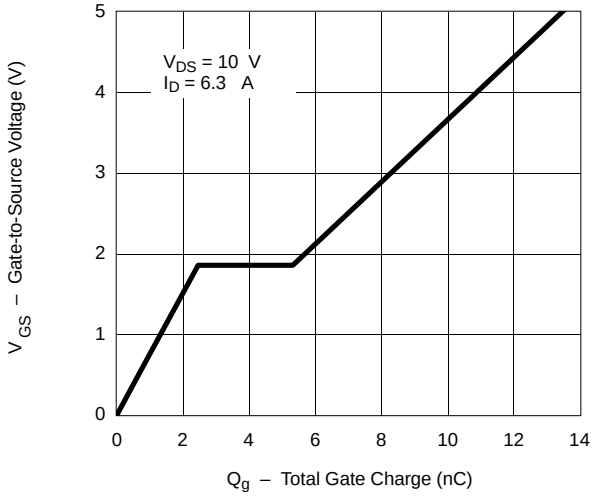
On-Resistance vs. Drain Current



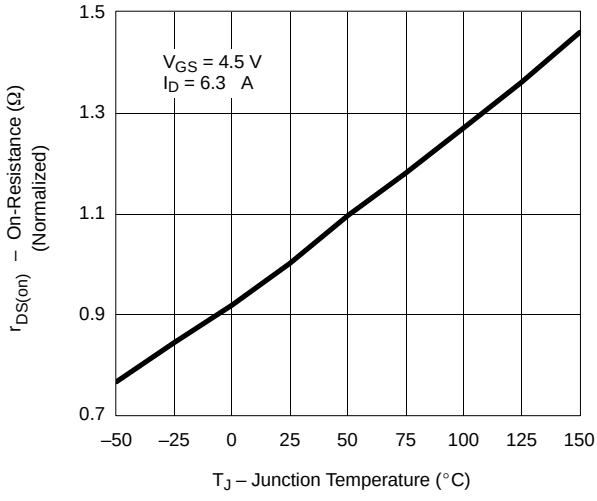
Capacitance



Gate Charge

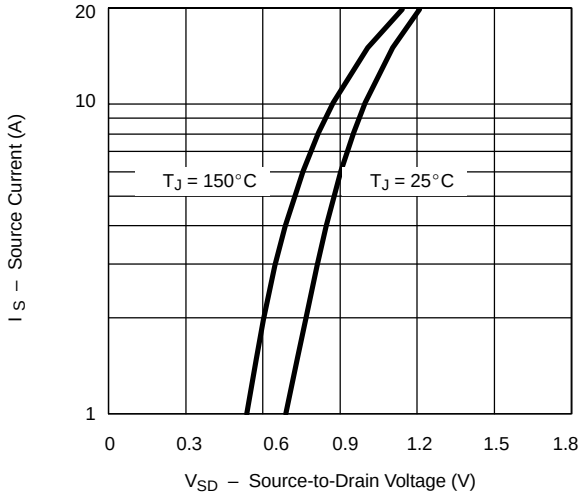


On-Resistance vs. Junction Temperature

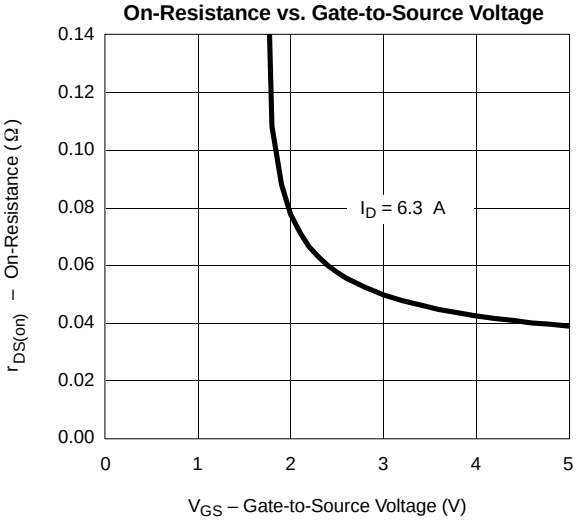


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

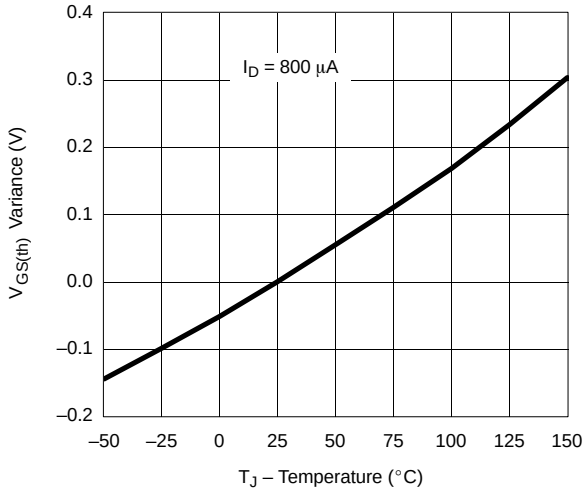
Source-Drain Diode Forward Voltage



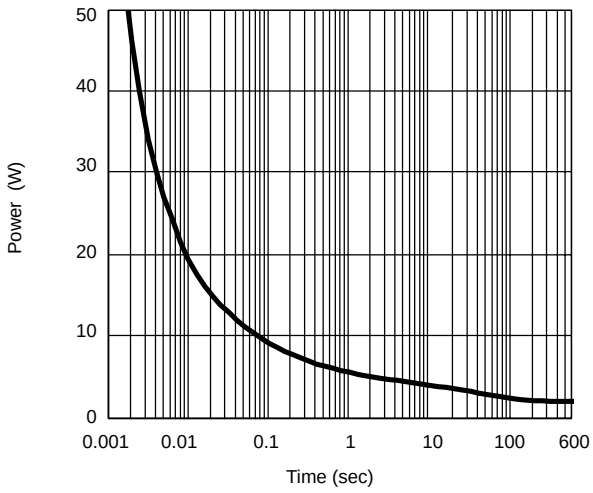
On-Resistance vs. Gate-to-Source Voltage



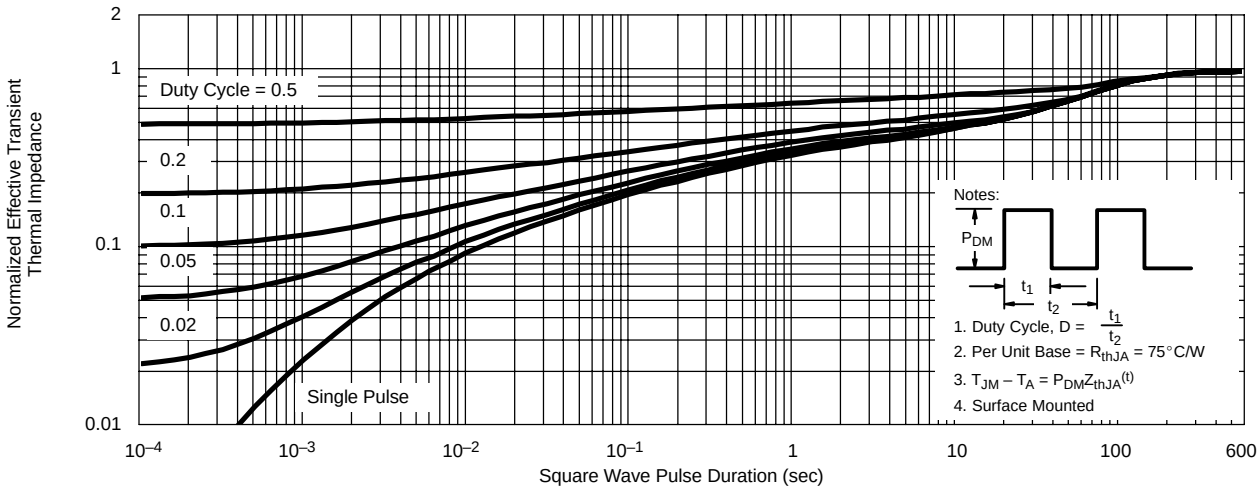
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Case