19-2525; Rev 0; 7/02

MAXIM

16-Bit, +5V, 200ksps ADC with 10µA Shutdown

General Description

The MAX1162 low-power, 16-bit analog-to-digital converter (ADC) features a successive-approximation ADC, automatic power-down, fast 1.1µs wakeup, and a high-speed SPI™/QSPI™/MICROWIRE™-compatible interface. The MAX1162 operates with a single +5V analog supply and features a separate digital supply, allowing direct interfacing with +2.7V to +5.25V digital logic.

At the maximum sampling rate of 200ksps, the MAX1162 consumes only 2.5mA. Power consumption is only 12.5mW (AV_{DD} = DV_{DD} = +5V) at a 200ksps (max) sampling rate. AutoShutdown™ reduces supply current to 130µA at 10ksps and to less than 10µA at reduced sampling rates.

Excellent dynamic performance and low power, combined with ease of use and small package size (10-pin µMAX and 10-pin DFN) make the MAX1162 ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

Applications

Motor Control

Industrial Process Control

Industrial I/O Modules

Data-Acquisition Systems

Thermocouple Measurements

Accelerometer Measurements

Portable- and Battery-Powered Equipment

Functional Diagram appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Features

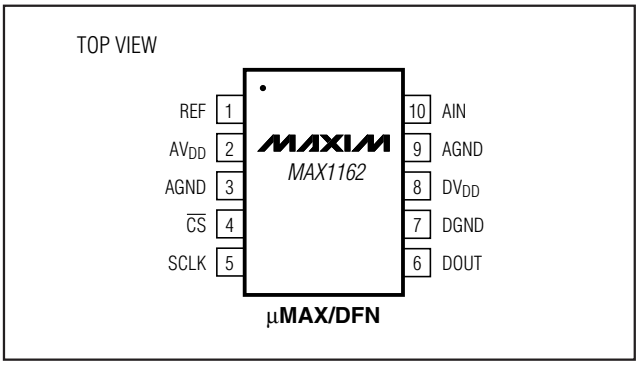
- **16-Bit Resolution, No Missing Codes**
- **+5V Single-Supply Operation**
- **Adjustable Logic Level (+2.7V to +5.25V)**
- **Input Voltage Range: 0 to V_{REF}**
- **Internal Track/Hold, 4MHz Input Bandwidth**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Small 10-Pin µMAX or 10-Pin DFN Package**
- **Low Power**
  - **2.5mA at 200ksps**
  - **130µA at 10ksps**
  - **0.1µA in Power-Down Mode**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1162ACUB	0°C to +70°C	10 µMAX	±2
MAX1162AC_B*	0°C to +70°C	10 DFN	±2
MAX1162BCUB	0°C to +70°C	10 µMAX	±2
MAX1162BC_B*	0°C to +70°C	10 DFN	±2
MAX1162CCUB	0°C to +70°C	10 µMAX	±4
MAX1162CC_B*	0°C to +70°C	10 DFN	±4
MAX1162AEUB	-40°C to +85°C	10 µMAX	±2
MAX1162AE_B*	-40°C to +85°C	10 DFN	±2
MAX1162BEUB	-40°C to +85°C	10 µMAX	±2
MAX1162BE_B*	-40°C to +85°C	10 DFN	±2
MAX1162CEUB	-40°C to +85°C	10 µMAX	±4
MAX1162CE_B*	-40°C to +85°C	10 DFN	±4

**Future product—contact factory for DFN package availability.*

Pin Configuration



µMAX/DFN

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
DGND to AGND.....-0.3V to +0.3V
AIN, REF to AGND .....-0.3V to (AV_{DD} + 0.3V)
SCLK, $\overline{CS}$ to DGND.....-0.3V to +6V
DOUT to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Current Into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Ranges
MAX1162_CUB .....0°C to +70°C
MAX1162_EUB .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz (50% duty cycle), 24 clocks/conversion (200ksps), V_{REF} = +4.096V, C_{REF} = 4.7µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (NOTE 1)							
Resolution				16			Bits
Relative Accuracy (Note 2)	INL	MAX1162A				±2	LSB
		MAX1162B				±2	
		MAX1162C				±4	
Differential Nonlinearity	DNL	No missing codes over temperature	MAX1162A			±1	LSB
			MAX1162B	-1		±1.75	
		MAX1162C				±2	
Transition Noise		RMS noise			±0.65		LSB_{RMS}
Offset Error					0.1	1	mV
Gain Error		(Note 3)			±0.002	±0.01	%FSR
Offset Drift					0.4		ppm/°C
Gain Drift		(Note 3)			0.2		ppm/°C
DYNAMIC SPECIFICATIONS (1kHz sine wave, 4.096V_{P-P}) (Note 1)							
Signal-to-Noise Plus Distortion	SINAD			86	89.5		dB
Signal-to-Noise Ratio	SNR			87	90		dB
Total Harmonic Distortion	THD					-90	dB
Spurious-Free Dynamic Range	SFDR			92	103		dB
Full-Power Bandwidth		-3dB point			4		MHz
Full-Linear Bandwidth		SINAD > 86dB			10		kHz
CONVERSION RATE							
Conversion Time	t_{CONV}	(Note 4)		5		240	µs
Serial Clock Frequency	f_{SCLK}			0.1		4.8	MHz
Aperture Delay	t_{AD}				15		ns
Aperture Jitter	t_{AJ}				<50		ps
Sample Rate	f_S	f_{SCLK} / 24				200	ksps
Track/Hold Acquisition Time	t_{ACQ}			1.1			µs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz (50% duty cycle), 24 clocks/conversion (200ksps), V_{REF} = +4.096V, C_{REF} = 4.7µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT (AIN)							
Input Range	V_{AIN}			0		V_{REF}	V
Input Capacitance	C_{AIN}				40		pF
EXTERNAL REFERENCE							
Input Voltage Range	V_{REF}			3.8		AV_{DD}	V
Input Current	I_{REF}	V_{REF} = +4.096V, f_{SCLK} = 4.8MHz			100		µA
		V_{REF} = +4.096V, SCLK idle			0.01		
		$\overline{CS}$ = DV_{DD}, SCLK idle			0.01		
DIGITAL INPUTS (SCLK, $\overline{CS}$)							
Input High Voltage	V_{IH}	DV_{DD} = +2.7V to +5.25V		0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}	DV_{DD} = +2.7V to +5.25V				0.3 x DV_{DD}	V
Input Leakage Current	I_{IN}	V_{IN} = 0 to DV_{DD}			±0.1	±1	µA
Input Hysteresis	V_{HYST}				0.2		V
Input Capacitance	C_{IN}				15		pF
DIGITAL OUTPUT (DOUT)							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA, DV_{DD} = +2.7V to +5.25V		DV_{DD} - 0.25V			V
Output Low Voltage	V_{OL}	I_{SINK} = 10mA, DV_{DD} = +4.75V to +5.25V				0.7	V
		I_{SINK} = 1.6mA, DV_{DD} = +2.7V to +5.25V				0.4	
Three-State Output Leakage Current	I_L	$\overline{CS}$ = DV_{DD}			±0.1	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = DV_{DD}			15		pF
POWER SUPPLIES							
Analog Supply	AV_{DD}			4.75		5.25	V
Digital Supply	DV_{DD}			2.7		5.25	V
Analog Supply Current	I_{AVDD}	$\overline{CS}$ = DGND	200ksps		2.0	2.5	mA
			100ksps		1.0		
			10ksps		0.1		
			1ksps		0.01		
Digital Supply Current	I_{DVDD}	$\overline{CS}$ = DGND, DOUT = all zeros	200ksps		0.6	1.0	mA
			100ksps		0.3		
			10ksps		0.03		
			1ksps		0.003		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +4.75V to +5.25V, f_{SCLK} = 4.8MHz (50% duty cycle), 24 clocks/conversion (200ksps), V_{REF} = +4.096V, C_{REF} = 4.7µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{AVDD} + I_{DVDD}	$\overline{CS}$ = DV_{DD}, SCLK = idle		0.1	10	µA
Power-Supply Rejection Ratio	PSRR	AV_{DD} = DV_{DD} = +4.75V to +5.25V, full-scale input (Note 5)		68		dB

TIMING CHARACTERISTICS (Figures 1, 2, 3, and 6)

(**AV_{DD} = DV_{DD} = +4.75V to +5.25V**, f_{SCLK} = 4.8MHz (50% duty cycle), 24 clocks/conversion (200ksps), V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.1			µs
SCLK to DOUT Valid	t_{DO}	C_{DOUT} = 50pF			50	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{DOUT} = 50pF			80	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{DOUT} = 50pF			80	ns
$\overline{CS}$ Pulse Width	t_{CSW}		50			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CSH}				0	ns
SCLK High Pulse Width	t_{CH}		65			ns
SCLK Low Pulse Width	t_{CL}		65			ns
SCLK Period	t_{CP}		208			ns

TIMING CHARACTERISTICS (Figures 1, 2, 3, and 6)

(AV_{DD} = +4.75V to +5.25V, **DV_{DD} = +2.7V to +5.25V**, f_{SCLK} = 4.8MHz (50% duty cycle), 24 clocks/conversion (200ksps), V_{REF} = +4.096V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.1			µs
SCLK to DOUT Valid	t_{DO}	C_{DOUT} = 50pF			100	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{DOUT} = 50pF			100	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{DOUT} = 50pF			80	ns
$\overline{CS}$ Pulse Width	t_{CSW}		50			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CSH}				0	ns
SCLK High Pulse Width	t_{CH}		65			ns
SCLK Low Pulse Width	t_{CL}		65			ns
SCLK Period	t_{CP}		208			ns

Note 1: AV_{DD} = DV_{DD} = +5V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: Offset and reference errors nulled.

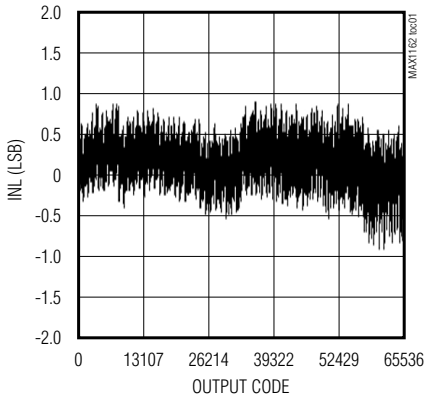
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 5: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply voltage.

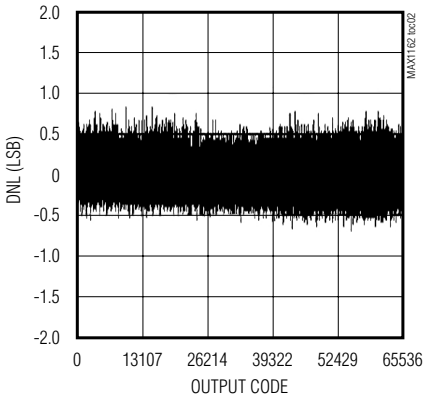
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = +5V, f_{SCLK} = 4.8MHz, C_{LOAD} = 50pF, C_{REF} = 4.7µF, V_{REF} = +4.096V, T_A = +25°C, unless otherwise noted.)

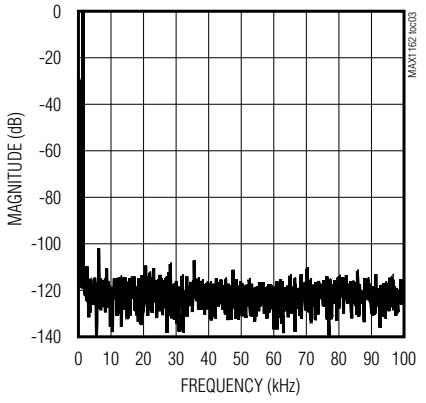
INL vs. OUTPUT CODE



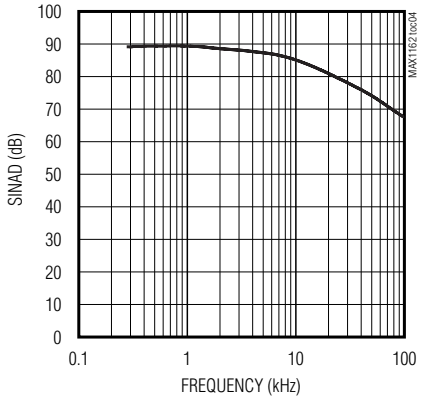
DNL vs. OUTPUT CODE



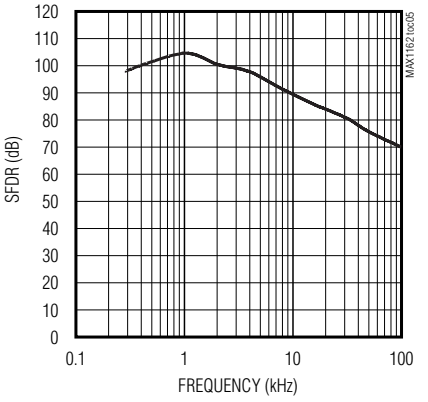
MAX1162 FFT



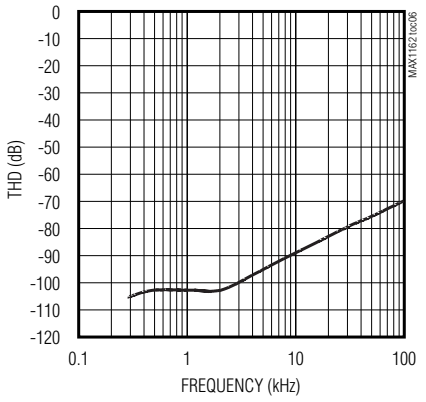
SINAD vs. FREQUENCY



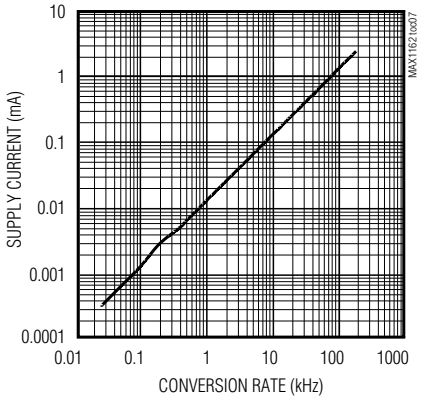
SFDR vs. FREQUENCY



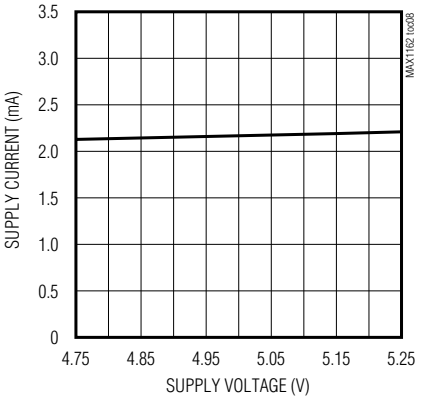
THD vs. FREQUENCY



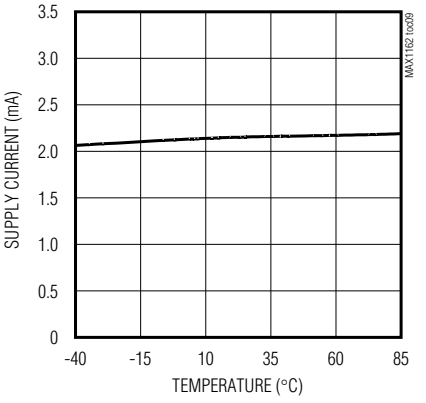
SUPPLY CURRENT vs. CONVERSION RATE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

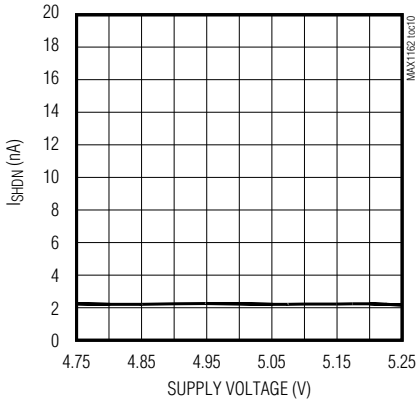


16-Bit, +5V, 200ksps ADC with 10µA Shutdown

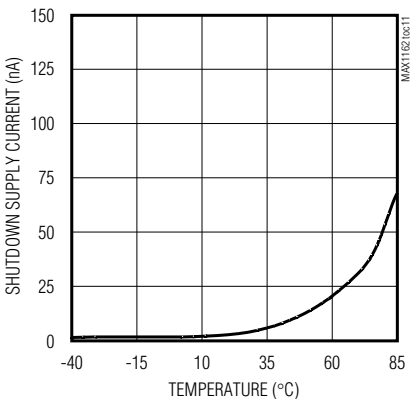
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5V, f_{SCLK} = 4.8MHz, C_{LOAD} = 50pF, C_{REF} = 4.7µF, V_{REF} = +4.096V, T_A = +25°C, unless otherwise noted.)

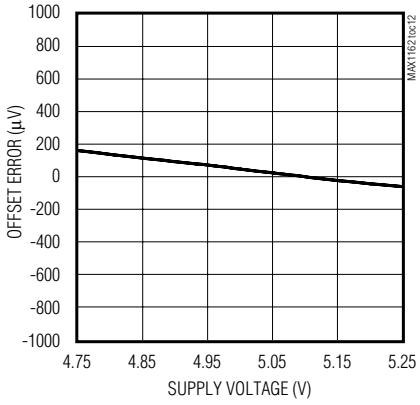
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



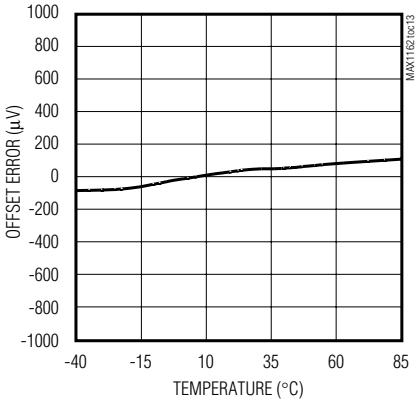
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



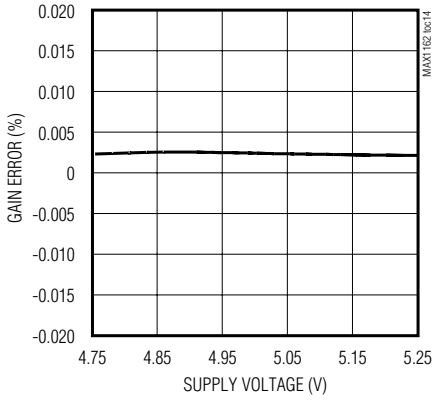
OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



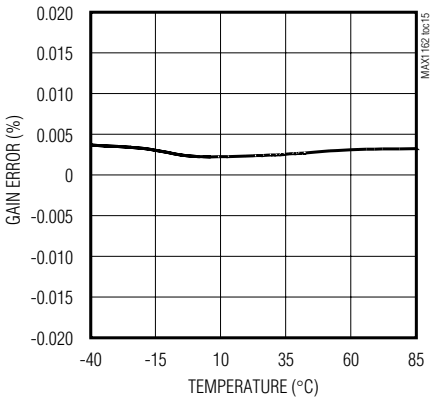
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	REF	External Reference Voltage Input. Sets the analog voltage range. Bypass to AGND with a 4.7µF capacitor.
2	AV_{DD}	Analog +5V Supply Voltage. Bypass to AGND (pin 3) with a 0.1µF capacitor.
3, 9	AGND	Analog Ground. Connect pins 3 and 9 together. Place star ground at pin 3.
4	$\overline{CS}$	Active-Low Chip-Select Input. Forcing $\overline{CS}$ high places the MAX1162 in shutdown with a typical current of 0.1µA. A high-to-low transition on $\overline{CS}$ activates normal operating mode and initiates a conversion.
5	SCLK	Serial Clock Input. SCLK drives the conversion process and clocks out data at data rates up to 4.8MHz.
6	DOUT	Serial Data Output. Data changes state on SCLK's falling edge. DOUT is high impedance when $\overline{CS}$ is high.
7	DGND	Digital Ground
8	DV_{DD}	Digital Supply Voltage. Bypass to DGND with a 0.1µF capacitor.
10	AIN	Analog Input

Detailed Description

The MAX1162 includes an input track-and-hold (T/H) and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 16-bit output. Figure 4 shows the MAX1162 in its simplest configuration. The serial interface requires only three digital lines (SCLK, $\overline{CS}$, and DOUT) and provides an easy interface to microprocessors (µPs).

The MAX1162 has two power modes: normal and shutdown. Driving $\overline{CS}$ high places the MAX1162 in shutdown, reducing the supply current to 0.1µA (typ), while pulling $\overline{CS}$ low places the MAX1162 in normal operating mode. Falling edges on $\overline{CS}$ initiate conversions that are driven by SCLK. The conversion result is available at DOUT in unipolar serial format. The serial data stream consists of eight zeros followed by the data bits (MSB first). Figure 3 shows the interface timing diagram.

Analog Input

Figure 5 illustrates the input sampling architecture of the ADC. The voltage applied at REF sets the full-scale input voltage.

Track-and-Hold (T/H)

In track mode, the analog signal is acquired on the internal hold capacitor. In hold mode, the T/H switches open and the capacitive DAC samples the analog input.

During the acquisition, the analog input (AIN) charges capacitor C_{DAC}. The acquisition interval ends on the falling edge of the sixth clock cycle (Figure 6). At this instant, the T/H switches open. The retained charge on C_{DAC} represents a sample of the input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to zero within the limits of 16-bit resolution. At the end of the conversion, force $\overline{CS}$ high and then low to reset the input side of the C_{DAC} switches back to AIN, and charge C_{DAC} to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$t_{ACQ} = 13(R_S + R_{IN}) \times 35pF$$

where $R_{IN} = 800\Omega$, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.1µs. A source impedance less than 1kΩ does not significantly affect the ADC's performance.

To improve the input signal bandwidth under AC conditions, drive AIN with a wideband buffer (>4MHz) that can drive the ADC's input capacitance and settle quickly.

16-Bit, +5V, 200ksps ADC with 10µA Shutdown

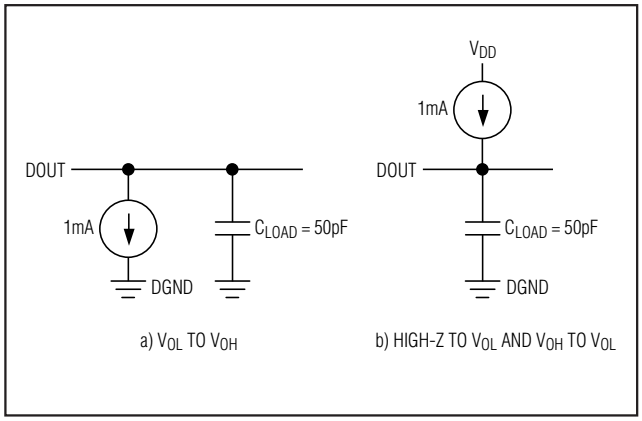


Figure 1. Load Circuits for DOUT Enable Time and SCLK to DOUT Delay Time

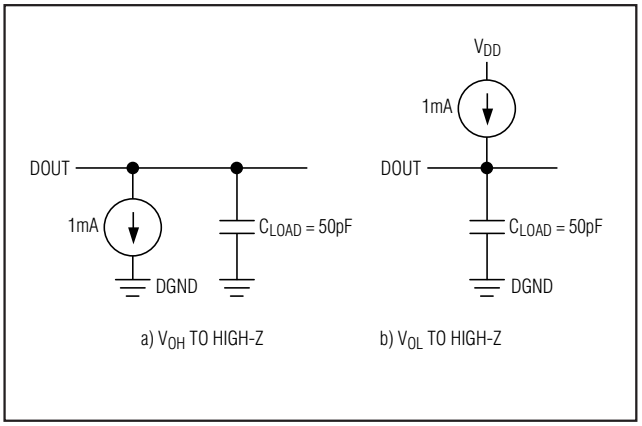


Figure 2. Load Circuits for DOUT Disable Time

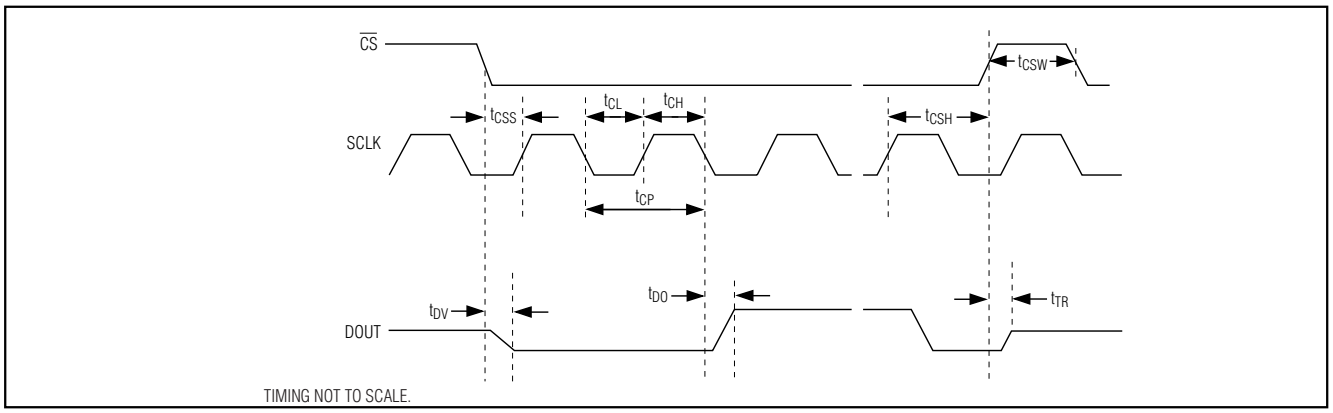


Figure 3. Detailed Serial Interface Timing

Input Bandwidth

The ADC's input tracking circuitry has a 4MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, use anti-alias filtering.

Analog Input Protection

Internal protection diodes, which clamp the analog input to AV_{DD} or AGND, allow the input to swing from AGND - 0.3V to AV_{DD} + 0.3V, without damaging the device.

If the analog input exceeds 300mV beyond the supplies, limit the input current to 10mA.

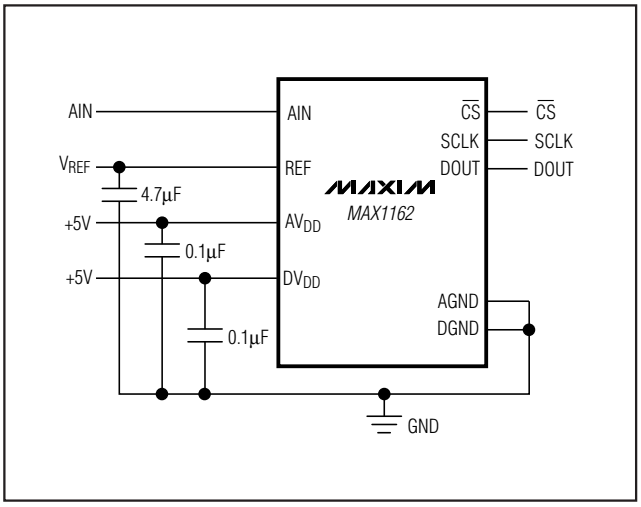


Figure 4. Typical Operating Circuit

Digital Interface

Initialization after Power-Up and Starting a Conversion

The digital interface consists of two inputs, SCLK and $\overline{CS}$, and one output, DOUT. A logic high on $\overline{CS}$ places the MAX1162 in shutdown (AutoShutdown) and places DOUT in a high-impedance state. A logic low on $\overline{CS}$ places the MAX1162 in the fully powered mode.

To start a conversion, pull $\overline{CS}$ low. A falling edge on $\overline{CS}$ initiates an acquisition. SCLK drives the A/D conversion and shifts out the conversion results (MSB first) at DOUT.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs (Figures 6 and 7). Ensure that the duty cycle on SCLK is between 40% and 60% at 4.8MHz (the maximum clock frequency). For lower clock frequencies, ensure that the minimum high and low times are at least 65ns. Conversions with SCLK rates less than 100kHz can result in reduced accuracy due to leakage.

Note: Coupling between SCLK and the analog inputs (AIN and REF) may result in an offset. Variations in frequency, duty cycle, or other aspects of the clock signal's shape result in changing offset.

A $\overline{CS}$ falling edge initiates an acquisition sequence. The analog input is stored in the capacitive DAC, DOUT changes from high impedance to logic low, and the ADC begins to convert after the sixth clock cycle. SCLK drives the conversion process and shifts out the conversion result on DOUT.

SCLK begins shifting out the data (MSB first) after the falling edge of the 8th SCLK pulse. Twenty-four falling clock edges are needed to shift out the eight leading zeros and 16 data bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to the rising edge of $\overline{CS}$, produce trailing zeros at DOUT and have no effect on the converter operation.

Force $\overline{CS}$ high after reading the conversion's LSB to reset the internal registers and place the MAX1162 in shutdown. For maximum throughput, force $\overline{CS}$ low again to initiate the next conversion immediately after the specified minimum time (t_{CSW}).

Note: Forcing $\overline{CS}$ high in the middle of a conversion immediately aborts the conversion and places the MAX1162 in shutdown.

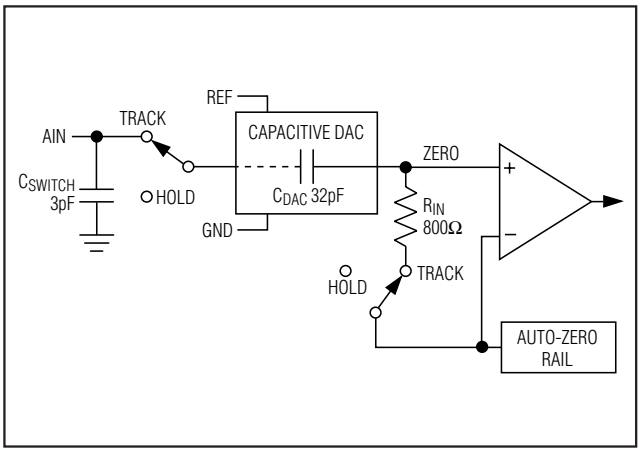


Figure 5. Equivalent Input Circuit

Output Coding and Transfer Function

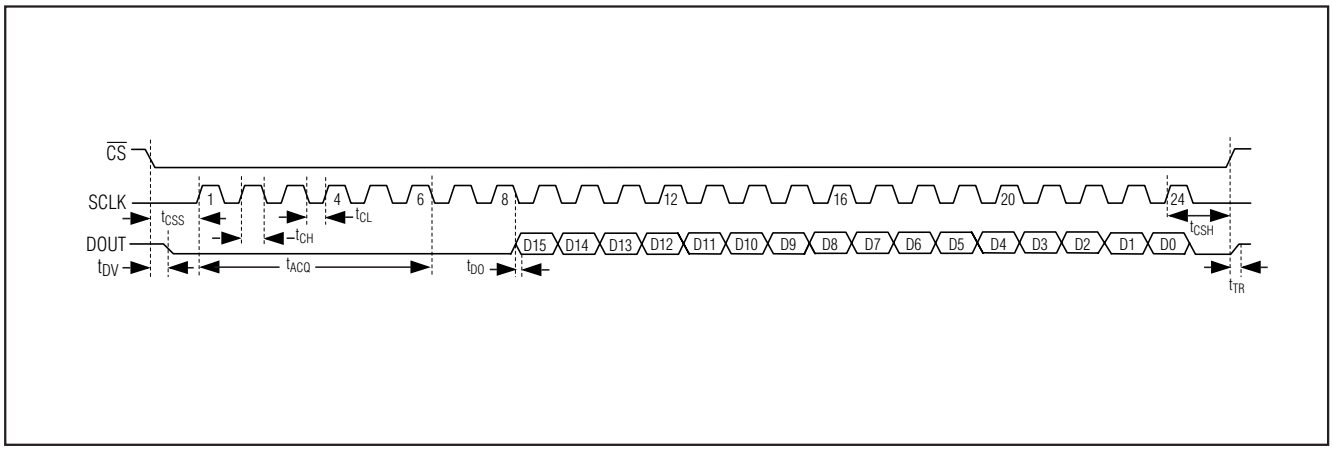


Figure 6. External Timing Diagram

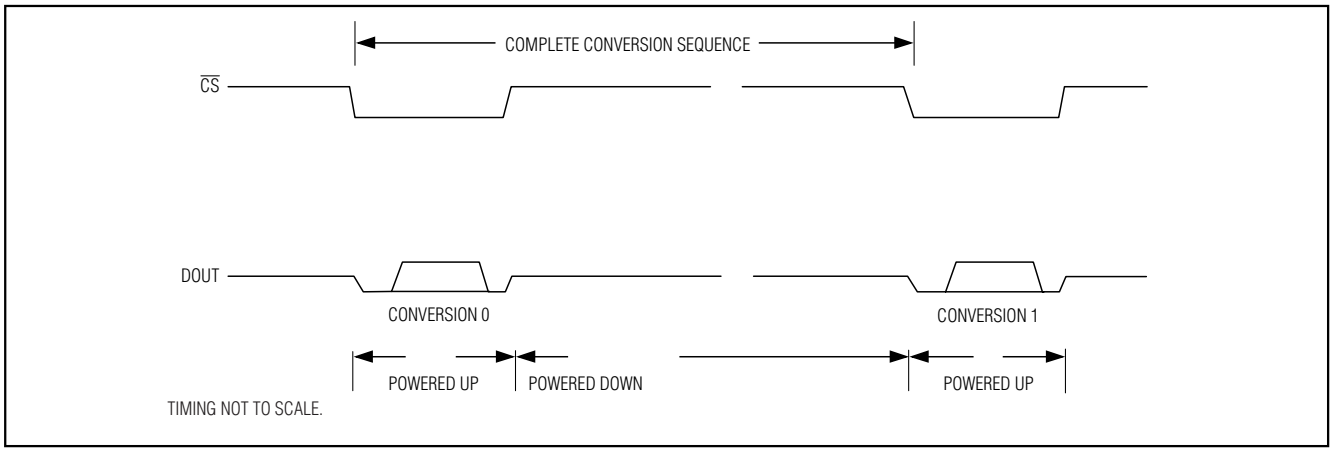


Figure 7. Shutdown Sequence

The data output from the MAX1162 is binary and Figure 8 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values (V_{REF} = 4.096V and 1LSB = 63µV or 4.096V/65536).

Applications Information

External Reference

The MAX1162 requires an external reference with a +3.8V and AV_{DD} voltage range. Connect the external reference directly to REF. Bypass REF to AGND (pin 3) with a 4.7µF capacitor. When not using a low-ESR bypass capacitor, use a 0.1µF ceramic capacitor in parallel with the 4.7µF capacitor. Noise on the reference degrades conversion accuracy.

The input impedance at REF is 40kΩ for DC currents. During a conversion the external reference at REF must deliver 100µA of DC load current and have an output impedance of 10Ω or less.

For optimal performance, buffer the reference through an op amp and bypass the REF input. Consider the MAX1162's equivalent input noise (38μV_{RMS}) when choosing a reference.

Input Buffer

Most applications require an input buffer amplifier to achieve 16-bit accuracy. If the input signal is multiplexed, switch the input channel immediately after acquisition, rather than near the end of or after a conversion (Figure 9). This allows the maximum time for the input buffer amplifier to respond to a large step change in the input signal. The input amplifier must have a slew rate of at least 2V/µs to complete the required output voltage change before the beginning of the acquisition time.

At the beginning of the acquisition, the internal sampling capacitor array connects to AIN (the amplifier output),

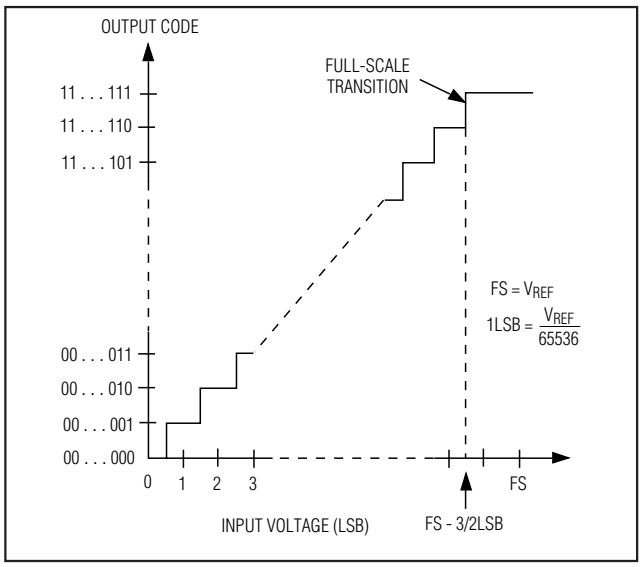


Figure 8. Unipolar Transfer Function, Full Scale (FS) = V_{REF}, Zero Scale (ZS) = GND

causing some output disturbance. Ensure that the sampled voltage has settled before the end of the acquisition time.

Digital Noise

Digital noise can couple to AIN and REF. The conversion clock (SCLK) and other digital signals active during input acquisition contribute noise to the conversion result. Noise signals synchronous with the sampling interval result in an effective input offset. Asynchronous signals produce random noise on the input, whose high-frequency components can be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the

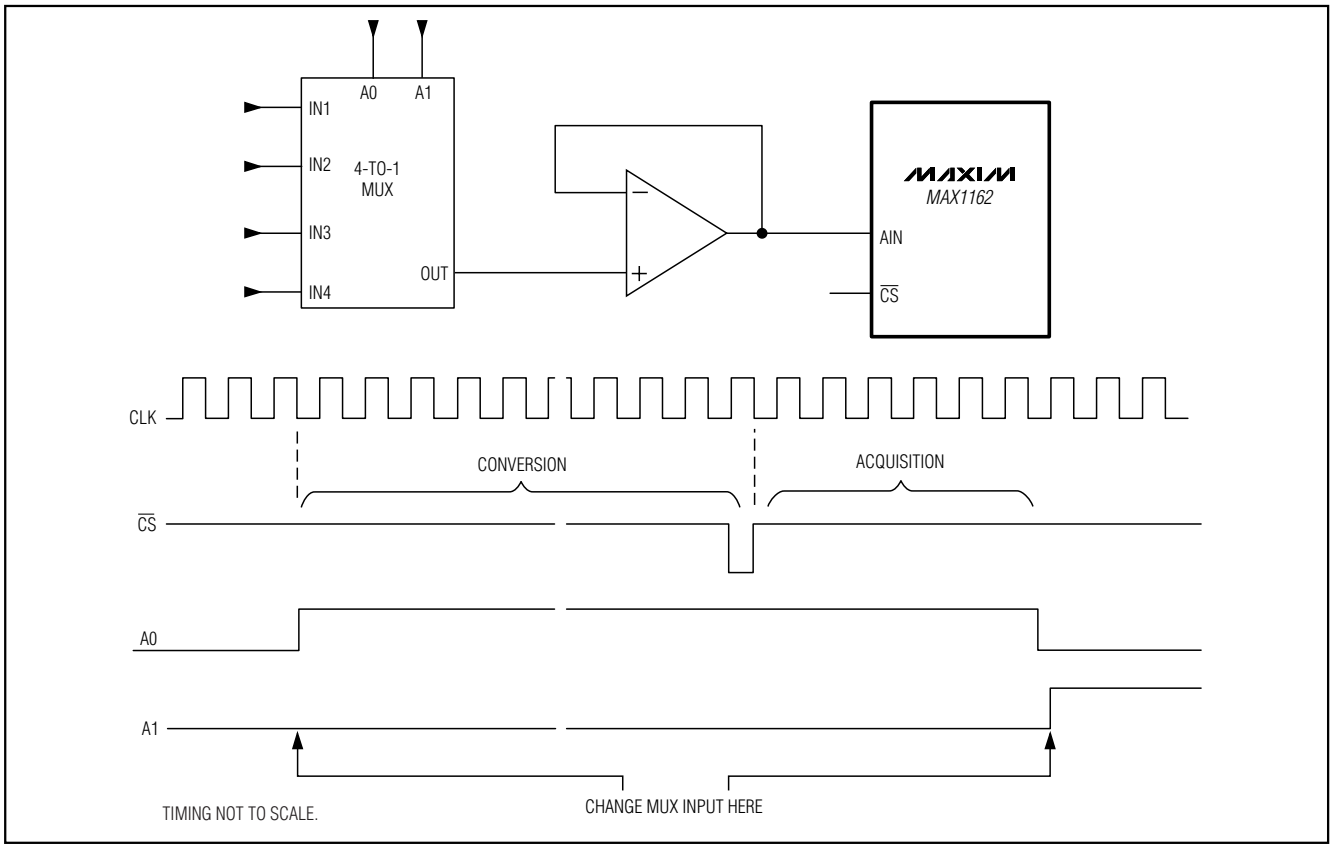


Figure 9. Change Multiplexer Input Near Beginning of Conversion to Allow Time for Slewing and Settling

noise signal) at the inputs. This requires bypassing AIN to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several MHz, or preferably both. AIN has 4MHz (typ) of bandwidth.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the MAX1162's total harmonic distortion (THD = -102dB at 1kHz) at frequencies of interest. If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration (positive input grounded) to eliminate errors from this source. Low temperature-coefficient, gain-setting resistors reduce linearity errors caused by resistance changes due to self-heating. To reduce linearity errors due to finite amplifier gain, use amplifier circuits with sufficient loop gain at the frequencies of interest.

DC Accuracy

To improve DC accuracy, choose a buffer with an offset much less than the MAX1162's offset (1mV (max) for +5V supply), or whose offset can be trimmed while maintaining stability over the required temperature range.

Serial Interfaces

The MAX1162's interface is fully compatible with SPI, QSPI, and MICROWIRE standard serial interfaces.

If a serial interface is available, establish the CPU's serial interface as master, so that the CPU generates the serial clock for the MAX1162. Select a clock frequency between 100kHz and 4.8MHz:

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
2) Activate SCLK for a minimum of 24 clock cycles. The serial data stream of eight leading zeros followed by the MSB of the conversion result begins at the falling edge of $\overline{CS}$. DOUT transitions on SCLK's falling edge and the output is available in MSB-first

16-Bit, +5V, 200ksps ADC with 10µA Shutdown

format. Observe the SCLK to DOUT valid timing characteristic. Clock data into the µP on SCLK's rising edge.

3) Pull $\overline{CS}$ high at or after the 24th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the least significant bit (D0 = LSB).

4) With $\overline{CS}$ high, wait at least 50ns (t_{CSW}) before starting a new conversion by pulling $\overline{CS}$ low. A conversion can be aborted by pulling $\overline{CS}$ high before the conversion ends. Wait at least 50ns before starting a new conversion.

Data can be output in three 8-bit sequences or continuously. The bytes contain the results of the conversion padded with eight leading zeros before the MSB. If the serial clock has not been idled after the LSB (D0) and $\overline{CS}$ has been kept low, DOUT sends trailing zeros.

SPI and MICROWIRE Interfaces

When using the SPI (Figure 10a) or MICROWIRE (Figure 10b) interfaces, set CPOL = 0 and CPHA = 0. Conversion begins with a falling edge on $\overline{CS}$ (Figure 10c). Three consecutive 8-bit readings are necessary to obtain the entire 16-bit result from the ADC. DOUT data transitions on the serial clock's falling edge. The first 8-bit data stream contains all leading zeros. The second 8-bit data stream contains the MSB through D8. The third 8-bit data stream contains D7 through D0.

QSPI Interface

Using the high-speed QSPI interface with CPOL = 0 and CPHA = 0, the MAX1162 supports a maximum f_{SCLK} of 4.8MHz. Figure 11a shows the MAX1162 connected to a QSPI master and Figure 11b shows the associated interface timing.

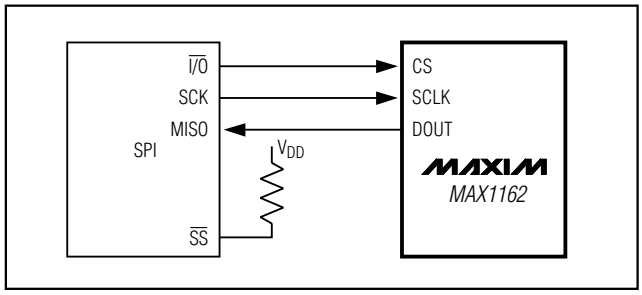


Figure 10a. SPI Connections

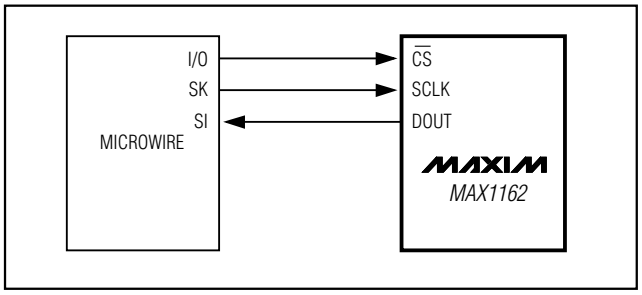


Figure 10b. MICROWIRE Connections

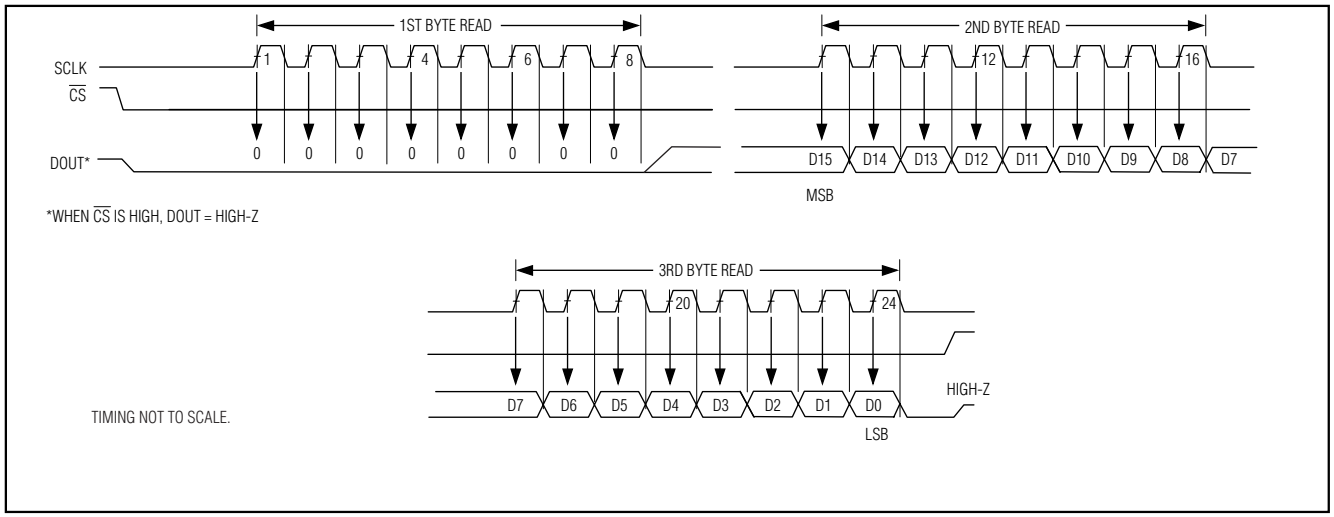


Figure 10c. SPI/MICROWIRE Interface Timing Sequence (CPOL = CPHA = 0)

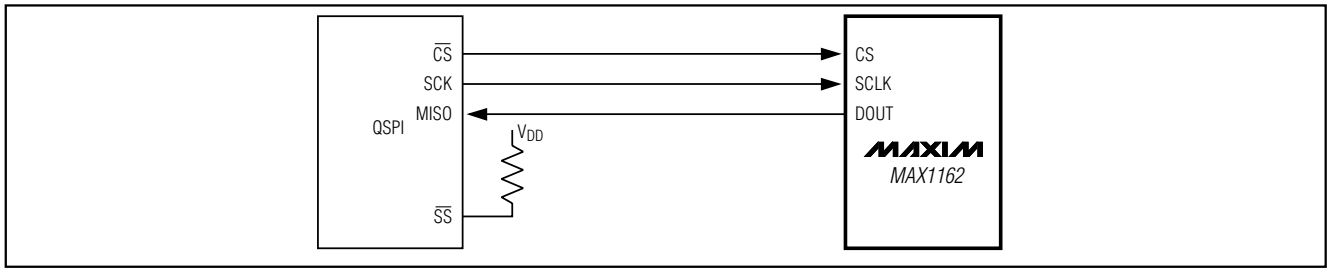


Figure 11a. QSPI Connections

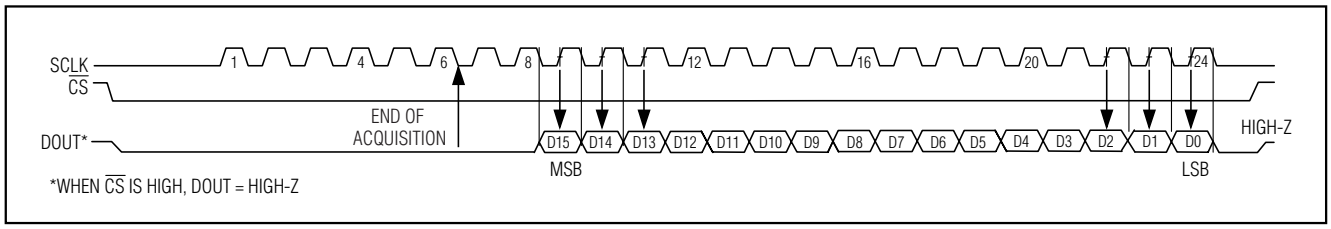


Figure 11b. QSPI Interface Timing Sequence (CPOL = CPHA = 0)

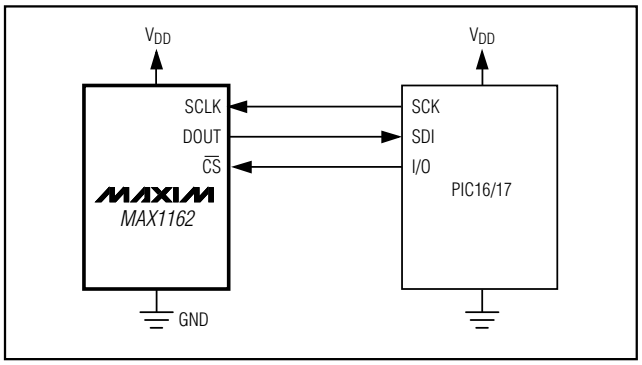


Figure 12a. SPI Interface Connection for a PIC16/PIC17

PIC16 with SSP Module and PIC17 Interface

The MAX1162 is compatible with a PIC16/PIC17 microcontroller (µC) using the synchronous serial-port (SSP) module.

To establish SPI communication, connect the controller as shown in Figure 12a. Configure the PIC16/PIC17 as system master, by initializing its synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 1 and 2.

In SPI mode, the PIC16/PIC17 µC allows 8 bits of data to be synchronously transmitted and received simulta-

Table 1. Detailed SSPCON Register Contents

CONTROL BIT		MAX1162 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	BIT7	X	Write Collision Detection Bit
SSPOV	BIT6	X	Receive Overflow Detect Bit
SSPEN	BIT5	1	Synchronous Serial-Port Enable Bit: 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial port pins.
CKP	BIT4	0	Clock Polarity Select Bit. CKP = 0 for SPI master mode selection.
SSPM3	BIT3	0	Synchronous Serial-Port Mode Select Bit. Sets SPI master mode and selects $f_{CLK} = f_{OSC} / 16$.
SSPM2	BIT2	0	
SSPM1	BIT1	0	
SSPM0	BIT0	1	

X = Don't care.

Table 2. Detailed SSPSTAT Register Contents

CONTROL BIT		MAX1162 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPSTAT)
SMP	BIT7	0	SPI Data Input Sample Phase. Input data is sampled at the middle of the data output time.
CKE	BIT6	1	SPI Clock Edge Select Bit. Data is transmitted on the rising edge of the serial clock.
D/A	BIT5	X	Data Address Bit
P	BIT4	X	Stop Bit
S	BIT3	X	Start Bit
R/W	BIT2	X	Read/Write Bit Information
UA	BIT1	X	Update Address
BF	BIT0	X	Buffer Full Status Bit

X = Don't care.

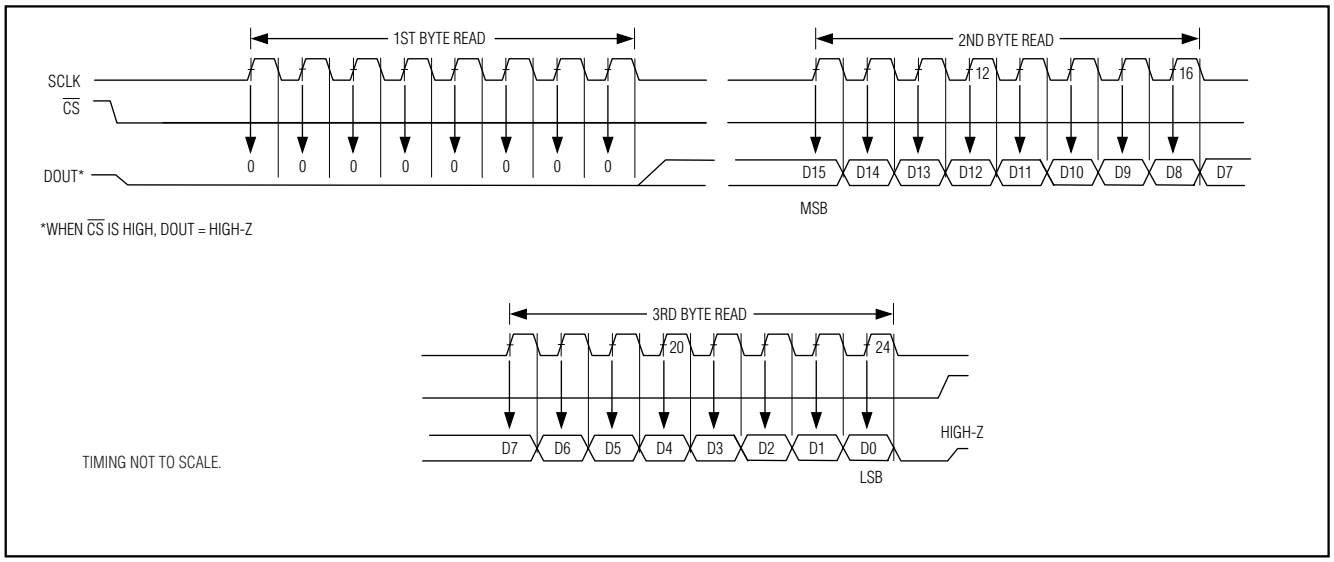


Figure 12b. SPI Interface Timing with PIC16/PIC17 in Master Mode (CKE = 1, CKP = 0, SMP = 0, SSPM3 - SSPM0 = 0001)

neously. Three consecutive 8-bit readings (Figure 12b) are necessary to obtain the entire 16-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µC on SCLK's rising edge. The first 8-bit data stream contains all zeros. The second 8-bit data stream contains the MSB through D8. The third 8-bit data stream contains bits D7 through D0.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-fit straight line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nulled. The static linearity parameters for the MAX1162 are measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Definitions

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between samples. Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when the actual sample is taken.

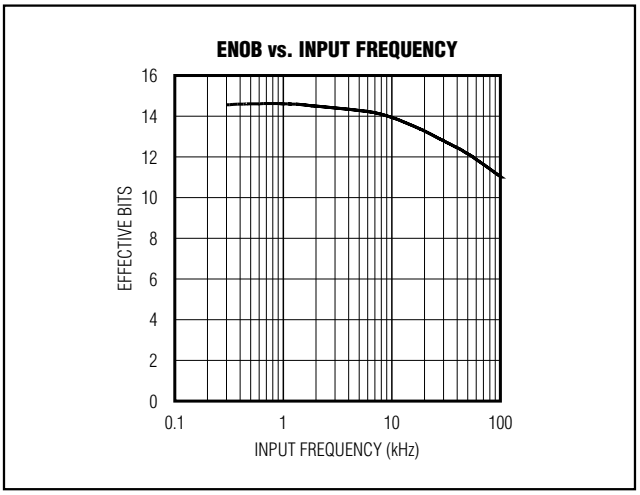


Figure 13. Effective Number of Bits vs. Input Frequency

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADCs resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals, excluding the DC offset.

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

Effective number of bits (ENOB) indicate the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Figure 13 shows the effective number of bits as a function of the MAX1162's input frequency.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

Supplies, Layout, Grounding, and Bypassing

Use PC boards with separate analog and digital ground planes. Do not use wire-wrap boards. Connect the two ground planes together at the MAX1162 (pin 3). Isolate the digital supply from the analog with a low-value resistor (10Ω) or ferrite bead when the analog and digital supplies come from the same source (Figure 14).

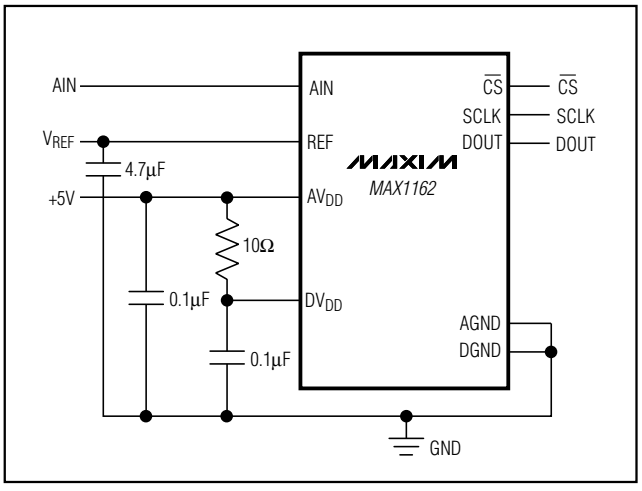


Figure 14. Powering AV_{DD} and DV_{DD} from a Single Supply

16-Bit, +5V, 200ksps ADC with 10µA Shutdown

Constraints on sequencing the power supplies and inputs are as follows:

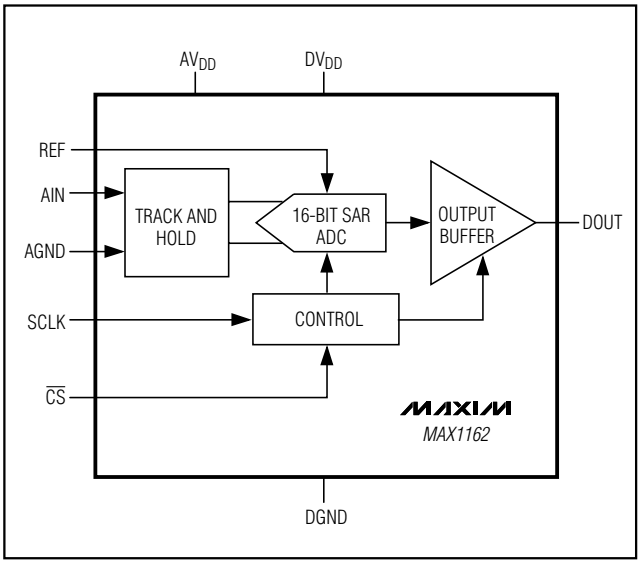
- Apply AGND before DGND.
- Apply AIN and REF after AV_{DD} and AGND are present.
- DV_{DD} is independent of the supply sequencing.

Ensure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05Ω creates an error voltage of about 250µV, 4LSB error with a +4V full-scale system.

The board layout should ensure that digital and analog signal lines are kept separate. Do not run analog and digital (especially the SCLK and DOUT) lines parallel to one another. If one must cross another, do so at right angles.

The ADCs high-speed comparator is sensitive to high-frequency noise on the AV_{DD} power supply. Bypass an excessively noisy supply to the analog ground plane with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor. Keep capacitor leads short for best supply-noise rejection.

Functional Diagram



Chip Information

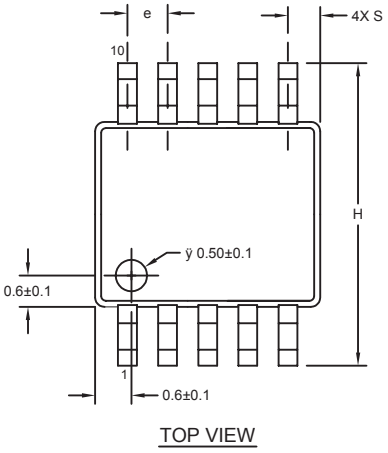
TRANSISTOR COUNT: 12,100

PROCESS: BiCMOS

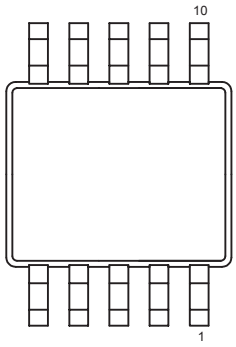
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

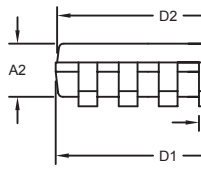


TOP VIEW

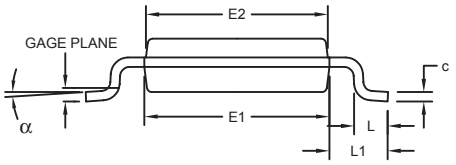


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

Note: Contact factory for DFN package outline.