

BUK75/764R0-55B

TrenchMOS™ standard level FET

Rev. 02 — 30 September 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive TrenchMOS™ technology.

Product availability:

BUK754R0-55B in SOT78 (TO-220AB)

BUK764R0-55B in SOT404 (D²-PAK).

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Standard level compatible.

1.3 Applications

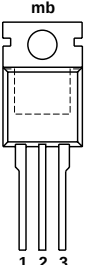
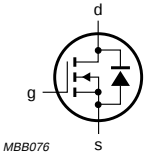
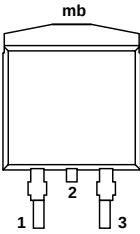
- Automotive systems
- Motors, lamps and solenoids
- 12 V and 24 V loads
- General purpose power switching.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.2 \text{ J}$
- $I_D \leq 75 \text{ A}$
- $R_{DS(on)} = 3.4 \text{ m}\Omega$ (typ)
- $P_{tot} \leq 300 \text{ W}$.

2. Pinning information

Table 1: Pinning - SOT78 and SOT404 simplified outlines and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 MBK106	 MBB076
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		
		 MBK116	
		SOT78 (TO-220AB)	SOT404 (D ² -PAK)

[1] It is not possible to make connection to pin 2 of the SOT404 package.

3. Limiting values

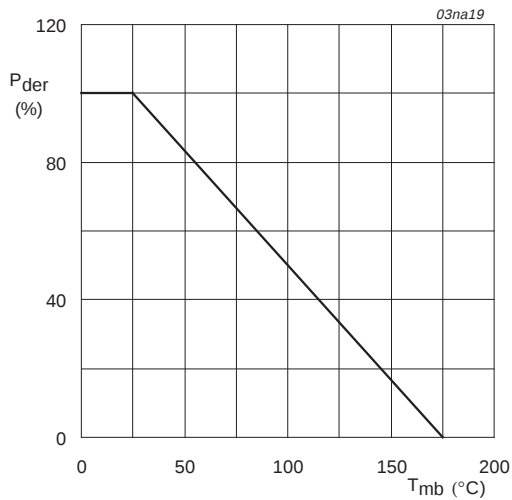
Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	[1] -	193	A
			[2] -	75	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	774	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Figure 1	-	300	W
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$
T_j	operating junction temperature		-55	+175	$^\circ\text{C}$
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	[1] -	193	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	774	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A}$; $V_{DS} \leq 55\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$; starting $T_{mb} = 25\text{ }^\circ\text{C}$	-	1.2	J

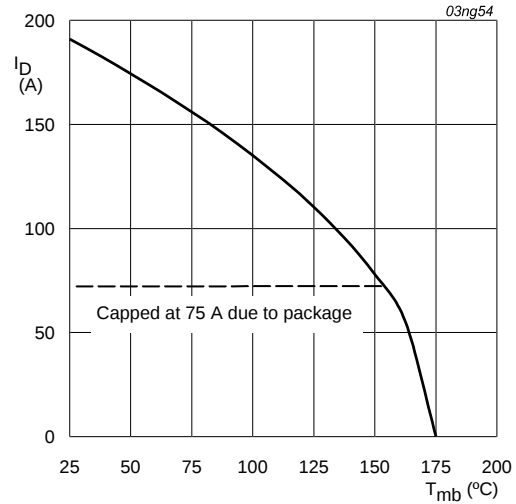
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package



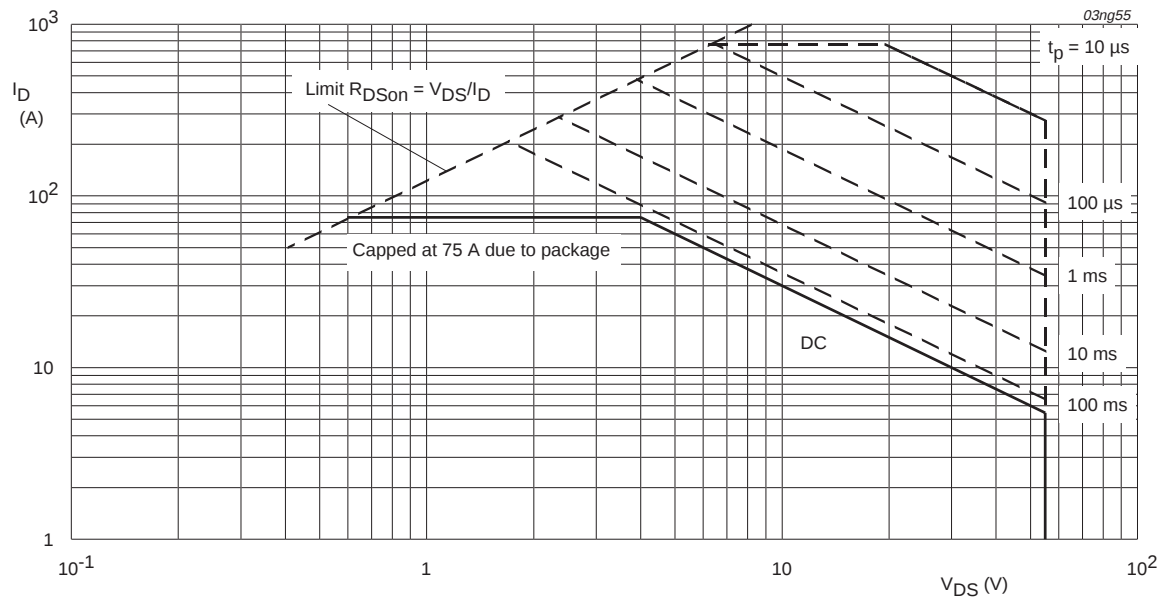
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT404	mounted on a printed circuit board; minimum footprint	-	50	-	K/W

4.1 Transient thermal impedance

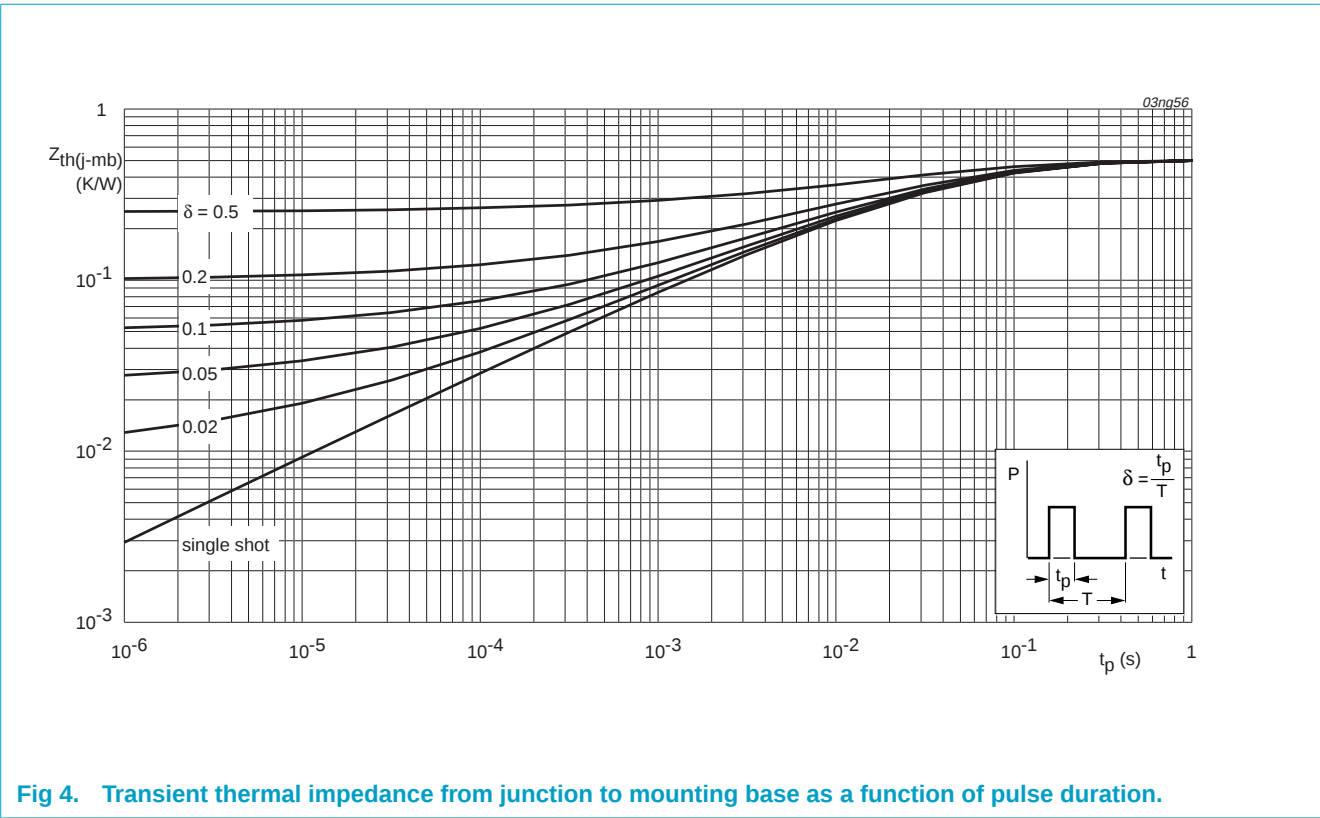


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

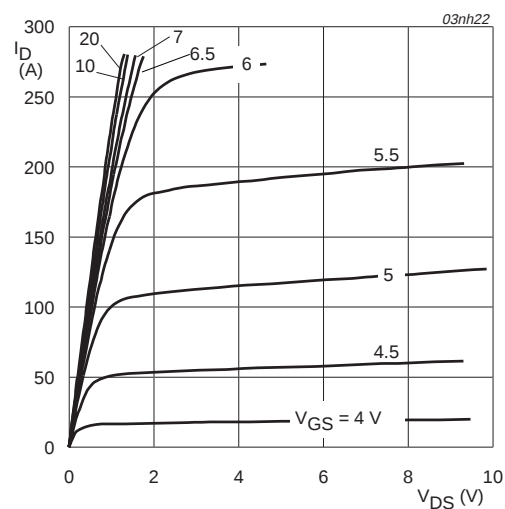
Table 4: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$				
		$T_J = 25\text{ }^{\circ}\text{C}$	55	-	-	V
		$T_J = -55\text{ }^{\circ}\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_J = 25\text{ }^{\circ}\text{C}$	2	3	4	V
		$T_J = 175\text{ }^{\circ}\text{C}$	1	-	-	V
		$T_J = -55\text{ }^{\circ}\text{C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_J = 25\text{ }^{\circ}\text{C}$	-	0.02	1	μA
		$T_J = 175\text{ }^{\circ}\text{C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8				
		$T_J = 25\text{ }^{\circ}\text{C}$	-	3.4	4.0	m Ω
		$T_J = 175\text{ }^{\circ}\text{C}$	-	-	8	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}$; $V_{DD} = 44\text{ V}$; $I_D = 25\text{ A}$; Figure 14	-	86	-	nC
Q_{gs}	gate-to-source charge		-	18	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	25	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 12	-	5082	6776	pF
C_{oss}	output capacitance		-	1054	1265	pF
C_{rss}	reverse transfer capacitance		-	289	396	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$	-	23	-	ns
t_r	rise time		-	51	-	ns
$t_{d(off)}$	turn-off delay time		-	71	-	ns
t_f	fall time		-	41	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
		from contact screw on mounting base to centre of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to centre of die SOT404	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

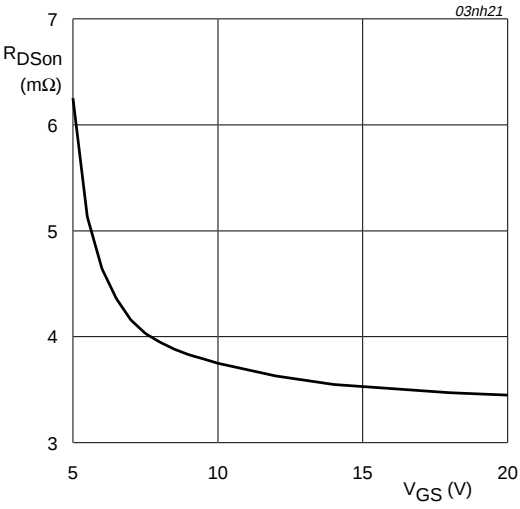
Table 4: Characteristics...continued
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 40 A; V _{GS} = 0 V; Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	95	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	251	-	nC



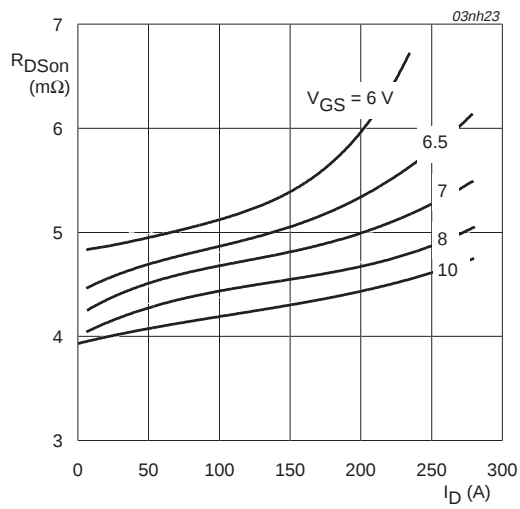
$T_J = 25\text{ }^{\circ}\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



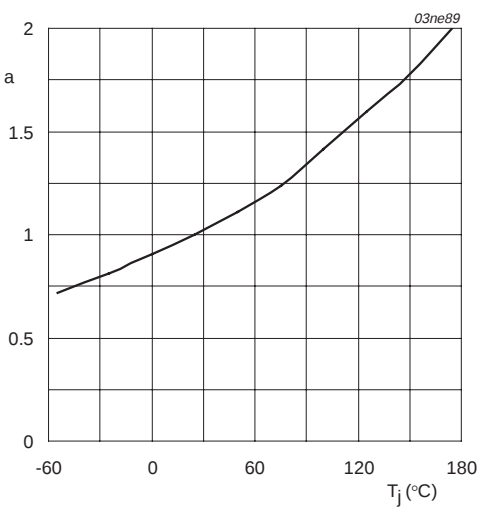
$T_J = 25\text{ }^{\circ}\text{C}$; $I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



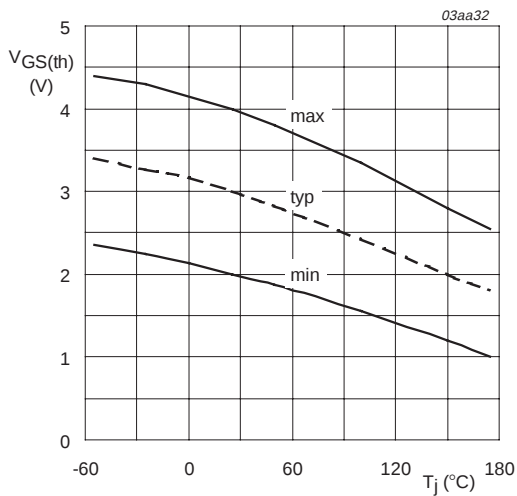
$T_J = 25\text{ }^{\circ}\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



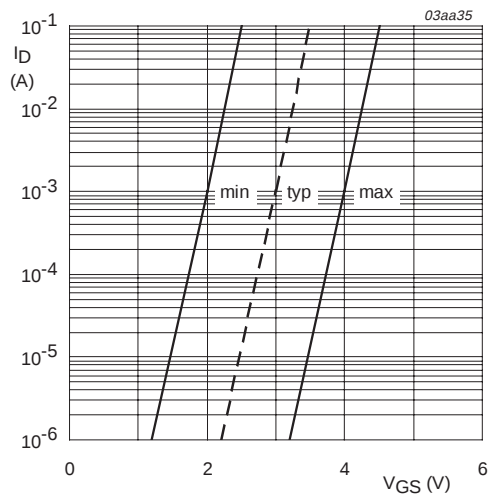
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



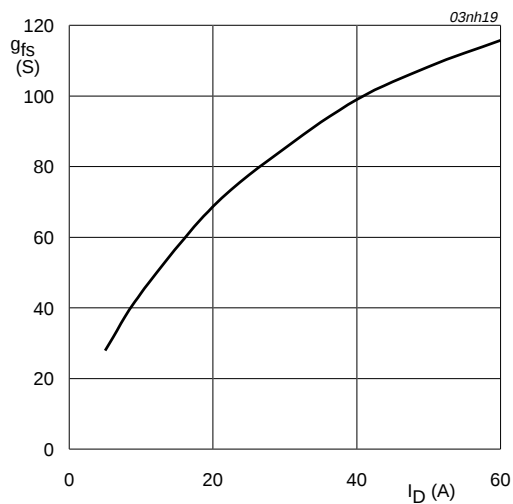
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



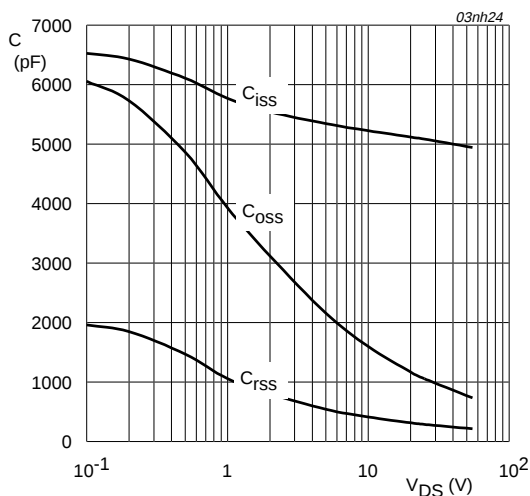
$T_j = 25 \text{ °C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



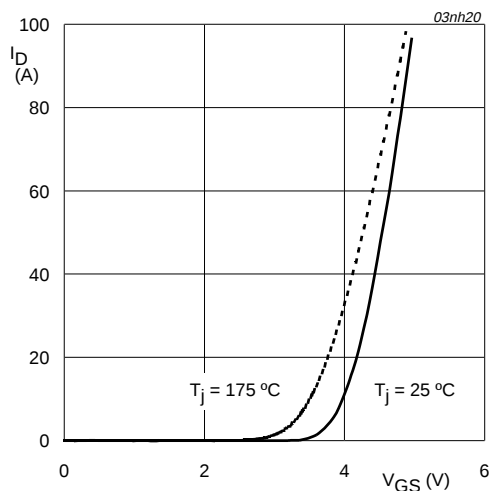
$T_j = 25 \text{ °C}$; $V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



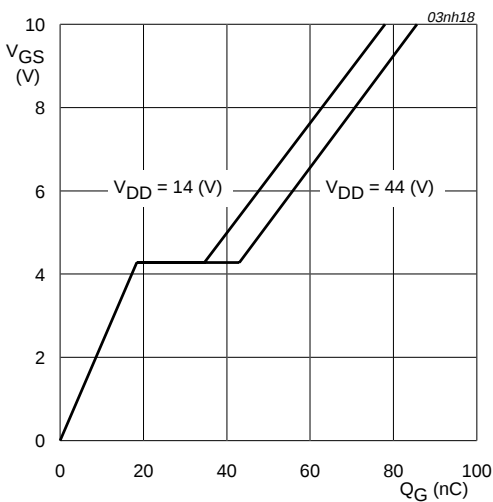
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



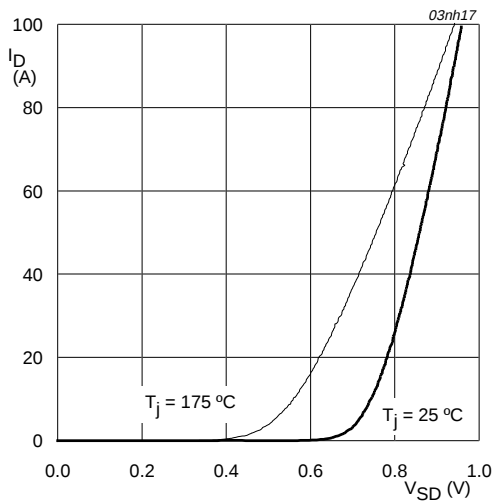
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_J = 25\text{ °C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



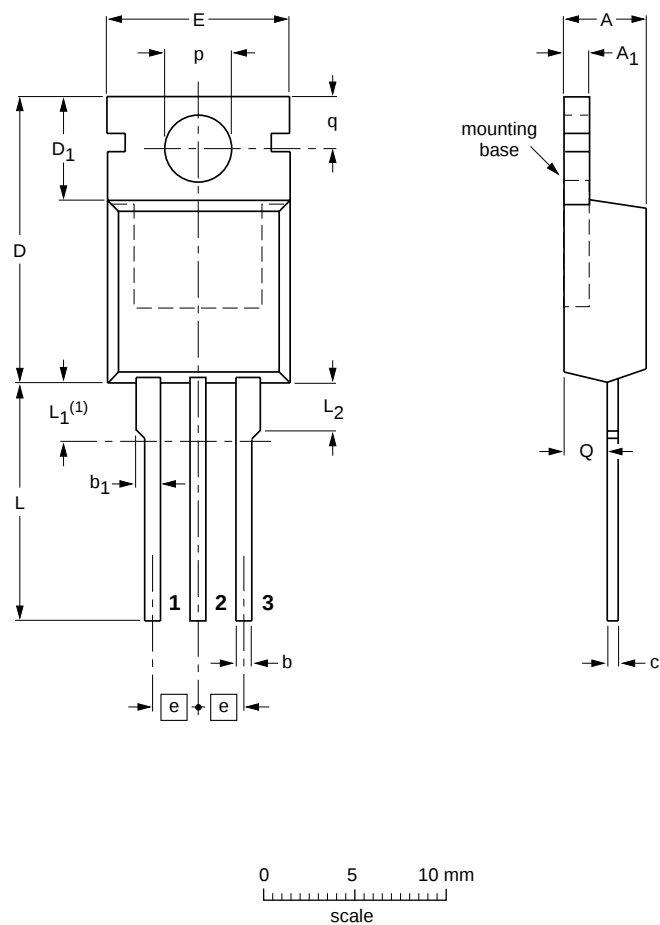
$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ ⁽¹⁾	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

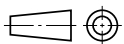
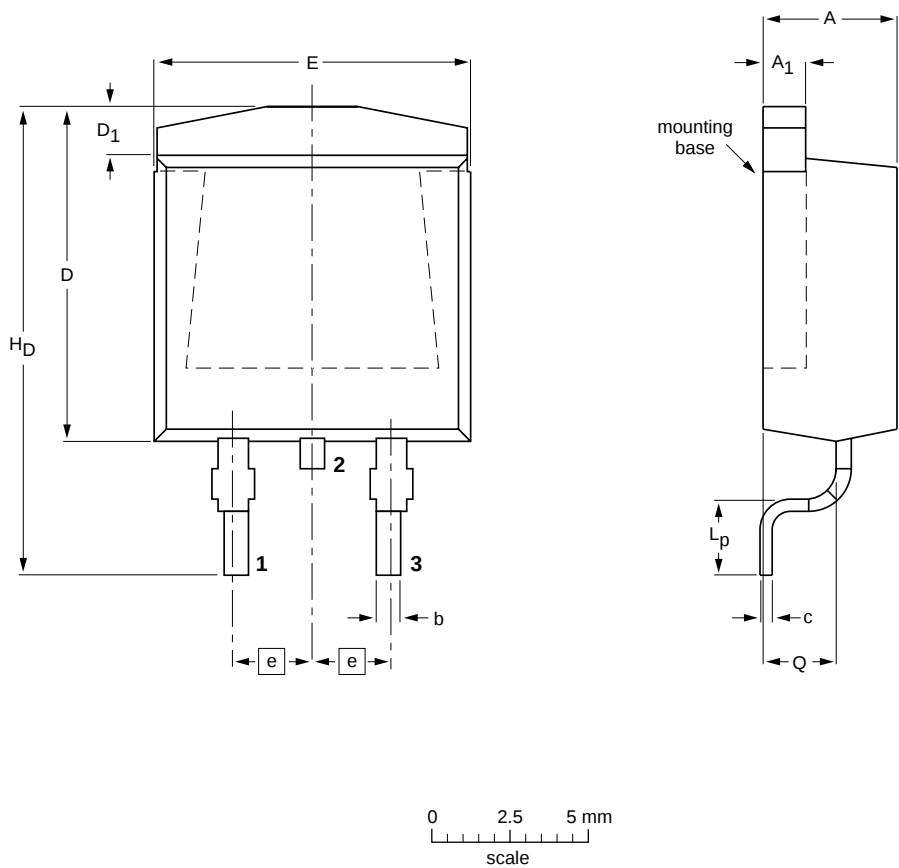
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07 01-02-16

Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						-99-06-25 01-02-12

Fig 17. SOT404 (D²-PAK)

7. Soldering

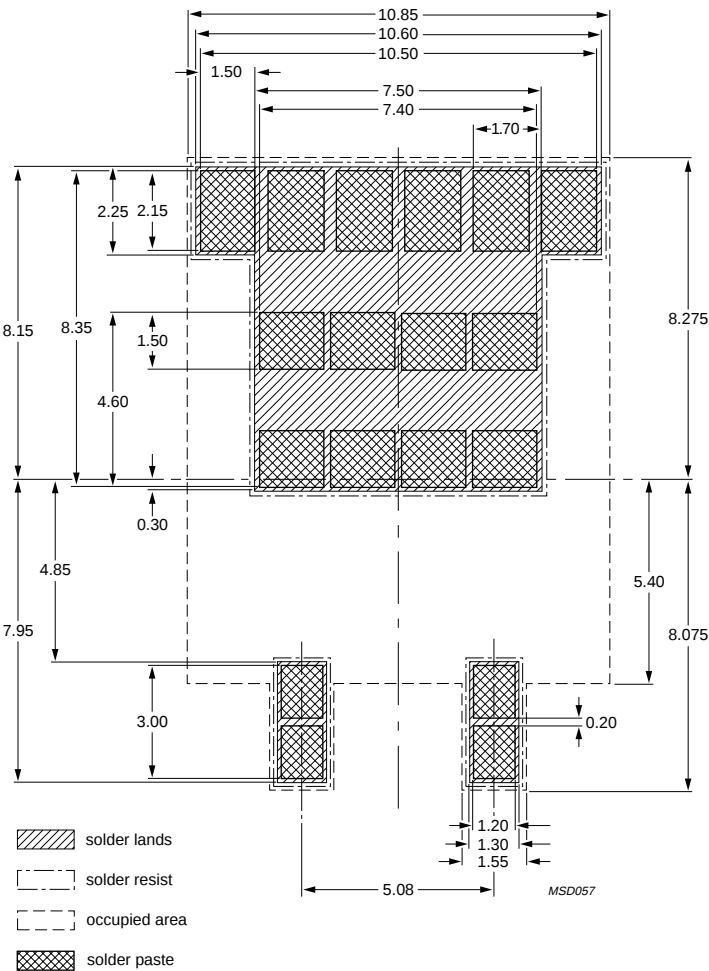


Fig 18. Reflow soldering footprint for SOT404.

8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20020930	-	Product data (9397 750 10276) Modifications: Description in Section 1 changed from: N-channel enhancement mode field-effect power transistor in a plastic package using generation three TrenchMOS™ technology, featuring very low on-state resistance. to: N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive TrenchMOS™ technology.
01	20020328	-	Product data (9397 750 09492)

9. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

11. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

12. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1 **Product profile** 1

1.1 Description 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data. 1

2 **Pinning information** 1

3 **Limiting values** 2

4 **Thermal characteristics** 4

4.1 Transient thermal impedance 4

5 **Characteristics** 5

6 **Package outline** 10

7 **Soldering** 12

8 **Revision history** 13

9 **Data sheet status** 14

10 **Definitions** 14

11 **Disclaimers** 14

12 **Trademarks** 14



PHILIPS

Let's make things better.