

Description

The MK1705A generates a low EMI output clock from a clock or crystal input. The part is designed to dither the LCD interface clock or other clocks for ATI's flat panel graphics controllers. The device uses ICS/MicroClock's proprietary mixture of analog and digital Phase-Locked Loop (PLL) technology to synthesize the frequency, and our patented technique to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

The MK1705A is designed to have the output spread centered around the input frequency. Refer to the MK1704A for spreading down from the input frequency, or the MK1714-0x for a crystal input and the widest selection of spread rates and multipliers.

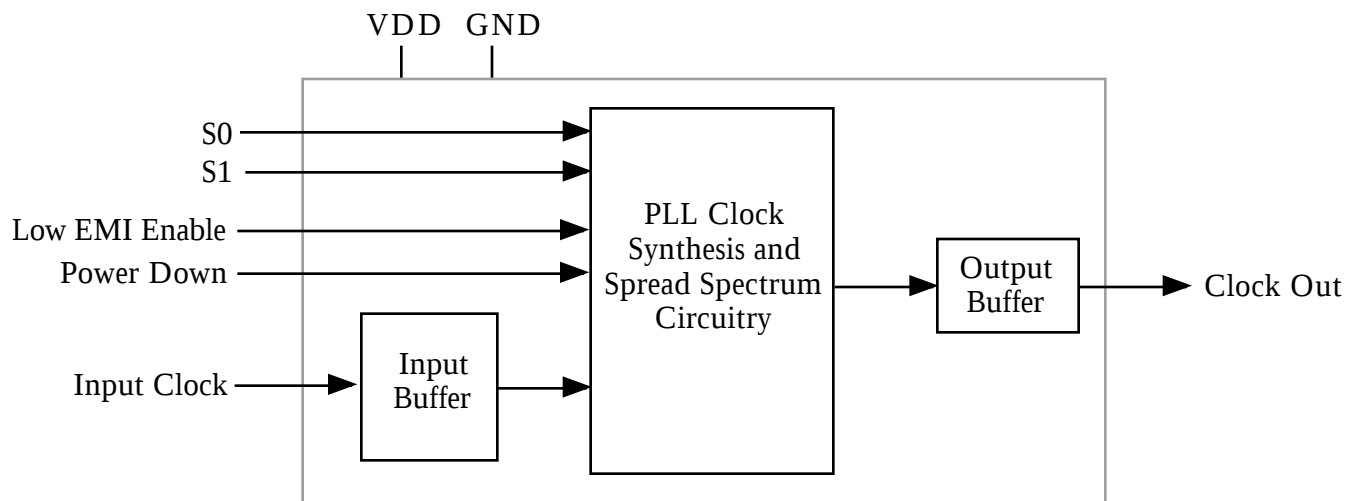
We offer many other clocks for computers and computer peripherals. Consult us when you need to remove crystals and oscillators from your board.

Features

- Packaged in 8 pin SOIC
- Provides a spread spectrum output clock
- Supports ATI's flat panel controllers
- Accepts a clock input, provides same frequency dithered output
- Good for all VGA modes from 40 to 167 MHz
- Peak reduction by 7dB - 14 dB typical on 3rd-19th odd harmonics
- Low EMI feature can be disabled
- 3.3 V or 5 V $\pm 10\%$ supply voltage
- Advanced, low power CMOS process

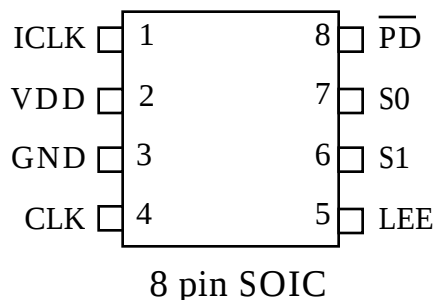


Block Diagram





Pin Assignment



Clock Output Select Table

S1 pin 6	S0 pin 7	Input/Output Range pin 1/pin 4	Frequency spread vs. CLK
0	0	40 to 167 MHz	Center $\pm 1.25\%$
0	1	60 to 167 MHz	Center $\pm 0.5\%$
1	0	Test	Test
1	1	40 to 100 MHz	Center $\pm 1\%$

Pin Descriptions

Pin #	Name	Type	Description
1	ICLK	I	Connect to graphics input clock
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	CLK	O	Spread spectrum Clock Output per table above.
5	LEE	I	Low EMI Enable. Turns on the spread spectrum when high. Internal pull-up.
6	S1	I	Frequency Select 1 Input. Selects spread amount and CLK range per table above. Internal pull-up.
7	S0	I	Frequency Select 0 Input. Selects spread amount and CLK range per table above. Internal pull-up.
8	$\overline{PD}$	I	Power Down. Stops output low when this pin is low. Internal pull-up.

Key: I = Input, O = output, P = power supply connection

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD and GND on pins 2 and 3 as close to the chip as possible, and a 33Wseries terminating resistor may be used on the clock output if the trace is longer than 1 inch.



Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+.5V	V
Clock Outputs	Referenced to GND	-0.5		VDD+.5V	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (at 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK		(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK			VDD/2	(VDD/2)-1	V
Output High Voltage, VOH, CMOS	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Operating Supply Current, IDD, 5V	No Load		20		mA
Operating Supply Current, IDD, 3.3V	No Load		15		mA
Input Capacitance	S0, S1, $\overline{\text{PD}}$, LEE pins		7		pF
AC CHARACTERISTICS (at 5.0V unless otherwise noted)					
Input Clock Frequency			40 - 167		MHz
Input Clock Duty Cycle	Time above VDD/2	20		80	%
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	Time above 1.5V	40	50	60	%
Output Clock Frequency Variation from Mean	LEE high		±0.5 to ±1.25		%
EMI Peak Frequency Reduction	3rd-19th odd harmonics		7 to 14		dB

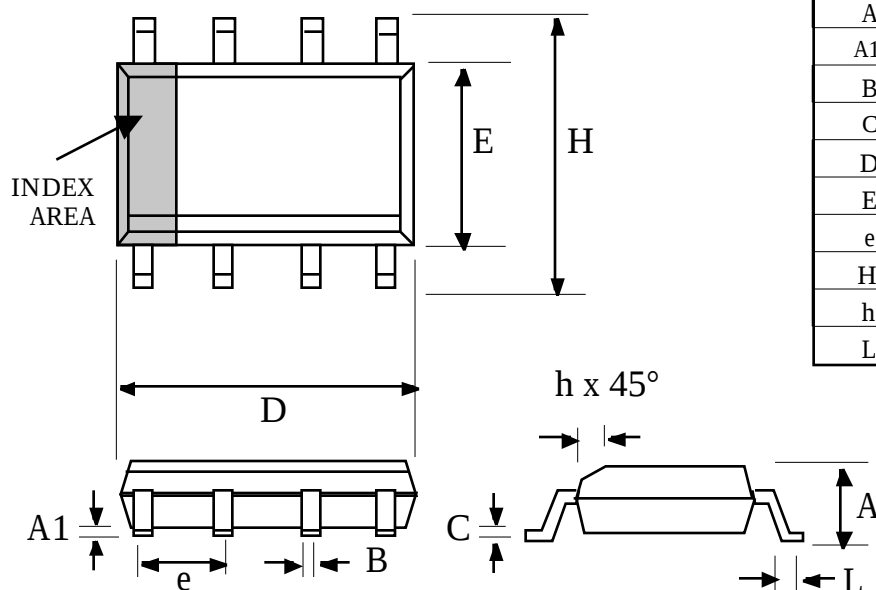
Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Typical values are at 25°C.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

8 pin SOIC



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK1705A	MK1705A	8 pin SOIC	0 to 70 °C
MK1705ATR	MK1705A	Add tape and reel	0 to 70 °C

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