HN28F101 Series

131072-word × 8-bit CMOS Flash Memory

The Hitachi HN28F101 is a 131072-word x 8-bit CMOS flash Memory, realizing on-board programming. It programs or erases data with only on-board power supply (12 V V_{PP} supply/5 V V_{CC} supply). It programs data with fast programming algorithm by command inputs. It has two types of erase algorithm : automatic erase and fast erase by command inputs. Automatic erase function can erase data automatically without external control only by inputting trigger pulse and inform erase completion to CPU by status polling. The HN28F101 can control programming erase algorithm externally.

Features

- On-board power supply (V_{CC}/V_{PP})
  - V_{CC} = 5 V ± 10%
  - V_{PP} = V_{SS} to V_{CC} (Read)
  - V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast access time
  - 120 ns/150 ns/200 ns (max)
- Programming function
  - Byte programming
  - Programming time: 25 µs typ/byte
  - Address, data, control latch function
- On-board automatic erase function
  - Chip erase
  - Erase time: 1 s typ
  - Address, data, control latch function
  - Status polling function
- Low power dissipation
  - I_{CC} = 10 mA typ (Read)
  - I_{CC} = 20 µA max (Standby)
  - I_{PP} = 30 mA typ (Auto erase/Program)
  - I_{PP} = 20 µA max (Read/Standby)
- Erasing endurance: 10,000 times
- Pin arrangement: 32-pin JEDEC standard
- Package
  - 32-pin DIP
  - 32-pin SOP
  - 32-pin TSOP
  - 32-pin PLCC

Ordering Information

Type No.	Access time	Package
HN28F101P-12	120 ns	32-pin plastic DIP (DP-32)
HN28F101P-15	150 ns	
HN28F101P-20	200 ns	
HN28F101FP-12	120 ns	32-pin plastic SOP (FP-32D)
HN28F101FP-15	150 ns	
HN28F101FP-20	200 ns	
HN28F101T-12	120 ns	32-pin plastic TSOP (TFP-32DA)
HN28F101T-15	150 ns	
HN28F101T-20	200 ns	
HN28F101R-12	120 ns	32-pin plastic TSOP (TFP-32DAR)
HN28F101R-15	150 ns	
HN28F101R-20	200 ns	
HN28F101CP-12	120 ns	32-pin PLCC (CP-32)
HN28F101CP-15	150 ns	
HN28F101CP-20	200 ns	

Ordering Information (cont.)

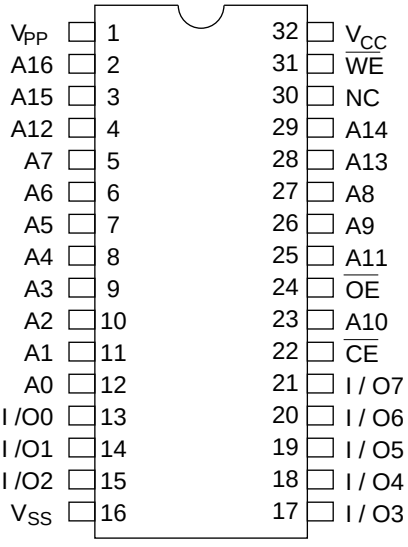
Type No.	Access time	Package
HN28F101TD-12	120 ns	32-pin plastic TSOP (TFP-32D)
HN28F101TD-15	150 ns	
HN28F101TD-20	200 ns	
HN28F101RD-12	120 ns	32-pin plastic TSOP (TFP-32DR)
HN28F101RD-15	150 ns	
HN28F101RD-20	200 ns	

Pin Description

Pin name	Function
A0-A16	Address
I/O0-I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

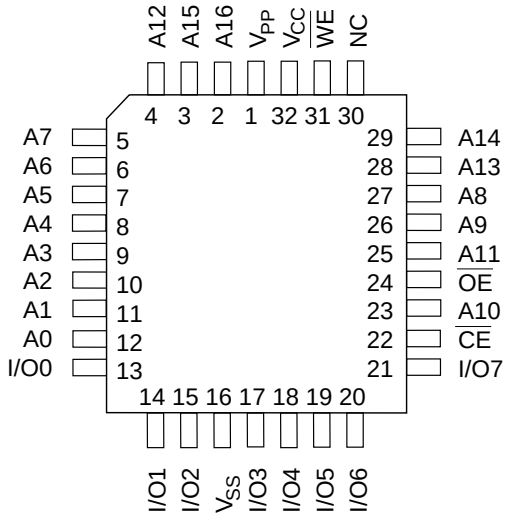
Pin Arrangement

HN28F101P/FP Series



(Top view)

HN28F101CP Series



(Top view)

Pin Arrangement (cont)

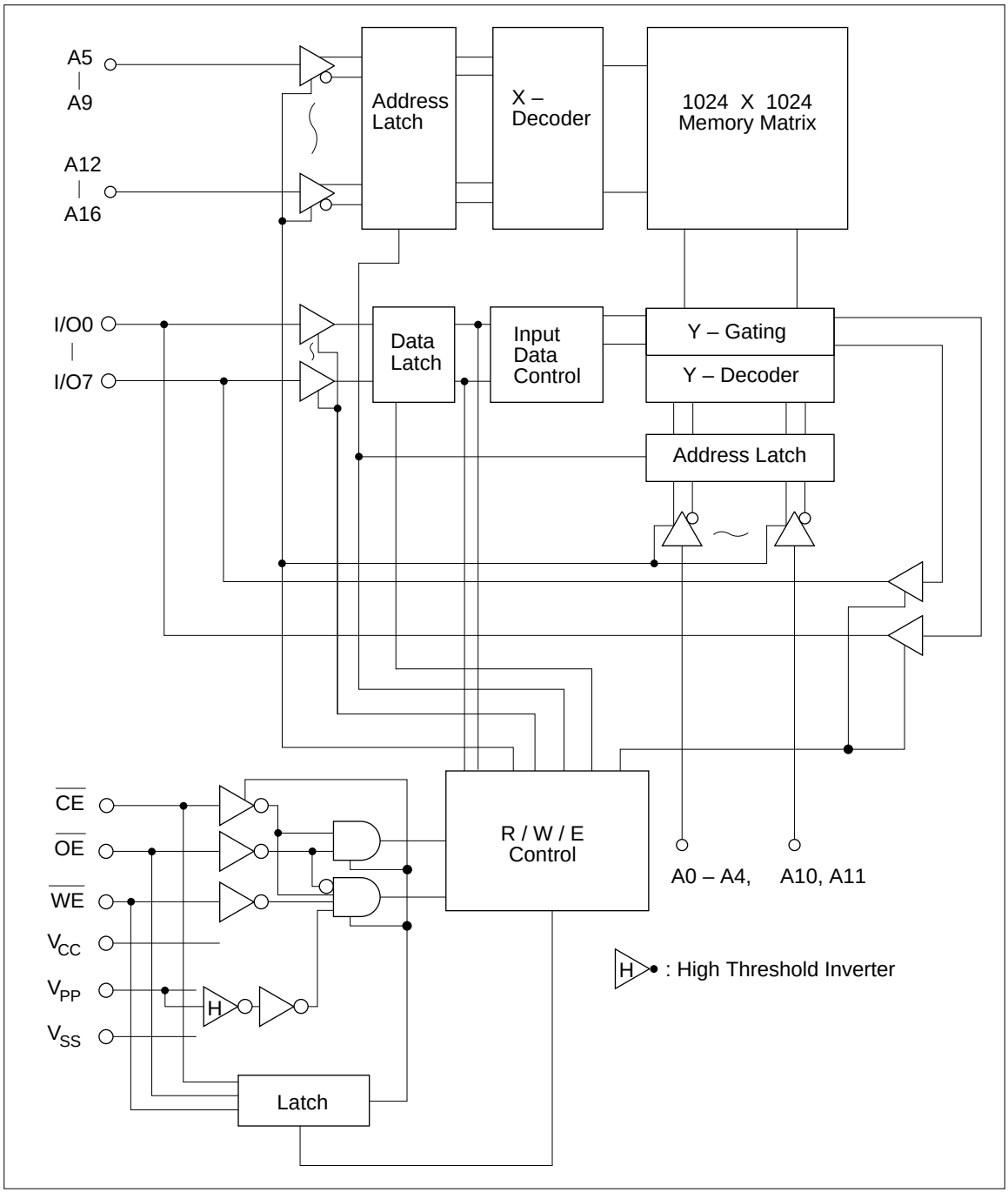
HN28F101T/TD Series

(Top view)

HN28F101R/RD Series

(Top view)

Block Diagram



Mode Selection

Mode	DIP, SOP, PLCC TSOP	Pin V_{PP} (1) (9)	$\overline{CE}$ (22) (30)	$\overline{OE}$ (24) (32)	$\overline{WE}$ (31) (7)	A9 (26) (2)	I/O0 – I/O7 (13 – 15, 17 – 21) (21 – 23, 25 – 29)
Read	Read	V_{CC}*6	V_{IL}	V_{IL}	V_{IH}	A9	Dout
	Output disable	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	Standby	V_{CC}	V_{IH}	X	X	X	High-Z
	Identifier*1	V_{CC}	V_{IL}	V_{IL}	V_{IH}	VH*2	ID
Command program	Read*3,*5	V_{PP}	V_{IL}	V_{IL}	V_{IH}	A9	Dout
	Output disable	V_{PP}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	Standby	V_{PP}	V_{IH}	X	X	X	High-Z
	Write*4	V_{PP}	V_{IL}	V_{IH}	V_{IL}	A9	Din

Notes:
1. Device identifier code can be output in command programming mode. Refer to the table of command address and data input.
2. V_H: 11.5 $\leq V_H \leq$ 12.5V.
3. Data can be read when 12 V is applied to V_{PP}. Device identifier code can be output by command inputs.
4. Refer to the table of command address and data input. Data is programmed, erased, or verified after mode setting by command inputs.
5. Status of automatic erase can be verified in this mode. Status outputs on I/O7. I/O0 to I/O6 are in high impedance state.
6. X : V_{IH} or V_{IL}. V_{PP} = 0 V to V_{CC}

Command Address and Data Input

Command	The number of cycle	First cycle			Second cycle		
		Operation mode[*1]	Address[*2]	Data[*3]	Operation mode[*1]	Address[*2]	Data[*3]
Read (memory)[*4]	1	Write	X	00H	Read	RA	Dout
Read identified codes	2	Write	X	90H	Read	IA	ID
Setup erase/erase[*5]	2	Write	X	20H	Write	X	20H
Erase verify[*5]	2	Write	EA	A0H	Read	X	EVD
Setup auto erase/ auto erase[*6]	2	Write	X	30H	Write	X	30H
Setup program/ program[*7]	2	Write	X	40H	Write	PA	PD
Program verify[*7]	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

Notes:
1. Refer to command program mode in mode selection about operation mode.
2. Refer to device identifier mode. IA = Identifier address, PA = Programming address, EA = Erase verify address, RA = Read address
3. Refer to device identifier mode. PA are latched by programming command. ID = Identifier output code, PD = Programming data, PVD = Programming verify output data, EVD = Erase verify output data
4. Command latch default value when applying 12 V to V_{PP} is “00H”. Device is in read mode after V_{PP} is set 12 V (before other command is input).
5. All data in chip are erased. Erase data according to fast high-reliability erase flowchart.
6. All data in chip are erased. Data are erased automatically by internal logic circuit. External erase verify is not required. Erasure completion must be verified by status polling after automatic erase starts.
7. Program data according to fast high-reliability programming flowchart.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltage[*1]	Vin, Vout	–0.6[*2] to +7.0	V
V_{PP} voltage[*1]	V_{PP}	–0.6 to +14.0	V
V_{CC} voltage[*1]	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range[*3]	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –2.0 V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 10%, $V_{PP} = V_{CC}$~V_{SS}, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 to V_{CC}
V_{PP} current	I_{PP1}	—	—	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	—	20	µA	$\overline{CE}$ = V_{CC}
Operating V_{CC} current	I_{CC1}	—	6	15	mA	Iout = 0 mA, f = 1 MHz
	I_{CC2}	—	10	30	mA	Iout = 0 mA, f = 8 MHz
Input voltage*3	V_{IL}	–0.3*1	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} + 0.3*2	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{IL} min = –2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Only defined for DC and long cycle function test.
V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{SS} to V_{CC}, Ta = 0 to +70°C)

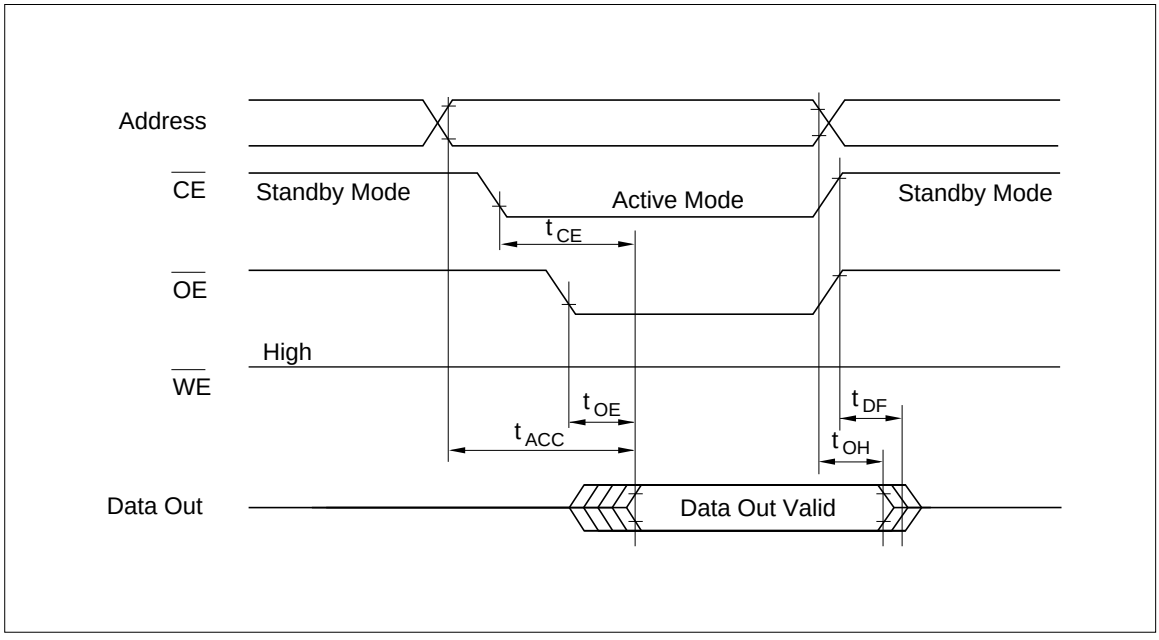
Test Conditions

- Input pulse levels: 0.45 V/2.4 V
- Input rise and fall times: 10 ns
- Output load: 1TTL Gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Parameter	Symbol	HN28F101-12 Min	HN28F101-12 Max	HN28F101-15 Min	HN28F101-15 Max	HN28F101-20 Min	HN28F101-20 Max	Unit	Test condition
Address to output delay	t_{ACC}	—	120	—	150	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	70	—	80	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float*1	t_{DF}	0	40	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	—	5	—	5	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform

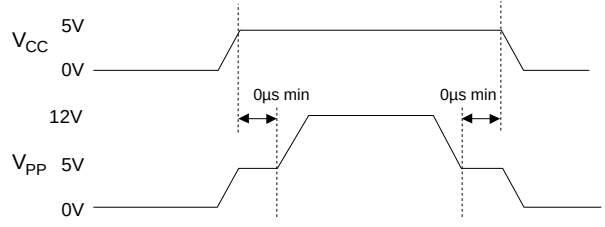


Command Programming/Data Programming/Erase Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.6 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current		I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Output leakage current		I_{LO}	—	—	2	µA	Vout = 0 V to V_{CC}
Standby V_{CC} current		I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
		I_{SB2}	—	—	200	µA	$\overline{CE}$ = V_{CC}
Operating V_{CC} current	Read	I_{CC1}	—	6	15	mA	Iout = 0 mA, f = 1 MHz
		I_{CC2}	—	10	30	mA	Iout = 0 mA, f = 8 MHz
	Program	I_{CC3}	—	2	10	mA	
	Erase	I_{CC4}	—	10	40	mA	In automatic erase
		I_{CC5}	—	5	15	mA	In high-reliability erase
V_{PP} current	Read	I_{PP1}	—	—	1	mA	V_{PP} = 12.6 V
	Program	I_{PP2}	—	5	30	mA	In programming
	Erase	I_{PP3}	—	35	80	mA	In automatic erase
		I_{PP4}	—	10	30	mA	In high-reliability erase
Input voltage		V_{IL}	– 0.3[*4]	—	0.8	V	
		V_{IH}	2.2	—	V_{CC} + 0.3[*5]	V	
Output voltage		V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing
V_{CC} must be applied before or simultaneously V_{PP}, and removed after or simultaneously V_{PP}.
This V_{CC}/V_{PP} power on/off timing must be satisfied at V_{CC}/V_{PP} on/off caused by power failure.



2. V_{PP} must not exceed 14 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12 V.
4. V_{IL} min = –1.0 V for pulse width ≤ 20 ns.
5. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.6 V, Ta = 0 to +70°C)

Test condition

- Input pulse levels: 0.45 V/2.4 V
- Input rise and fall times: 10 ns
- Output load: 1TTL Gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 2.0 V

		HN28F101-12		HN28F101-15		HN28F101-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test condition**
Command programming cycle time	t_{CWC}	120	—	150	—	200	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	60	—	60	—	60	—	ns	
Data setup time	t_{DS}	50	—	50	—	50	—	ns	
Data hold time	t_{DH}	10	—	10	—	10	—	ns	
$\overline{CE}$ setup time	t_{CES}	0	—	0	—	0	—	ns	
$\overline{CE}$ hold time	t_{CEH}	50	—	50	—	50	—	ns	
V_{PP} setup time	t_{VPS}	100	—	100	—	100	—	ns	
V_{PP} hold time	t_{VPH}	100	—	100	—	100	—	ns	
$\overline{WE}$ programming pulse width	t_{WEP}	70	—	70	—	80	—	ns	
$\overline{WE}$ programming pulse high time	t_{WEH}	40	—	40	—	40	—	ns	
$\overline{OE}$ setup time before command programming	t_{OEWS}	0	—	0	—	0	—	ns	
$\overline{OE}$ setup time before verify	t_{OERS}	6	—	6	—	6	—	µs	
Verify access time	t_{VA}	—	120	—	150	—	200	ns	
Verify access time in erase	t_{VAE}	—	300	—	300	—	300	ns	
$\overline{OE}$ setup time before status polling	t_{OEPS}	120	—	120	—	120	—	ns	
Status polling access time	t_{SPA}	—	120	—	150	—	200	ns	
Standby time before programming	t_{PPW}	25	—	25	—	25	—	µs	
Standby time in erase	t_{ET}	9	11	9	11	9	11	ms	
Output disable time*3	t_{DF}	0	40	0	50	0	60	ns	
Total erase time in automatic erase*3	t_{AET}	—	30	—	30	—	30	s	

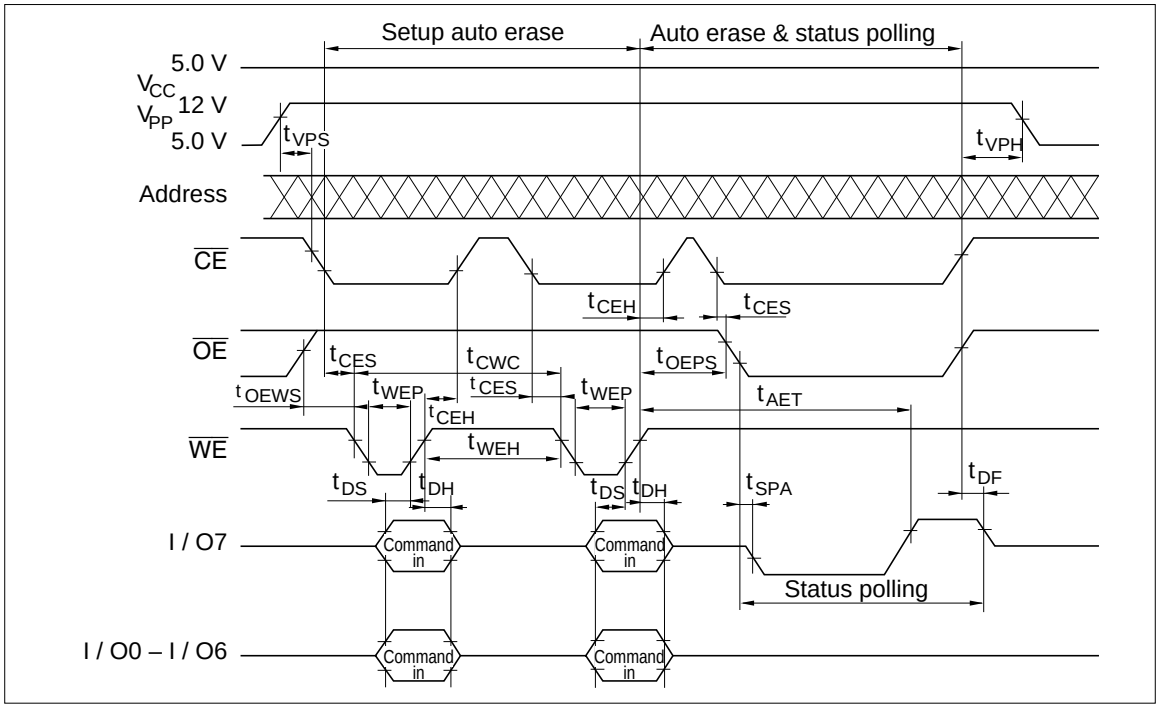
Notes: 1. $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Refer to read operation when $V_{PP} = V_{CC}$ about read operation while V_{PP} = 12 V .
3. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
4. Address are taken into on the falling edge of write-enable pulse and addresses are latched on the rising edge of write-enabke pulse during chip-enable is low. Data is latched on the rising edge of write-enable pulse during chip-enable is low.

Erase and Program Time

	Erase and program mode	Min	Typ*4	Max	Unit
Chip (128 kB) erase time	Auto erase mode	—	1	30	second
	Fast high-reliability erase mode*2, 3	—	0.6	30	second
Chip (128 kB) program time	Fast high-reliability program mode*3	—	5	81*5	second

Notes: 1. Each values are same for all read access version.
2. Excludes pre-write process before erasure and verify process (6 µs x 128 kB).
3. Excludes system overhead.
4. Ta = 25°C, V_{PP} = 12 V, V_{CC} = 5 V
5. Theoretical value calculated from fast high-reliability programming flowchart.
(25 µs program + 6 µs verify) x 20 times x 128 kB = 81 second.

Automatic Erase Timing Waveform



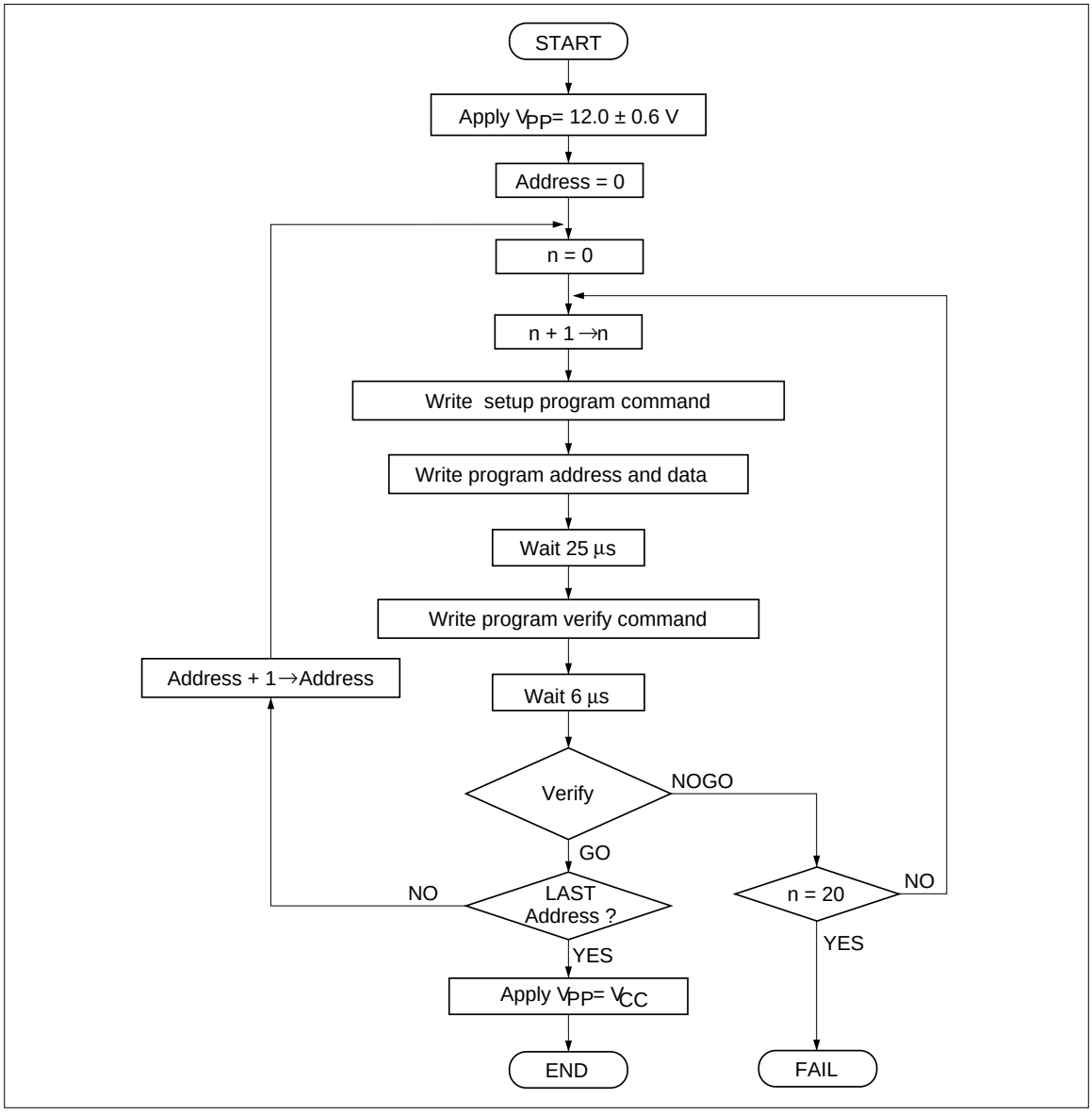
Status Polling

Status polling allows the status of the flash memory to be determined. If the flash memory is set to the status polling mode during erase cycle, I/O7 pin is lowered to V_{OL} level to indicate that the flash memory is performing erase operation. I/O7 pin is set to the V_{OH} level when erase operation has finished.

Notes: In automatic erase mode, the device automatically processes to pre-write all “0“ before erasing. Therefore, it is not required to pre-write by fast high-reliability programming.

Fast High-Reliability Programming

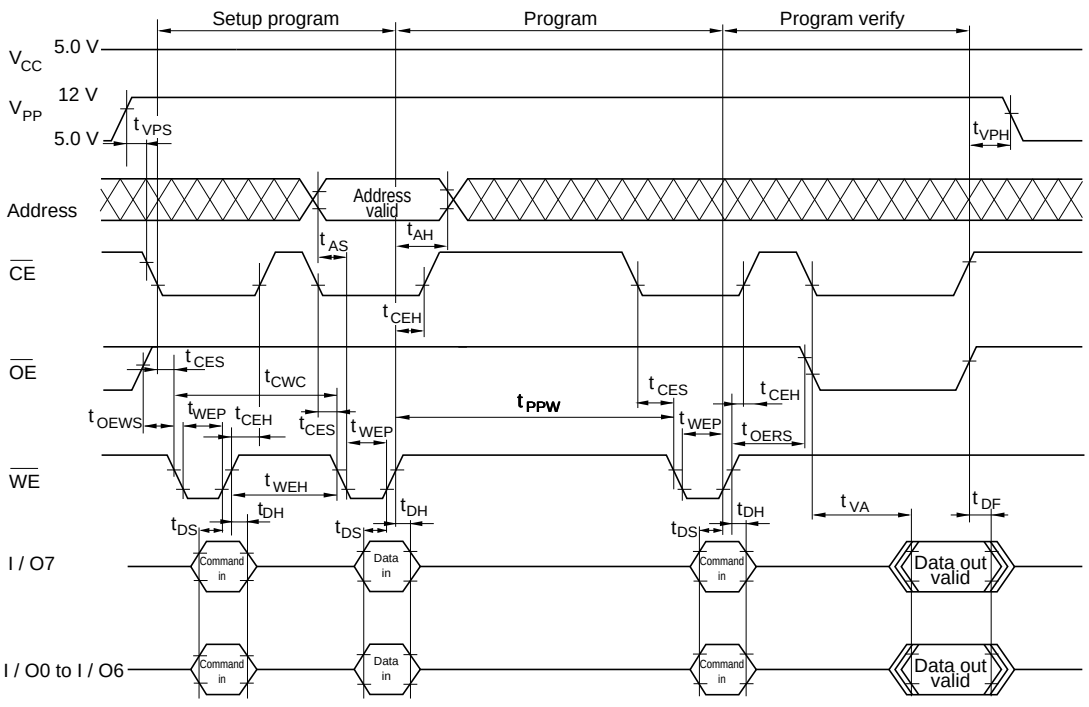
This device can be applied the fast high-reliability programming algorithm shown in following flowchart. This algorithm allows to obtain fasterprogramming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

Notes: In case of two or more devices are programmed simultaneously, following steps should be apllied to avoid over programming for the verified device .
(1) Write set up program command to FFH,
(2) Write program command to FFH,
(3) Write program verify command to 00H and program verify address to read address.

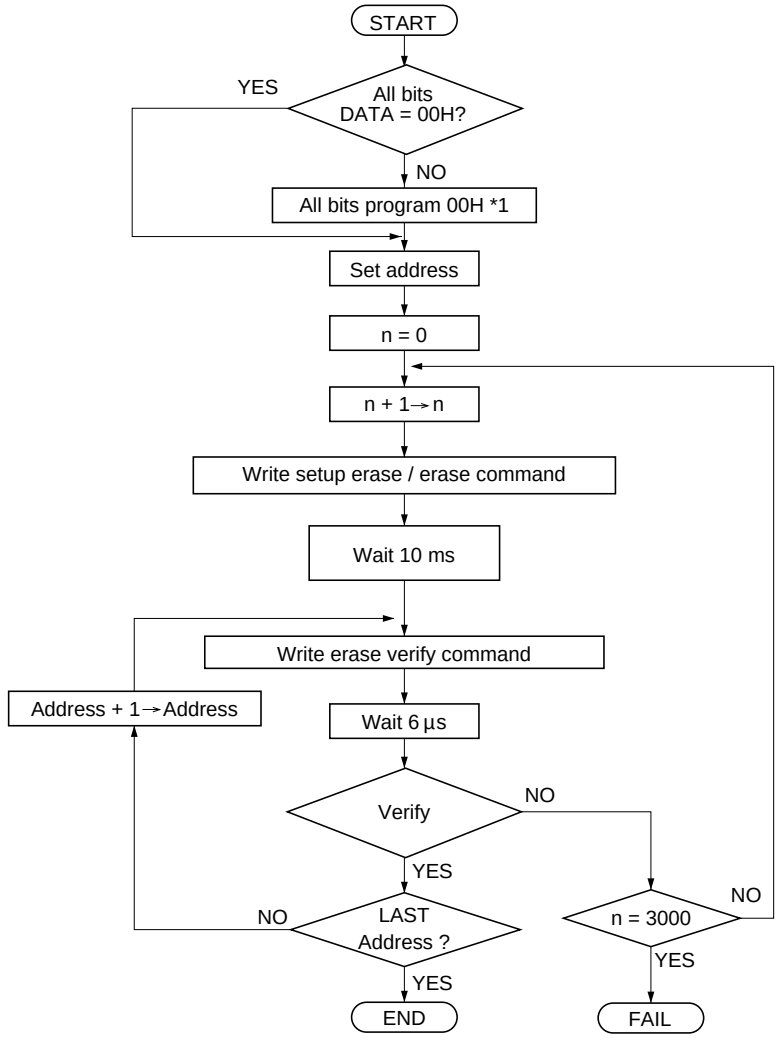
Fast High-Reliability Programming Timing Waveform



Notes: The data output level during program verification may result in an intermediate level between V_{OH} and V_{OL} due to an insufficiently programmed.

Fast High-Reliability Erase

This device can be applied the fast high-reliability erase algorithm showm in following flowchart
This algorithm allows to abtain faster erase time without any voltage any voltage stress to the device nor deterioration in reliability of data.

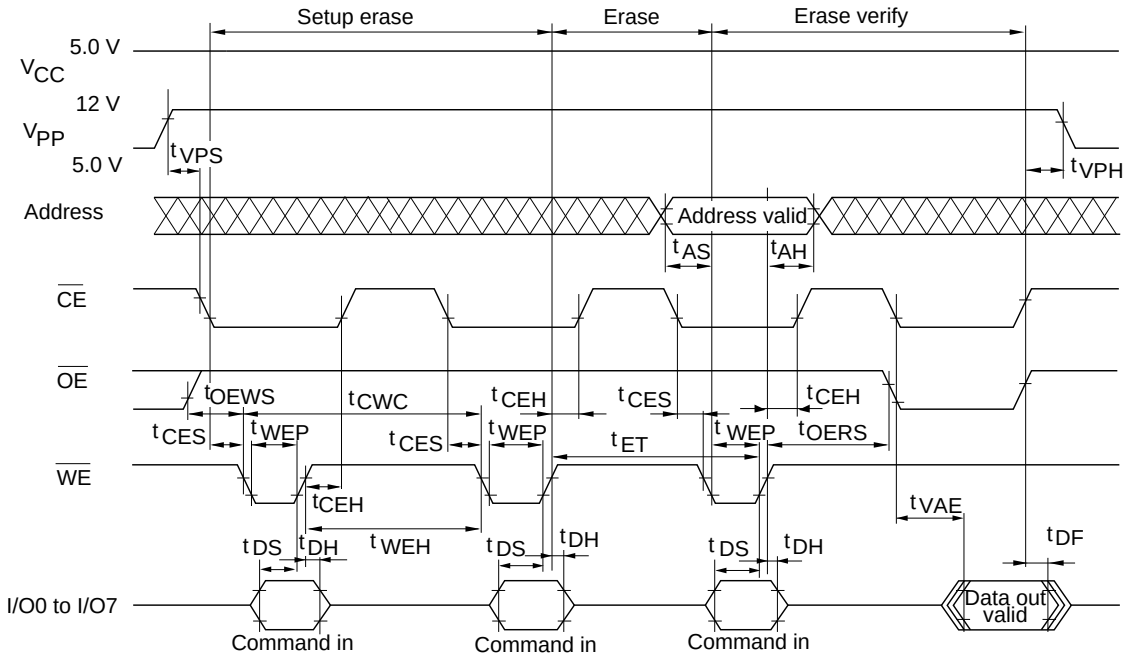


*1. Program data to all bits according to fast high-reliability erasing flowchart.

Fast High-Reliability Erasing Flowchart

Notes: In case of two or more devices are erased simultaneously, following steps should be applied to avoid over erase for verified device.
(1) Write set up erase command to A0H and set erase verify address to verify address.
(2) Write erase command to A0H.
(3) Write erase verify command to A0H.

Erase Timing Waveforms



Notes: The data output level during erasure verification may result in an intermediate level between V_{OH} and V_{OL} due to an insufficiently erased.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of flash memory. By this mode, the device will be automatically matched its own corresponding erase and programming algorithm, using programming equipment.

HN28F101 Series Identifier Code

Identifier	Pins DIP. SOP, PLCC TSOP	A0 (12) (20)	I/O7 (21) (29)	I/O6 (20) (28)	I/O5 (19) (27)	I/O4 (18) (26)	I/O3 (17) (25)	I/O2 (15) (23)	I/O1 (14) (22)	I/O0 (13) (21)	Hex Data
Manufacturer code		V_{IL}	0	0	0	0	0	1	1	1	07
Device code		V_{IH}	0	0	0	1	1	0	0	1	19

Notes : 1. Device identifier code can be read out by applying 12.0 V ±0.5 V to A9 when $V_{PP} = V_{CC}$, or inputting command while V_{PP} is 12 V.
2. A1 to A8, A10 to A16, and $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
3. $V_{CC} = V_{PP} = 5$ V ±10%