Features

- Logic voltage: 5V
- High-voltage output: V_{DD}-35V max.
- Multiple display
  (12-segment & 16-digit to 20-segment & 8-digit)
- 12×4 matrix key scanning
- 8 steps dimmer circuit
- 5 LED output ports (20mA max.)
- 4-bit general purpose input port
- No external resistors necessary for driver output (provides PMOS open-drain and pull-low resistor output)
- Serial interface with MCU (CLK, $\overline{CS}$, DI, DO)
- 52-pin QFP package

Applications

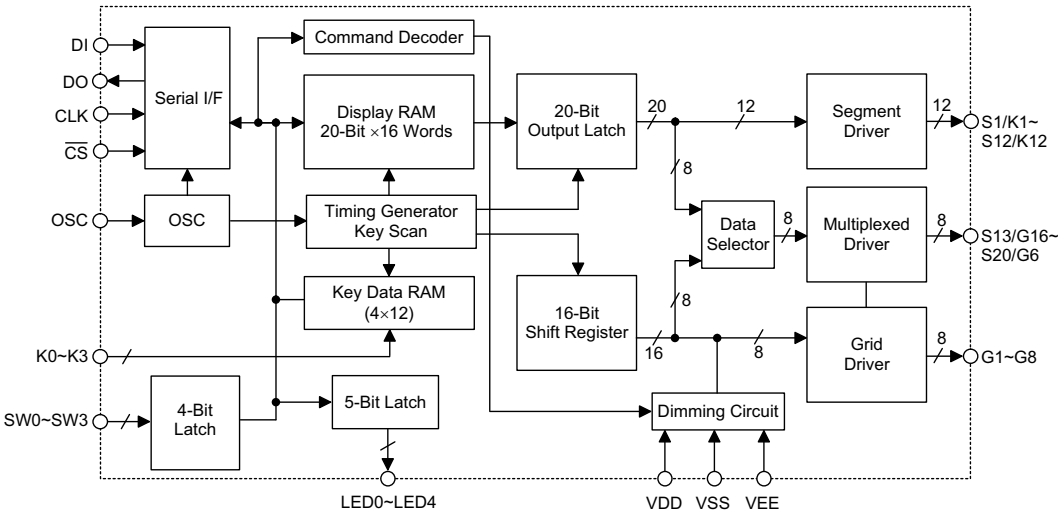
- Consumer products panel function control
- Industrial measuring instrument panel function control
- Other similar application panel function control

General Description

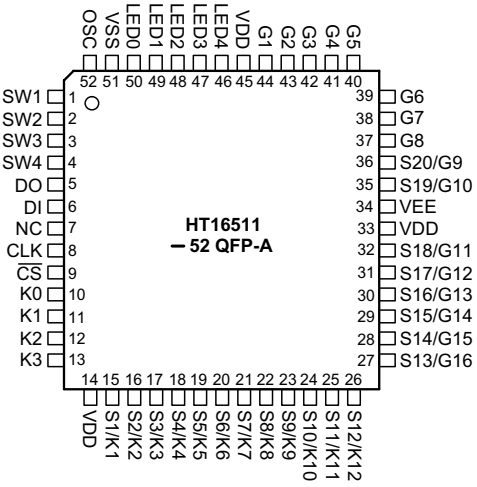
HT16511 is a VFD (Vacuum Fluorescent Display) controller/driver that is driven on a 1/8 to 1/16 duty factor. It consists of 12 segment output lines, 8 grid output lines, 8 segment/grid output drive lines, 5 LED output ports, a control circuit, a display memory, and a key scan circuit.

Serial data inputs to the HT16511 through a three-line serial interface. This VFD controller/driver is ideal as a peripheral device for an MCU.

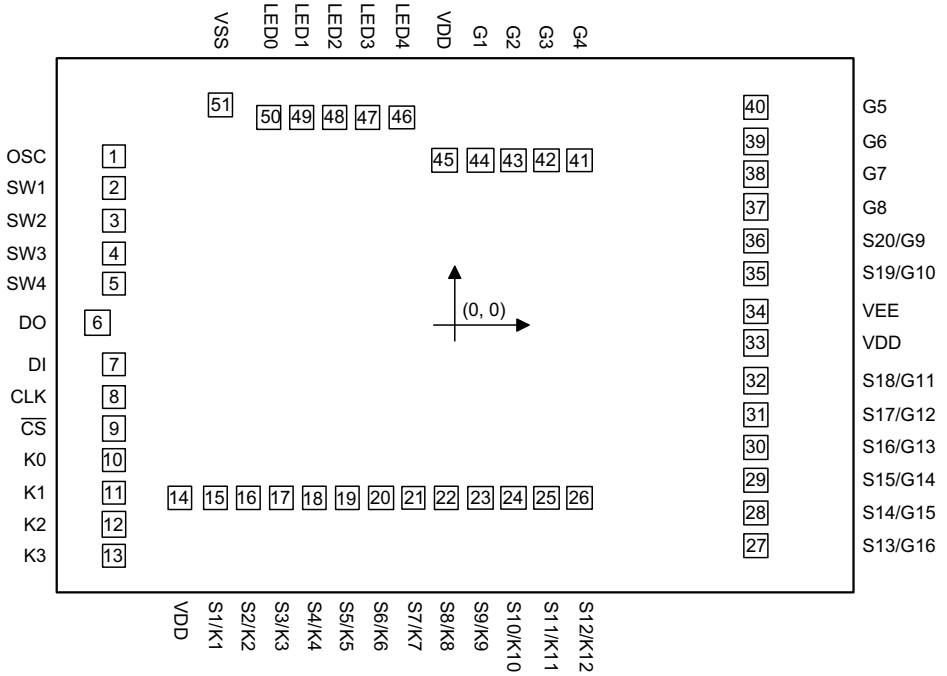
Block Diagram



Pin Assignment



Pad Assignment



Chip Size: 103.5 × 70.5 (mil)^2

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

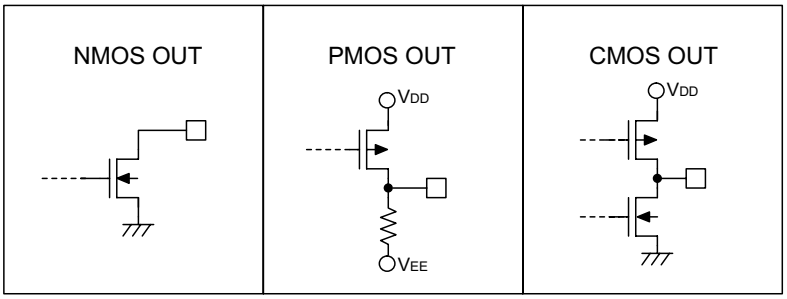
Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1110.000	555.300	27	977.250	-720.000
2	-1110.000	450.300	28	977.250	-612.000
3	-1110.000	345.300	29	977.250	-504.000
4	-1110.000	240.300	30	977.250	-396.000
5	-1110.000	135.300	31	977.250	-288.000
6	-1165.900	9.800	32	977.250	-180.000
7	-1110.000	-125.500	33	977.250	-55.150
8	-1110.000	-230.500	34	977.250	49.850
9	-1110.000	-335.500	35	977.250	173.350
10	-1110.000	-440.500	36	977.250	281.350
11	-1110.000	-545.500	37	977.250	389.350
12	-1110.000	-650.500	38	977.250	497.350
13	-1110.000	-755.500	39	977.250	605.350
14	-897.200	-560.300	40	977.250	713.350
15	-782.500	-560.300	41	405.500	545.400
16	-674.500	-560.300	42	297.500	545.400
17	-566.500	-560.300	43	189.500	545.400
18	-458.500	-560.300	44	81.500	545.400
19	-350.500	-560.300	45	-34.700	545.400
20	-242.500	-560.300	46	-173.950	684.850
21	-134.500	-560.300	47	-285.150	684.850
22	-26.500	-560.300	48	-390.150	684.850
23	81.500	-560.300	49	-501.350	684.850
24	189.500	-560.300	50	-606.350	684.850
25	297.500	-560.300	51	-765.200	726.350
26	405.500	-560.300			

Pin Description

Pin No.	Pin Name	I/O	Description
1~4	SW1~SW4	I	4-bit general purpose input port
5	DO	O	Output serial data at the falling edge of the shift clock, starting from low order bit. This is an NMOS open-drain output pin.
6	DI	I	Input serial data at the rising edge of the shift clock, starting from the low order bit.
7	NC	—	No connection
8	CLK	I	Reads serial data at the rising edge, and outputs data at the falling edge.
9	$\overline{CS}$	I	Initializes serial interface at the rising or falling edge of the HT16511. Then it waits to receive a command. Data input after $\overline{CS}$ has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While $\overline{CS}$ is high, CLK is ignored.
10~13	K0~K3	I	Keying data input to these pins is latched at the end of the display cycle.
14, 33, 45	VDD	—	Posistive power supply
15~26	S1/K1~S12/K12	O	Segment or key source output pins (dual function). This is PMOS open-drain and pull-low resistor output.
27~32, 35~36	S13/G16~S20/G9	O	Segment or Grid driver output pins. These pins are selectable for segment or grid driving. This is PMOS open-drain and pull-low resistor output.
34	VEE	—	VFD power supply
37~44	G8~G1	O	Grid driver output pins (Grid only). This is PMOS open-drain and pull-low resistor output.
46~50	LED4~LED0	O	LED driver output ports. This is a CMOS output pin.
51	VSS	—	Negative power supply, ground
52	OSC	I	Connected to an external resistor or an RC oscillator circuit.

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Operating Temperature ..... –25°C to 75°C

Storage Temperature ..... –50°C to 125°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	—	—	4.5	5	5.5	V
V_{EE}	VFD Supply Voltage	—	—	0	—	V_{DD}–35	V
f_{OSC}	Oscillation Frequency	5V	R_{OSC}=51kΩ	350	500	650	kHz
R_{PL}	Output Pull-low Resistor	5V	Driver output	50	100	150	kΩ
I_{DD}	Operating Current	5V	No load, VFD display off	—	—	5	mA
I_{OL}	Driver Leakage Current	5V	V_O=V_{DD}–30V, VFD driver off	—	—	–10	μA
I_{OL1}	LED Sink Current	5V	V_{OL}=1V, LED0~LED4	20	—	—	mA
I_{OH1}	LED Source Current	5V	V_{OH}=0.9V_{DD}, LED0~LED4	–1	—	—	mA
I_{OH21}	Segment/Key Source Current	5V	V_{OH}=V_{DD}–2V, S1/K1~S12/K12	–3	—	—	mA
I_{OH22}	Segment/Grid Source Current	5V	V_{OH}=V_{DD}–2V	–15	—	—	mA
I_{OL3}	DO Sink Current	5V	V_{OL}=0.4V	4	—	—	mA
V_{IH}	"H" Input Voltage	—	—	0.7V_{DD}	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	0.3V_{DD}	V
V_{OH1}	High-level Output Voltage	5V	LED0~LED4, I_{OH1}=–1mA	0.9V_{DD}	—	V_{DD}	V
V_{OL1}	Low-level Output Voltage	5V	LED0~LED4, I_{OL1}=20mA	0	—	1	V
V_{OL2}	Low-level Output Voltage	5V	DO, I_{OL2}=4mA	0	—	0.4	V

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{PHL}	Propagation Delay Time	5V	CLK→DO C_L=15pF, R_L=10kΩ	—	—	300	ns
t_{PLH}		5V		—	—	100	ns
t_{r1}	Rise Time	5V	C_L=300pF, S0~S12	—	—	2	μs
t_{r2}		5V	C_L=300pF, G1~G16	—	—	0.5	μs
t_f	Fall Time	5V	C_L=300pF, Sn, Gn	—	—	120	μs
t_{max}	Maximum Clock Frequency	5V	Duty=50%	1	—	—	MHz
C_i	Input Capacitance	5V	—	—	—	15	pF
t_{CW}	Clock Pulse Width	5V	—	400	—	—	ns
t_{SW}	Strobe Pulse Width	5V	—	1	—	—	us
t_{SU}	Data Setup Time	5V	—	100	—	—	ns
t_h	Data Hold Time	5V	—	100	—	—	ns
t_{CS}	Clock-Strobe Time	5V	CLK rising edge to CS rising edge	1	—	—	μs
t_W	Wait Time	5V	CLK rising edge to CLK falling edge	1	—	—	μs

Functional Description

Display RAM and Display Mode

The static display RAM is organized into 40×8 bits and stores the data transmitted from an external device to the HT16511 through a serial interface. The contents of the RAM are directly mapped to the contents of the VFD driver. Data in the RAM can be accessed through the data setting, address setting and display control commands. It is assigned addresses in 8-bit unit as follows:

SEG1	SEG4	SEG8	SEG12	SEG16	SEG20	
00HL	00HU	01HL	01HU	02HL		DIG1
03HL	03HU	04HL	04HU	05HL		DIG2
06HL	06HU	07HL	07HU	08HL		DIG3
09HL	09HU	0AHL	0AHU	0BHL		DIG4
0CHL	0CHU	0DHL	0DHU	0EHL		DIG5
0FHL	0FHU	10HL	10HU	11HL		DIG6
12HL	12HU	13HL	13HU	14HL		DIG7
15HL	15HU	16HL	16HU	17HL		DIG8
18HL	18HU	19HL	19HU	1AHL		DIG9
1BHL	1BHU	1CHL	1CHU	1DHL		DIG10
1EHL	1EHU	1FHL	1FHU	20HL		DIG11
21HL	21HU	22HL	22HU	23HL		DIG12
24HL	24HU	25HL	25HU	26HL		DIG13
27HL	27HU	28HL	28HU	29HL		DIG14
2AHL	2AHU	2BHL	2BHU	2CHL		DIG15
2DHL	2DHU	2EHL	2EHU	2FHL		DIG16

b0 b3	b4 b7
XXHL	XXHU
Lower 4 bits	Higher 4 bits

Note: Only the lower 4 bits of the addresses assigned to SEG17 through SEG20 are valid, the higher 4 bits are ignored.

Dimming Control

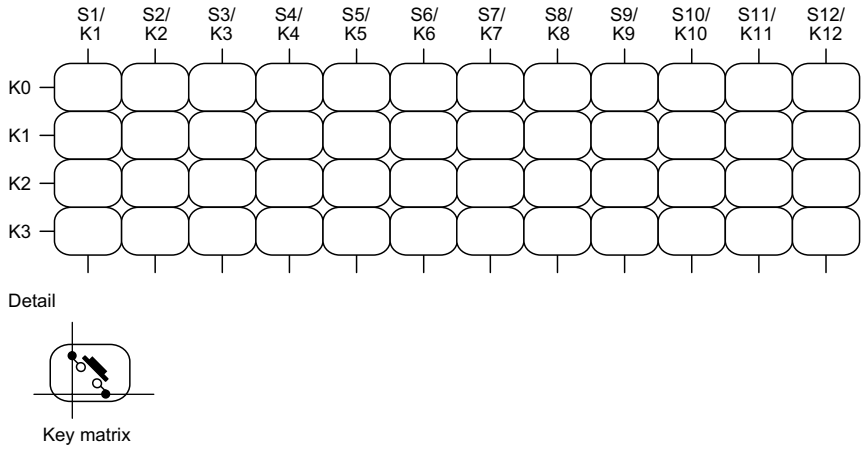
HT16511 provides 8-step dimmer function on display by controlling the 3-bit binary command code. The full pulse width of grid signal is divides into 16 uniform sections by PWM (pulse width modulation) technology.

The 16 uniform sections available form 8 steps dimmer via 3-bit binary code. The 8-step dimmer includes 1/16, 2/16, 4/16, 10/16, 11/16, 12/16, 13/16 and 14/16. The 1/16 pulse width indicates minimum lightness. The 14/16 pulse width represents maximum lightness (Refer to the display control command).

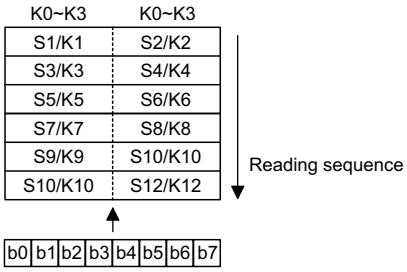
Key Matrix and Key-Input Data Storage RAM

The key matrix scans the series key states at each level of the key strobe signal (S1/K1~S12/K12) output of the HT16511. The key strobe signal outputs are time-multiplexed signals from S1/K1~S12/K12. The states of inputs K0~K3 are sampled by strobe signal S1/K1~S12/K12 and latched into the register.

The key matrix is made up of a 12×4 matrix, as shown below.



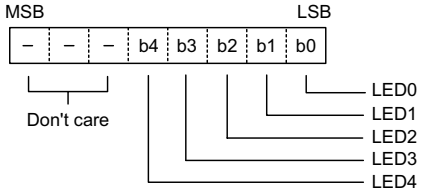
The data of each key is stored as illustrated below, and is read with the read command, starting from the least significant bit.



LED Port

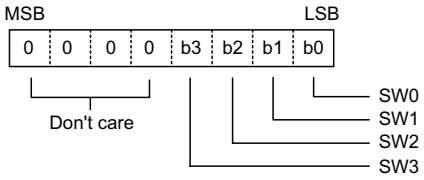
The LED port belongs to the CMOS output configuration.

Data is written to the LED port with the write command, starting from the least port′s least significant bit. In our application (see application circuits), the user adopts an internal NMOS device to a driver LED component by connecting VDD. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED turns off. The data of bits 6 through 8 are ignored.



SW Data

The HT16511 provides an extra 4-bit general input port. The SW data is provided with available binary code. The SW data is read with the read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.

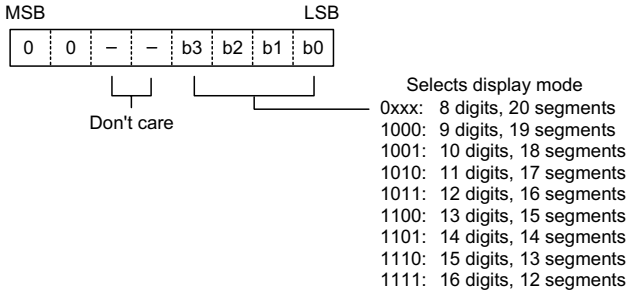


Commands

Commands set the display mode and status of the VFD driver.

The first 1 byte input to the HT16511 through the DI pin after the $\overline{CS}$ pin has fallen, is regarded as a command. If $\overline{CS}$ is set high while commands/data are transmitted, serial communication is initialized, and the commands/data being transmitted are not valid (however, the commands/data previously transmitted remains valid).

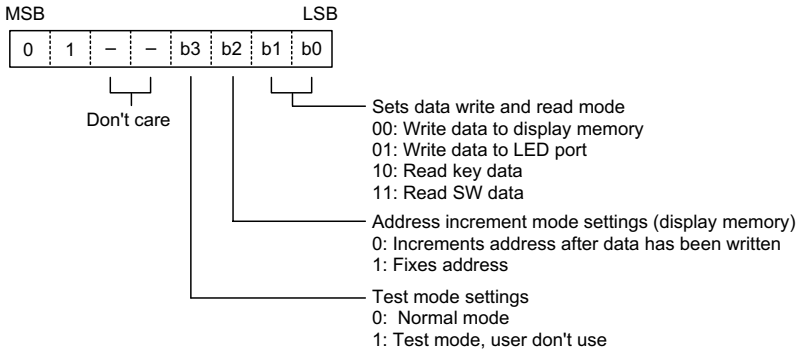
- Display mode setting commands
  These commands initialize the HT16511 and select the number of segments and the number of grids (1/8~1/16 duty, 12 segments to 20 segments).
  When these commands are executed, the display is forcibly turned off, and key scanning is also stopped. To resume display, the display command ″ON″ must be executed. If the same mode is selected, nothing happens.



Note: Power-on status: 16-digit, 12 segment mode is selected.

- Data setting commands

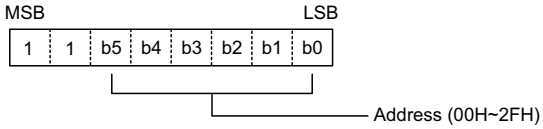
These commands set the data write and data read modes.



Note: power-on status: normal mode operation and address increment mode are set.

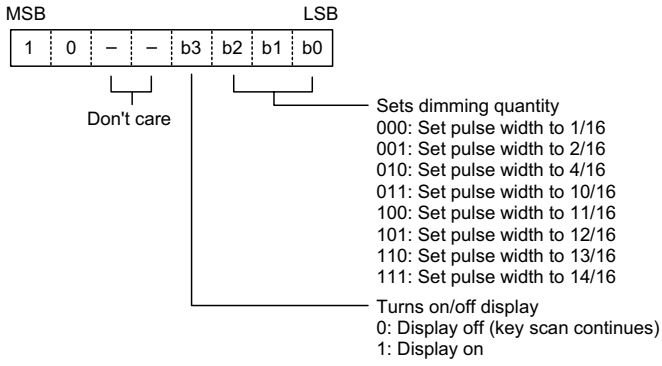
- Address setting commands

These commands set the address of the display memory.



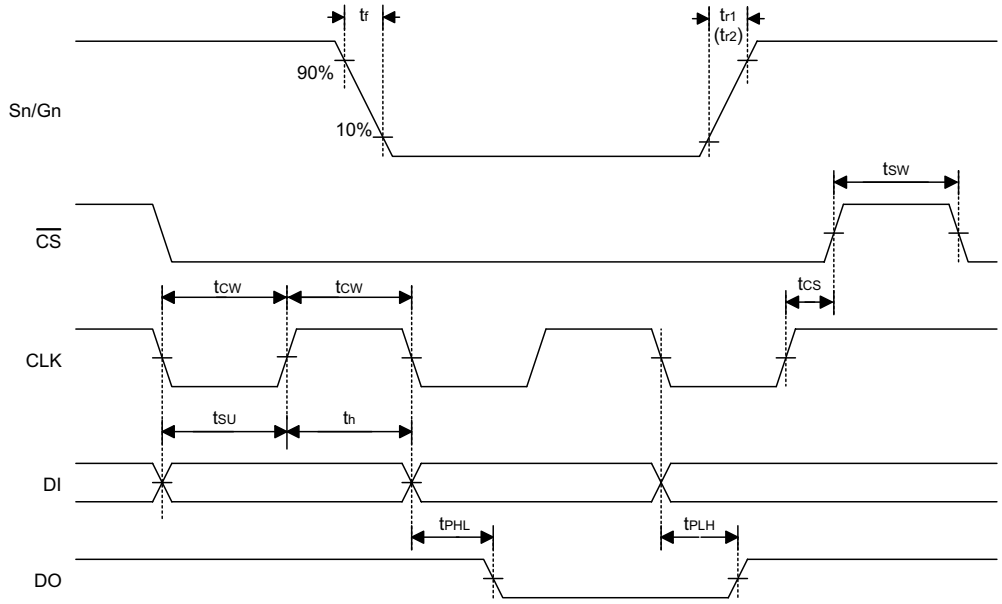
If address 30H or higher is set, data is ignored until a valid address is set.
Note: power-on status: the address is set to 00H.

- Display control commands

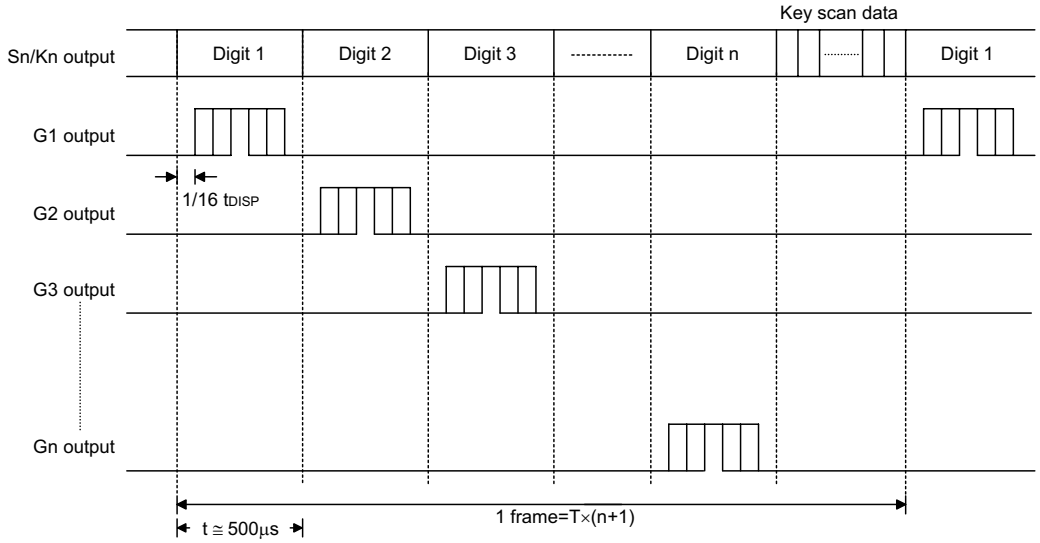


Note: power-on status: 1-16 pulse width is set and the display is turned off. Key scanning will be stopped during power

Timing Diagrams



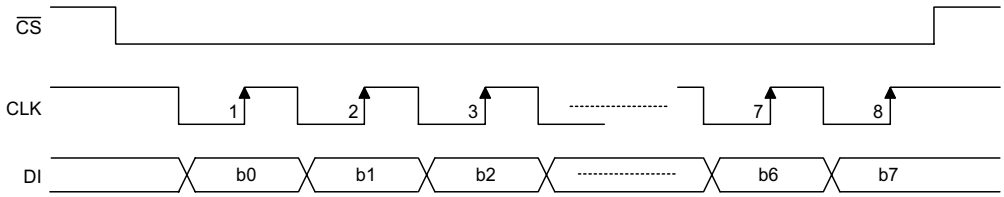
Key Scanning and Display Timing



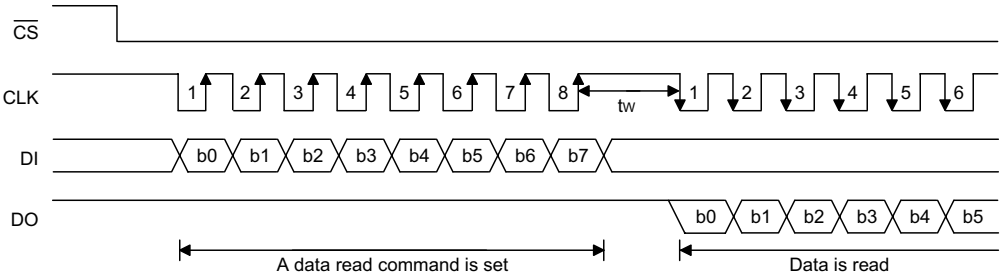
Note: One cycle of key scan consists of two frames, and data of 12×4 matrixes is stored in RAM.

Serial Communication Format

- Reception (command/data write)

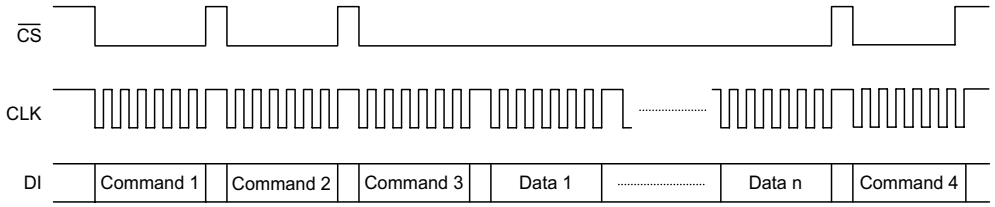


- Transmission (data read)



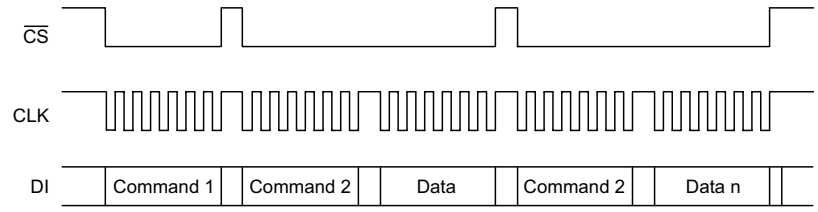
DO must be sure to connect an external pull-high resistor to this pin (1kΩ to 10kΩ).
Note: When data is read, a wait time "t_W" of 1μs is necessary.

- Updating display memory by incrementing address



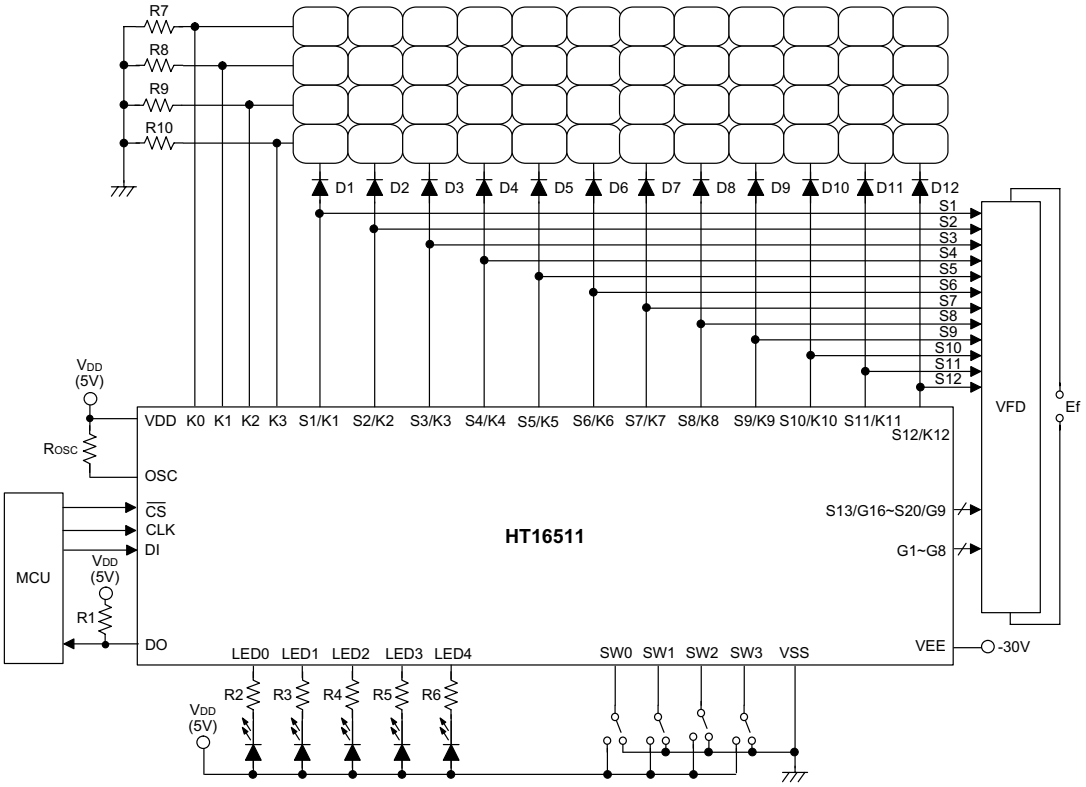
Note: Command 1: sets display mode
Command 2: sets data
Command 3: sets address
Data 1 to n: transfers display data (48 bytes max.)
Command 4: controls display

- Updating specific addresses



Note: Command 1: sets data
Command 2: sets address
Data: display data

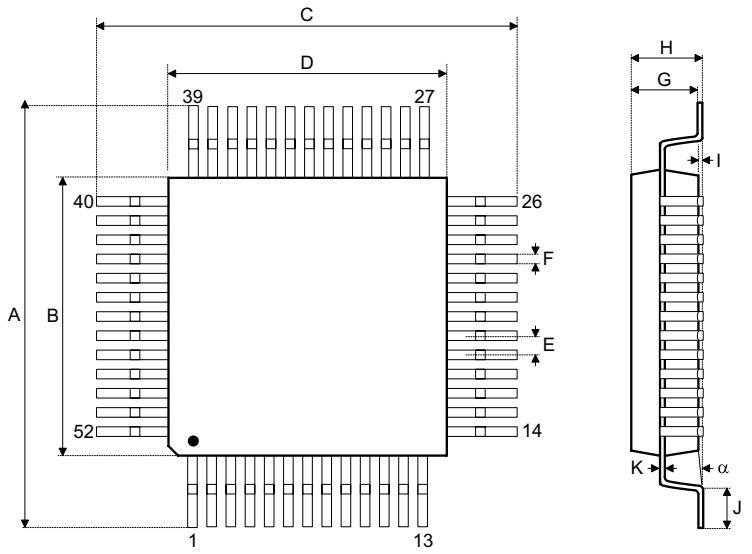
Application Circuits



Note: R_{OSC}=51kΩ for oscillator resistor
R1=1~10kΩ for external pull-high resistor
R2~R6=750Ω~1.2kΩ
R7~R10=10kΩ for external pull-low resistor
D1~D12=1N4001
Ef=Filament voltage for VFD

Package Information

52-pin QFP (14×14) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	18.80	—	19.20
B	13.90	—	14.10
C	18.80	—	19.20
D	13.90	—	14.10
E	—	0.65	—
F	—	0.40	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	0.73	—	1.03
K	0.10	—	0.20
α	0°	—	7°

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