Am29PL320D

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **20475** Revision **C** Amendment **2** Issue Date **October 2, 2003**

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Am29PL320D

32 Megabit (2 M x 16-Bit/1 M x 32-Bit) CMOS 3.0 Volt-only High Performance Page Mode Flash Memory

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **32 Mbit Page Mode device**
  - Word (16-bit) or double word (32-bit) mode selectable via WORD# input
  - Page size of 8 words/4 double words: Fast page read access from random locations within the page
- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Flexible sector architecture**
  - Sector sizes (x16 configuration): One 16 Kword, two 8 Kword, one 96 Kword and fifteen 128 Kword sectors
  - Supports full chip erase
- **SecSi™ (Secured Silicon) Sector region**
  - Current version of device has 512 words (256 double words); future versions will have 128 words (64 double words)
- **Top or bottom boot block configuration**
- **Manufactured on 0.23 µm process technology**
- **20-year data retention at 125°C**
- **Minimum 1 million erase cycles guarantee per sector**

PERFORMANCE CHARACTERISTICS

- **High performance read access times**
  - Page access times as fast as 20 ns
  - Random access times as fast as 60 ns
- **Power consumption (typical values)**
  - Initial page read current: 4 mA (1 MHz), 40 mA (10 MHz)
  - Intra-page read current: 15 mA (10 MHz), 50 mA (33 MHz)
  - Program/erase current: 25 mA
  - Standby mode current: 2 µA

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation

HARDWARE FEATURES

- **Sector Protection**
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked via programming equipment
  - Temporary Sector Unprotect command sequence allows code changes in previously locked sectors
- **ACC (Acceleration) input provides faster programming times**
- **WP# (Write Protect) input**
  - At V_{IL}, protects the first or last 32 Kword sector, regardless of sector protect/unprotect status
  - At V_{IH}, allows removal of sector protection
  - An internal pull up to V_{CC} is provided
- **Package Options**
  - 84-ball FBGA

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GENERAL DESCRIPTION

The Am29PL320D is a 32 Mbit, 3.0 Volt-only page mode Flash memory device organized as 2,097,152 words or 1,048,576 double words. The device is offered in an 84-ball FBGA package. The word-wide data (x16) appears on DQ15–DQ0; the double word-wide (x32) data appears on DQ31–DQ0. The device is available in both top and bottom boot versions. This device can be programmed in-system or with in standard EPROM programmers. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations.

The device offers fast page access times of 20, 25, and 35 ns, with corresponding random access times of 60, 70, 90 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#), and output enable (OE#) controls.

Page Mode Features

The device is AC timing, input, output, and package **compatible with 16 Mbit x 16 page mode Mask ROM**. The page size is 8 words or 4 double words.

After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

The **SecSi™ Sector** (Secured Silicon) is an extra sector capable of being permanently locked by AMD or customers. The **SecSi Indicator Bit** (DQ7) is permanently set to a 1 if the part is **factory locked**, and set to a 0 if **customer lockable**. This way, customer lockable parts can never be used to replace a factory locked part. **Current version of device has 512 words (256 double words); future versions will have only 128 words (64 double words). This should be considered during system design.** Factory locked parts can store a secure, random 16 byte ESN (Electronic Serial Number), customer code (programmed through AMD's ExpressFlash service), or both. Customer Lockable parts may be programmed after being shipped from AMD.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

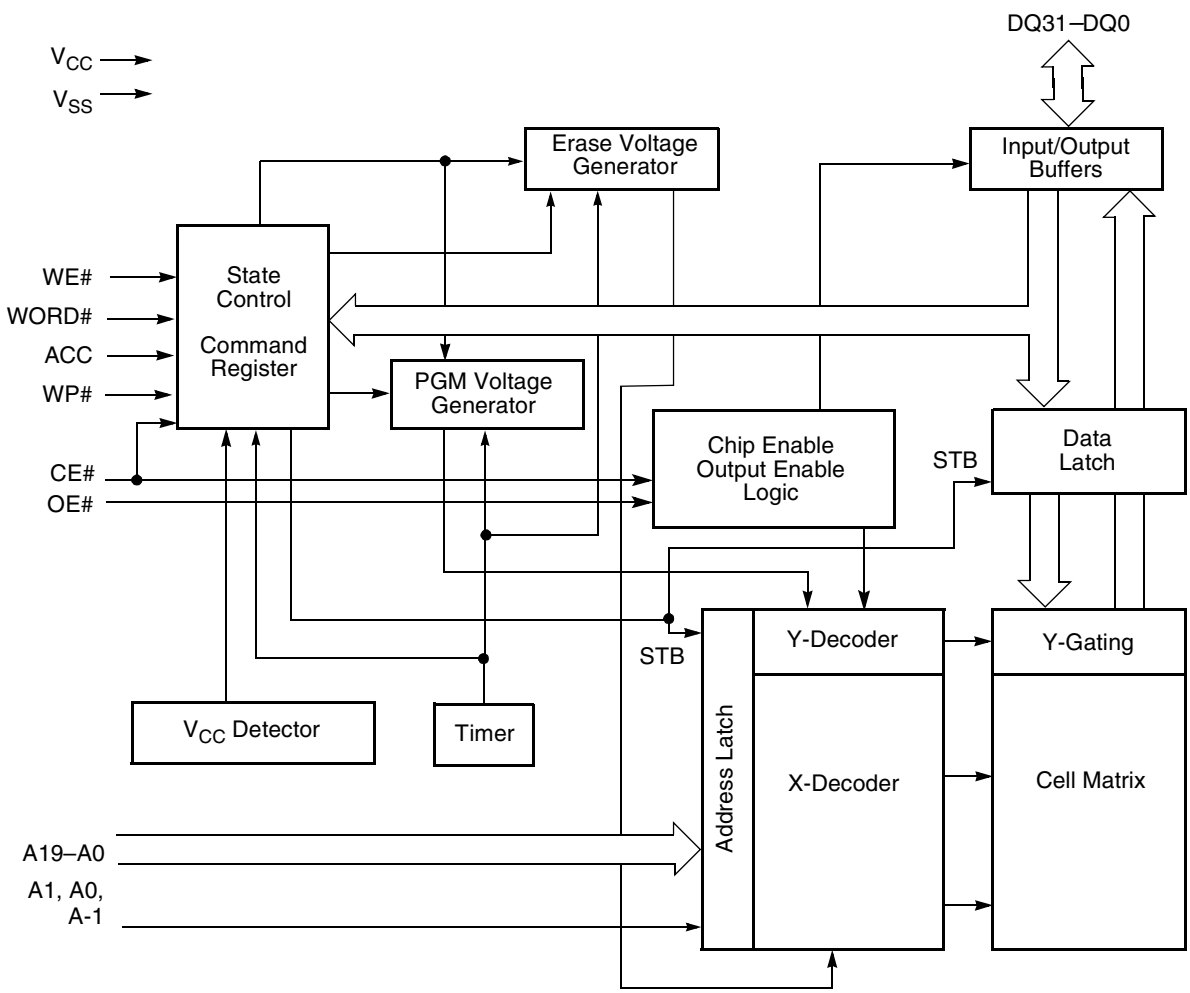
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Family Part Number		Am29PL320D		
Speed Option	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**60R**	**70R**	
	Full Voltage Range: V_{CC} = 2.7–3.6 V		**70**	**90**
Max access time, ns (t_{ACC})		60	70	90
Max CE# access time, ns (t_{CE})		60	70	90
Max page access time, ns (t_{PACC})		20	25	30
Max OE# access time, ns (t_{OE})		20	25	30

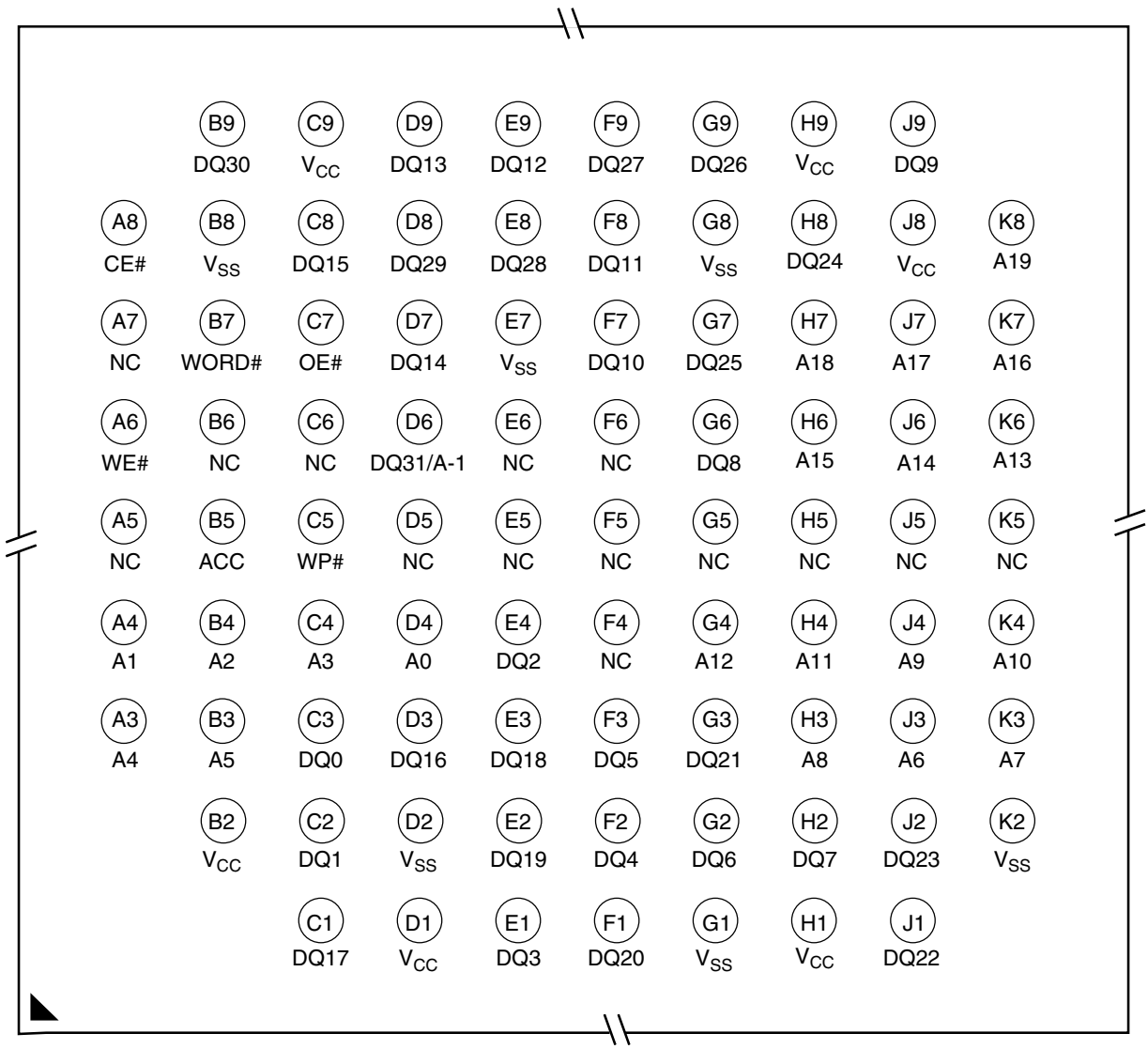
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS

84-Ball FBGA
Top View, Balls Facing Down



Special Handling Instructions for FBGA Package

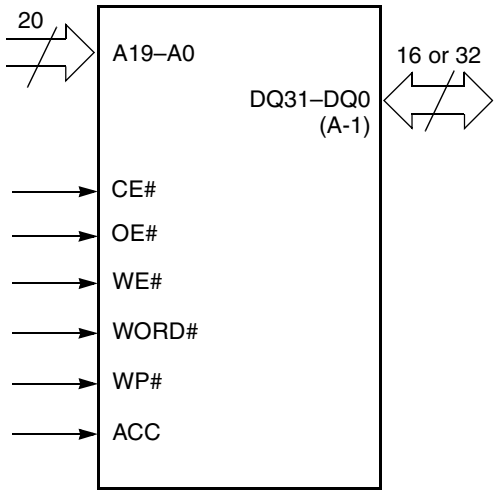
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

INPUT CONFIGURATION

A19–A0	=	20 address inputs
DQ30–DQ0	=	31 data inputs/outputs
DQ31/A-1	=	In double word mode, functions as DQ31. In word mode, functions as A-1 (LSB address input)
WORD#	=	Word enable input When low, enables word mode When high, enables double word mode
WP#	=	Hardware Write Protect input
ACC	=	Acceleration input
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	input not connected internally

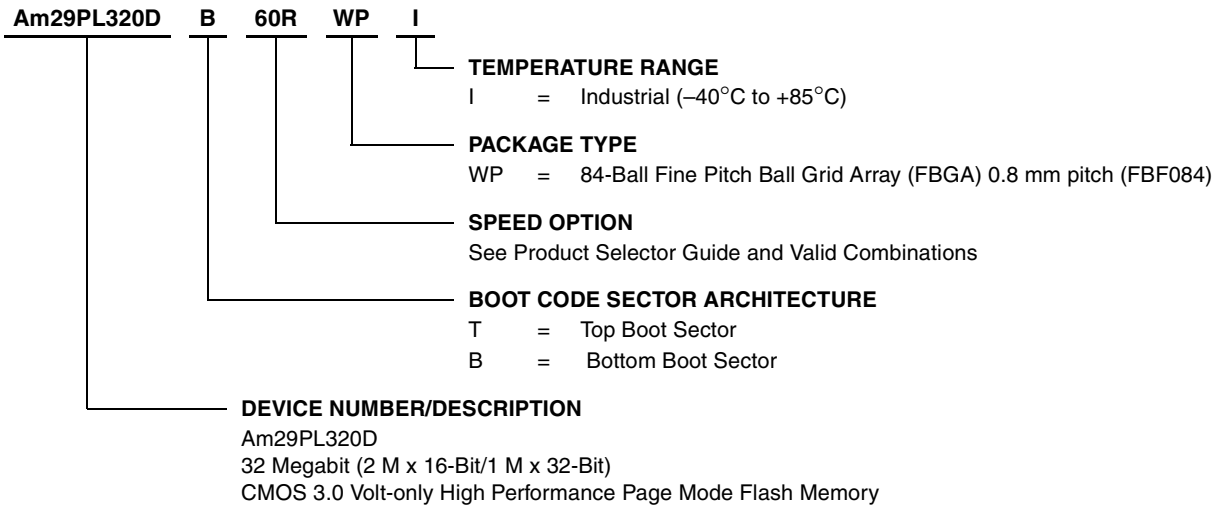
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		Package Marking	Voltage Range
AM29PL320DT60R, AM29PL320DB60R	WPI	P320DT60RI, P320DB60RI	V_{CC} = 3.0–3.6 V
AM29PL320DT70R, AM29PL320DB70R		P320DT70RI, P320DB70RI	
AM29PL320DT70, AM29PL320DB70		P320DT70VI, P320DB70VI	V_{CC} = 2.7–3.6 V
AM29PL320DT90, AM29PL320DB90		P320DT90VI, P320DB90VI	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29PL320D Device Bus Operations

Operation	CE#	OE#	WE#	WP#	Addresses (Note 1)	DQ7–DQ0	DQ31–DQ8	
							WORD# = V_{IH}	WORD# = V_{IL}
Read	L	L	H	X	A_{IN}	D_{OUT}	D_{OUT}	DQ30–DQ16 = High-Z, DQ31 = A-1
Write	L	H	L	X	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC} \pm 0.3$ V	X	X	X	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	X	X	High-Z	High-Z	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. *Addresses are A19–A0 in double word mode (WORD# = V_{IH}), A19–A-1 in word mode (WORD# = V_{IL}).*
2. *The sector protect and sector unprotect functions must be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Word/Double Word Configuration

The WORD# input controls whether the device data I/Os DQ31–DQ0 operate in the word or double word configuration. If the WORD# input is set at V_{IH}, the device is in double word configuration; DQ31–DQ0 are active and controlled by CE# and OE#.

If the WORD# input is set at logic '0', the device is in word configuration, and only data I/Os DQ15–DQ0 are active and controlled by CE# and OE#. The data I/Os DQ30–DQ16 are tri-stated, and the DQ31 input is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# inputs to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output inputs. WE# should remain at V_{IH}. The WORD# input determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Read Mode

Random Read (Non-Page Mode Read)

The device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection. OE# is the output control and should be used to gate data to the output inputs if the device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The Am29PL320D is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the Am29PL320D device is 8 words, or 4 double words, with the appropriate page being selected by the higher address bits A19–A2 and the LSB bits A1–A0 (in the double word mode) and A1 to A-1 (in the word mode) determining the specific word/double word within that page. This is an asynchronous operation with the microprocessor supplying the specific word or double word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping A19–A2 constant and changing A1 to A0 to select the specific double word, or changing A1 to A-1 to select the specific word, within that page.

The following tables determine the specific word and double word within the selected page:

Table 2. Double Word Mode

Word	A1	A0
Double Word 0	0	0
Double Word 1	0	1
Double Word 2	1	0
Double Word 3	1	1

Table 3. Word Mode

Word	A1	A0	A-1
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the WORD# input determines whether the device accepts program data in double words or words. Refer to "Word/Double Word Configuration" for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or double word, instead of four. The "Word/Double Word Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput during system production.

If the system asserts V_{HH} (11.5 to 12.5 V) on this input, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to "AC Characteristics" for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# input is both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# is held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during Automatic Sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output inputs are placed in the high impedance state.

Table 4. Sector Address Table, Top Boot (Am29PL320DT)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kwords/ Kdouble words)	Address Range (in hexadecimal)	
										Word Mode (x16)	Double Word Mode (x32)
SA0	0	0	0	0	X	X	X	X	128/64	000000–01FFFF	00000–0FFFF
SA1	0	0	0	1	X	X	X	X	128/64	020000–03FFFF	10000–1FFFF
SA2	0	0	1	0	X	X	X	X	128/64	040000–05FFFF	20000–2FFFF
SA3	0	0	1	1	X	X	X	X	128/64	060000–07FFFF	30000–3FFFF
SA4	0	1	0	0	X	X	X	X	128/64	080000–09FFFF	40000–4FFFF
SA5	0	1	0	1	X	X	X	X	128/64	0A0000–0BFFFF	50000–5FFFF
SA6	0	1	1	0	X	X	X	X	128/64	0C0000–0DFFFF	60000–6FFFF
SA7	0	1	1	1	X	X	X	X	128/64	0E0000–0FFFFF	70000–7FFFF
SA8	1	0	0	0	X	X	X	X	128/64	100000–11FFFF	80000–8FFFF
SA9	1	0	0	1	X	X	X	X	128/64	120000–13FFFF	90000–9FFFF
SA10	1	0	1	0	X	X	X	X	128/64	140000–15FFFF	A0000–AFFFF
SA11	1	0	1	1	X	X	X	X	128/64	160000–17FFFF	B0000–BFFFF
SA12	1	1	0	0	X	X	X	X	128/64	180000–19FFFF	C0000–CFFFF
SA13	1	1	0	1	X	X	X	X	128/64	1A0000–1BFFFF	D0000–DFFFF
SA14	1	1	1	0	X	X	X	X	128/64	1C0000–1DFFFF	E0000–EFFFF
SA15	1	1	1	1	0000–1011				96/48	1E0000–1F7FFF	F0000–FBFFF
SA16	1	1	1	1	1	1	0	0	8/4	1F8000–1F9FFF	FC000–FCFFF
SA17	1	1	1	1	1	1	0	1	8/4	1FA000–1FBFFF	FD000–FDFFF
SA18	1	1	1	1	1	1	1	X	16/8	1FC000–1FFFFF	FE000–FFFFF

Note: *Address range is A19–A-1 if device is in word mode (WORD# = V_{IL}). Address range is A19–A0 if device is in double word mode (WORD# = V_{IH}).*

Table 5. SecSi™ Sector Addresses for Top Boot Devices

Device	Sector Address A7–A0	Sector Size	(x16) Address Range	(x32) Address Range
Am29PL320DT	00000000	512 words/256 double words	000000h–0001FFh	00000h–000FFh

Table 6. Sector Address Table, Bottom Boot (Am29PL320DB)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kwords/ Kdouble words)	Address Range (in hexadecimal)	
										Word Mode (x16)	Double Word Mode (x32)
SA0	0	0	0	0	0	0	0	X	16/8	000000–003FFF	00000–001FF
SA1	0	0	0	0	0	0	1	0	8/4	004000–005FFF	02000–02FFF
SA2	0	0	0	0	0	0	1	1	8/4	006000–007FFF	03000–03FFF
SA3	0	0	0	0	01000–11111				96/48	008000–01FFFF	04000–0FFFF
SA4	0	0	0	1	X	X	X	X	128/64	020000–03FFFF	10000–1FFFF
SA5	0	0	1	0	X	X	X	X	128/64	040000–05FFFF	20000–2FFFF
SA6	0	0	1	1	X	X	X	X	128/64	060000–07FFFF	30000–3FFFF
SA7	0	1	0	0	X	X	X	X	128/64	080000–09FFFF	40000–4FFFF
SA8	0	1	0	1	X	X	X	X	128/64	0A0000–0BFFFF	50000–5FFFF
SA9	0	1	1	0	X	X	X	X	128/64	0C0000–0DFFFF	60000–6FFFF
SA10	0	1	1	1	X	X	X	X	128/64	0E0000–0FFFFF	70000–7FFFF
SA11	1	0	0	0	X	X	X	X	128/64	100000–11FFFF	80000–8FFFF
SA12	1	0	0	1	X	X	X	X	128/64	120000–13FFFF	90000–9FFFF
SA13	1	0	1	0	X	X	X	X	128/64	140000–15FFFF	A0000–AFFFF
SA14	1	0	1	1	X	X	X	X	128/64	160000–17FFFF	B0000–BFFFF
SA15	1	1	0	0	X	X	X	X	128/64	180000–19FFFF	C0000–CFFFF
SA16	1	1	0	1	X	X	X	X	128/64	1A0000–1BFFFF	D0000–DFFFF
SA17	1	1	1	0	X	X	X	X	128/64	1C0000–1DFFFF	E0000–EFFFF
SA18	1	1	1	1	X	X	X	X	128/64	1E0000–1FFFFF	F0000–FFFFF

Note: *Address range is A19–A-1 if device is in word mode (WORD# = V_{IL}). Address range is A19–A0 if device is in double word mode (WORD# = V_{IH}).*

Table 7. SecSi™ Sector Addresses for Bottom Boot Devices

Device	Sector Address A7–A0	Sector Size	(x16) Address Range	(x32) Address Range
Am29PL320DB	00000000	512 words/256 double words	000000h–0001FFh	00000h–000FFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address input A9. Address inputs must be as shown in Table 8. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (Table 4). Table 8 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 13. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 8. Am29PL320D Autoselect Codes (High Voltage Method)

Description		Mode	CE#	OE#	WE#	A19–12	A11–A10	A9	A8–A7	A6	A5–A4	A3	A2	A1	A0	DQ31–DQ8	DQ7–DQ0
Manufacturer ID: AMD			L	L	H	X	X	V_{ID}	X	L	X	X	X	L	L	X	01h
Device ID	Read Cycle 1	Word	L	L	H	X	X	V_{ID}	X	L	X	L	L	L	H	22h	7Eh
		Dbl. Word	L	L	H											222222h	
	Read Cycle 2	Word	L	L	H	X	X	V_{ID}	X	L	X	H	H	H	L	22h	03h
		Dbl. Word	L	L	H											222222h	
	Read Cycle 3	Word	L	L	H	X	X	V_{ID}	X	L	X	H	H	H	H	22h	00h (bottom boot) 01h (top boot)
		Dbl. Word	L	L	H											222222h	
SecSi™ Sector Indicator Bit			L	L	H	X	X	V_{ID}	X	L	X	L	L	H	H	X	80h (factory locked) 00h (not factory locked)
Sector Protection Verification			L	L	H	SA	X	V_{ID}	X	L	X	L	L	H	L	X	01h (protected) 00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note: *The autoselect codes may also be accessed in-system via command sequences. See Table 13.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Sector protection and unprotection must be implemented via programming equipment. The procedure requires high voltage (V_{ID}) to be placed on address input A9 and control input OE#. This method is compatible with programmer routines written for earlier AMD 3.0 volt devices. Publication number 24136 contains further details; contact an AMD representative to request a copy. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. Note that after the sector unprotect operation, all previously protected sectors must be re-protected using the sector protect algorithm.

The device features a temporary unprotect command sequence to allow changing array data in-system. See "Temporary Sector Unprotect Enable/Disable Command Sequence" for more information.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in double word mode (or address AAh in word mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 9–12. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 9–12. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 9. CFI Query Identification String

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase), D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} input present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} input present)
1Fh	3Eh	0004h	Typical timeout per single word/double word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for word/ double word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0006h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0005h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0004h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0000h 0000h 0080h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	0001h 0000h 0040h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0003h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	000Eh 0000h 0000h 0004h	Erase Block Region 4 Information

Table 12. Primary Vendor-Specific Extended Query

Addresses (Double Word Mode)	Addresses (Word Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0032h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0001h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = 4 Word Linear Burst, 02 = 8 Word Linear Burst, 03 = 32 Linear Burst, 04 = 4 Word Interleave Burst
4Ch	98h	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = not supported, D7–D4: volt; D3–D0: 100 millivolt.
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = not supported, D7–D4: volt; D3–D0: 100 millivolt.
50h	A0h	0000h	Program Suspend 00h = not supported, 01h = supported

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is a minimum of 128 words (64 double words) in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field. **Current version of device has 512 words; future versions will have only 128 words. This should be considered during system design.**

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize the that sector in any manner they choose. The customer-lockable version has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi™ Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up the device reverts to sending commands to the boot sectors.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In a factory locked device, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through the ExpressFlash service
- Both a random, secure ESN and customer code through the ExpressFlash service.

In devices that have an ESN, a Bottom Boot device will have the 8-word (4-double word) ESN in the lowest addressable memory area at addresses 000000h–000003h in double word mode (or 000000h–000007h in word mode). In the Top Boot device the starting address of the ESN will be at the bottom of the lowest 8 Kbyte boot sector at addresses 1F8000h–1F8003h in double word mode (or addresses FC0000h–FC0007h in word mode).

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. AMD programs the customer's code, with or without the random ESN. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Locked At the Factory

If the security feature is not required, the SecSi Sector can be treated as an additional Flash memory space, expanding the size of the available Flash array. **Current version of device has 512 words; future versions will have only 128 words. This should be considered during system design.** The SecSi Sector can be read, programmed, and erased as often as required. (*In upcoming versions of this device, the SecSi Sector erase function will not be available.*) Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The SecSi Sector can be locked in-system by performing the following steps:

- Write the three-cycle Enter SecSi Sector Region command sequence.
- Write 60h to any address (protect command).
- Wait 150 µs, and then write 40h to address 01h (verify command).
- Read from address 02h. The data should be 01h.
- Write the reset command (F0h to any address).
- Write the four-cycle Exit SecSi Sector command sequence to return to reading from the array.

  To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 1.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

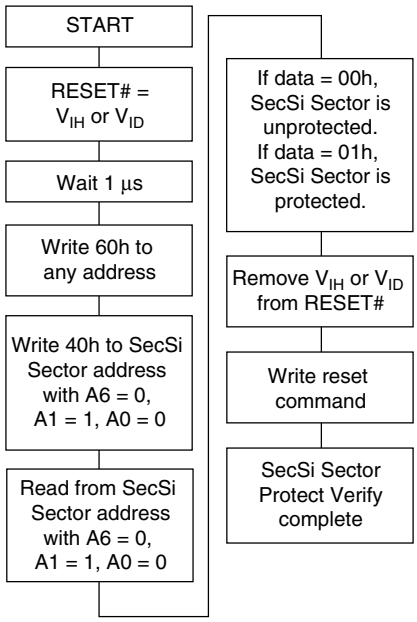


Figure 1. SecSi Sector Protect Verify

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}.

If the system asserts V_{IL} on the WP# input, the device disables program and erase functions in Sector 0 (for bottom boot) or Sector 18 (for top boot) independently of whether those sectors were protected or unprotected using the method described in "Sector Protection/Unprotection".

If the system asserts V_{IH} on the WP# input, the device reverts to whether Sector 0 or 18 was last set to be protected or unprotected. That is, sector protection or unprotection for that sector depends on whether they were last protected or unprotected using the method described in "Sector Protection/Unprotection".

Note that the WP# input must not be left floating or unconnected; inconsistent behavior of the device may result.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 13 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 13 defines the valid register command sequences. *Note that writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is required to return the device to normal operation*.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the

Erase Suspend mode, the system may once again read array data with the same exception. See “Erase Suspend/Erase Resume Commands” for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the “Reset Command” section, next.

See also “Requirements for Reading Array Data” in the “Device Bus Operations” section for more information. The Read Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don’t care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 13 shows the address and data requirements.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read any number of autoselect codes without reinitiating the command sequence.

Tables 13 and 14 show the address and data requirements for the command sequence. To determine sector protection information, the system must write to the appropriate sector address (SA). Tables 4 and 6 show the address range associated with each sector.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight-word (or four double word) electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Table 13 shows the address and data requirements for both command sequences. See also “SecSi™ (Secured Silicon) Sector Flash Memory Region” for further information.

Word/Double Word Program Command Sequence

The system may program the device by word or double word, depending on the state of the WORD# input. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 13 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See “Write Operation Status” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

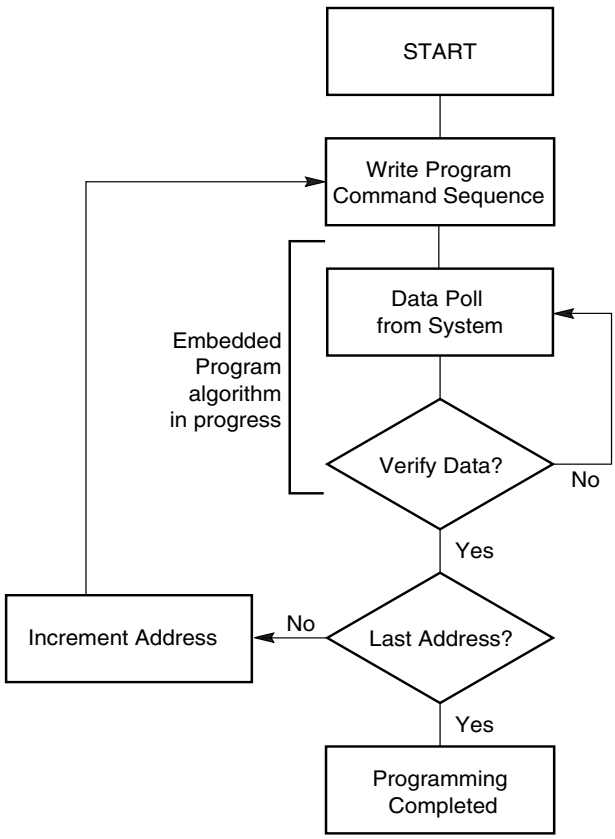
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a “0” back to a “1”.** Attempting to do so may halt the operation and set DQ5 to “1,” or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 13 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 2 illustrates the algorithm for the program operation. See the Program/Erase Operations table in "AC Characteristics" for parameters, and to Figure 17 for timing diagrams.



Note: *See Table 13 for program command sequence.*

Figure 2. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 13 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Program/Erase Operations tables in “AC Characteristics” for parameters, and to Figure 18 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 13 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the “DQ3: Sector Erase Timer” section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. (Refer to “Write Operation Status” for information on these status bits.)

Figure 3 illustrates the algorithm for the erase operation. Refer to the Program/Erase Operations tables in the “AC Characteristics” section for parameters, and to Figure 18 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase

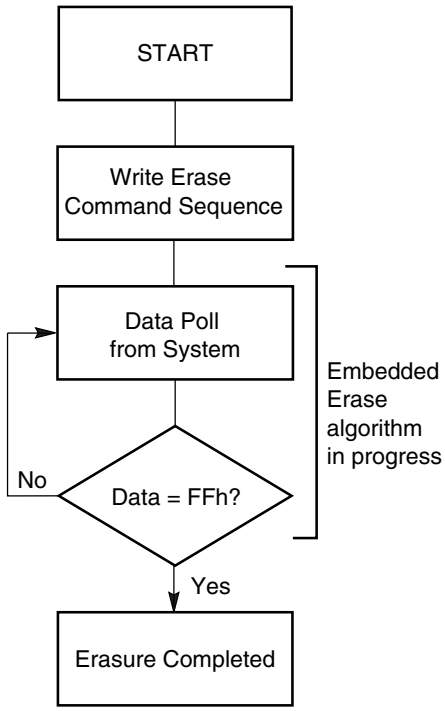
suspends" all sectors selected for erasure.) Note that unlock bypass programming is not allowed when the device is erase-suspended.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



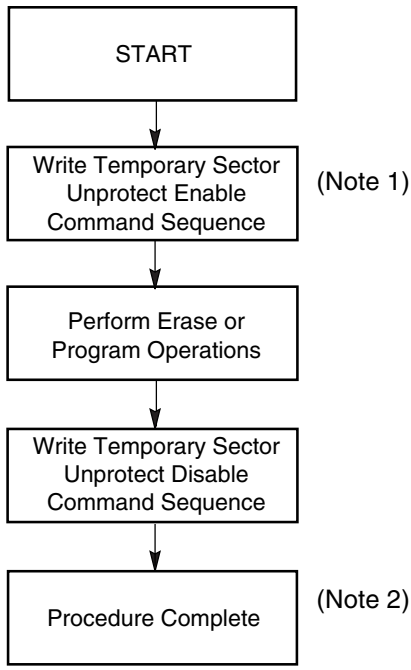
Notes:

1. *See Table 13 for erase command sequence.*
2. *See "DQ3: Sector Erase Timer" for more information.*

Figure 3. Erase Operation

Temporary Sector Unprotect Enable/Disable Command Sequence

The temporary unprotect command sequence is a four-bus-cycle operation. The sequence is initiated by writing two unlock write cycles. A third write cycle sets up the command. The fourth and final write cycle enables or disables the temporary unprotect feature. If the temporary unprotect feature is enabled, all sectors are temporarily unprotected. The system may program or erase data as needed. When the system writes the temporary unprotect disable command sequence, all sectors return to their previous protected or unprotected settings. See Table 13 and Figure 4 for more information.



Notes:

1. *All protected sectors are unprotected. If WP# = V_{IL}, the first or last 64 KByte sector will remain protected.*
2. *All previously protected sectors are protected once again.*

Figure 4. Temporary Sector Unprotect Algorithm

Command Definitions

Table 13. Command Definitions (Double Word Mode)

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	00	01				
	Device ID (Note 9)	6	555	AA	2AA	55	555	90	01	227E	0E	2203	0F	2200 2201
	SecSi™ Sector Factory Protect (Note 10)	4	555	AA	2AA	55	(BA) 555	90	(BA) X03	(Note 10)				
	Sector Protect Verify (Note 11)	4	555	AA	2AA	55	555	90	(SA) X02	(Note 11)				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
CFI Query (Note 12)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 13)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 15)		1	XXX	B0										
Erase Resume (Note 16)		1	XXX	30										
Temporary Sector Unprotect Enable		4	555	AA	2AA	55	555	E0	XXX	01				
Temporary Sector Unprotect Disable		4	555	AA	2AA	55	555	E0	XXX	00				

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ31–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *DQ31–DQ16 output 2222h for device ID reads. The device ID must be read across the fourth, fifth, and sixth cycles. The sixth cycle specifies 22222200h for bottom boot devices and 22222201h for top boot devices.*
10. *The data is 80h for factory locked and 00h for not factory locked.*
11. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
12. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*

Table 14. Command Definitions (Word Mode)

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	00	01				
	Device ID (Note 9)	6	AAA	AA	555	55	AAA	90	02	227E	1C	2203	1E	2200 / 2201
	SecSi™ Sector Factory Protect (Note 10)	4	AAA	AA	555	55	(BA) AAA	90	(BA) X06	(Note 10)				
	Sector Protect Verify (Note 11)	4	AAA	AA	555	55	AAA	90	(SA) X04	(Note 11)				
Enter SecSi Sector Region		3	AAA	AA	555	55	AAA	88						
Exit SecSi Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
CFI Query (Note 12)		1	55	98										
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 13)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend (Note 15)		1	XXX	B0										
Erase Resume (Note 16)		1	XXX	30										
Temporary Sector Unprotect Enable		4	AAA	AA	555	55	AAA	E0	XXX	01				
Temporary Sector Unprotect Disable		4	AAA	AA	555	55	AAA	E0	XXX	00				

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ31–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The device ID must be read across the fourth, fifth, and sixth cycles. The sixth cycle specifies 2200h for bottom boot devices and 2201h for top boot devices.*
10. *The data is 80h for factory locked and 00h for not factory locked.*
11. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
12. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 15 and the following subsections describe the functions of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

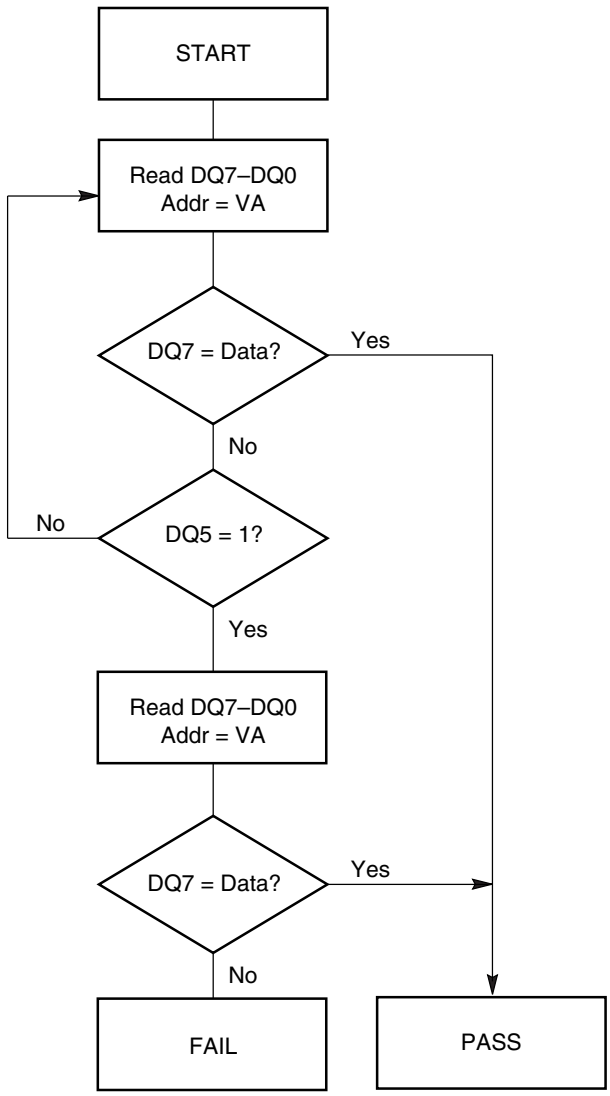
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement,” or “0.” The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. See Figure 18 in the “AC Characteristics” section.

Table 15 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5*

Figure 5. Data# Polling Algorithm

DQ6: Toggle Bit

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on “DQ7: Data# Polling”).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 15 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. Figure 20 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on “DQ2: Toggle Bit”.

DQ2: Toggle Bit

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 15 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. See also the DQ6: Toggle Bit subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

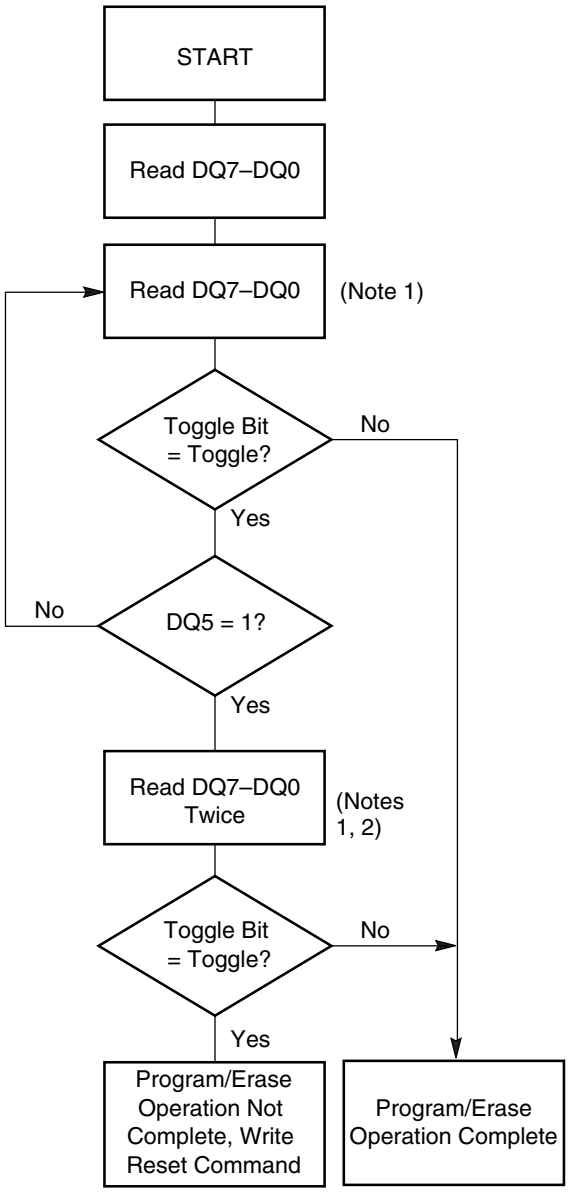
Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to "1". See text.*

Figure 6. Toggle Bit Algorithm

condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the "Write Operation Status" section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 15 shows the outputs for DQ3.

Table 15. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, ACC (Note 2) . . . . . –0.5 V to +13.0 V

All other inputs (Note 1) . . . . . –0.5 V to +5.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, voltages on inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/Os is V_{CC} + 0.5 V. During voltage transitions I/Os may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on inputs A9, OE#, and ACC is –0.5 V. During voltage transitions, A9 and OE# may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on input A9, OE#, and ACC is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

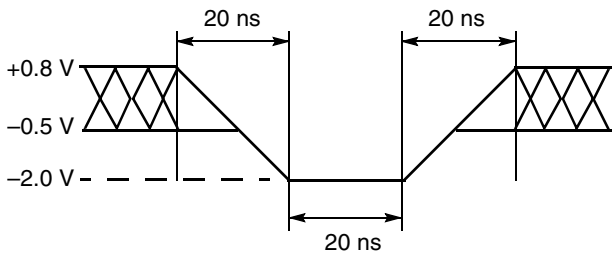


Figure 7. Maximum Negative Overshoot Waveform

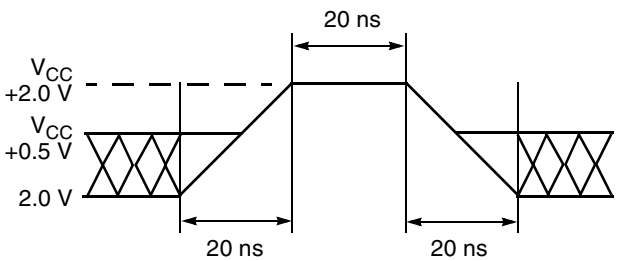


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range. . . . . 3.0 V to 3.6 V

V_{CC} for full voltage range . . . . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

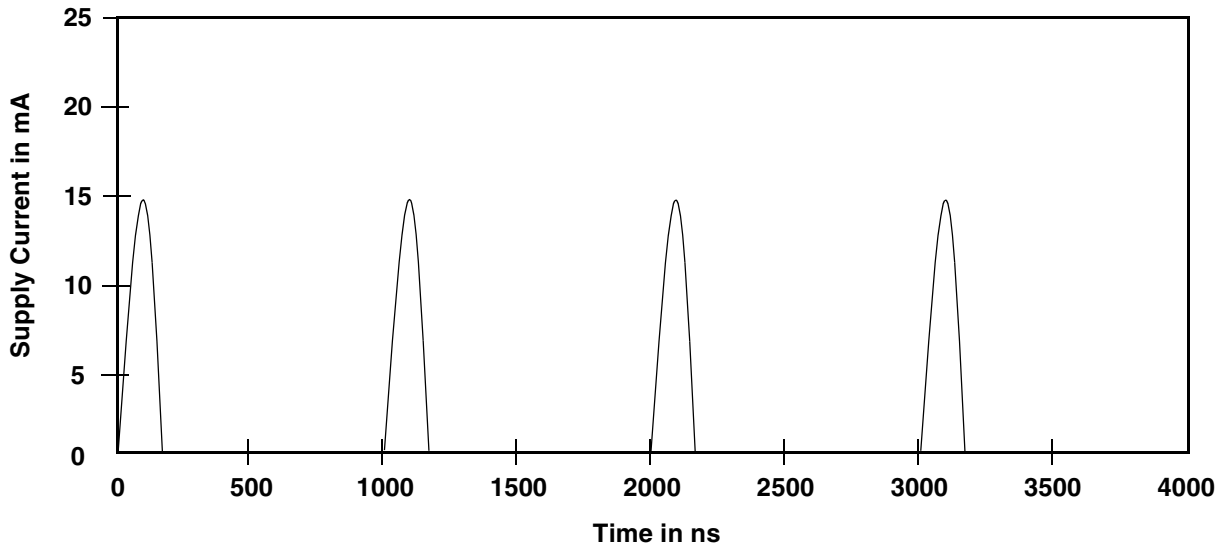
CMOS Compatible

Parameter Symbol	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Inter-Page Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	1 MHz		4	50	mA
			10 MHz		40	80	mA
I_{CC2}	V_{CC} Active Write Current (Notes 2, 4)	CE# = V_{IL}, OE# = V_{IH}			25	80	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE# = V_{CC}±0.3 V			2	5	µA
I_{CC4}	Automatic Sleep Mode (Notes 2, 3, 6)	$V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V	OE# = V_{IH}		1	5	µA
			OE# = V_{IL}		2	20	
I_{CC5}	V_{CC} Active Intra-Page Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}	10 MHz		15	50	mA
			33 MHz		50	80	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 0.3	V
V_{HH}	Voltage for Accelerated Programming on ACC			11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 ± 0.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 6)			2.3		2.5	V

Notes:

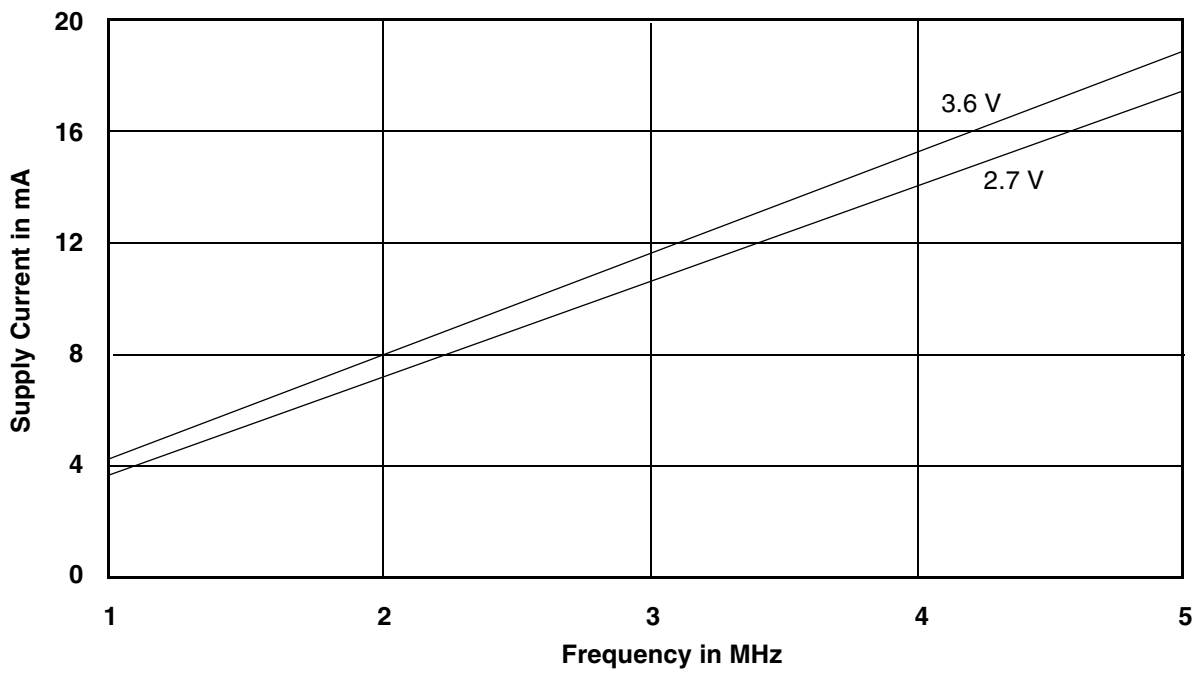
1. *The I_{CC} current listed is typically less than 4 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *The Automatic Sleep Mode current is dependent on the state of OE#.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
6. *Not 100% tested.*

DC CHARACTERISTICS (Continued)
Zero Power Flash



Note: *Addresses are switching at 1 MHz.*

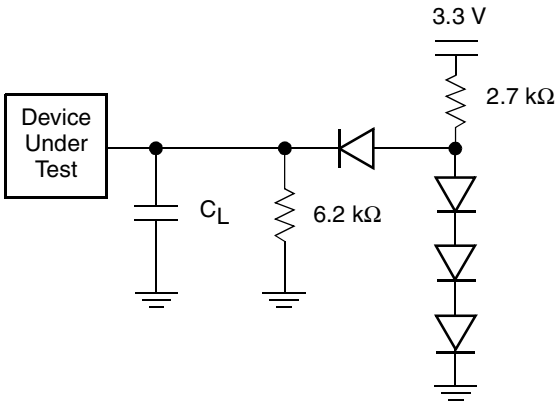
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 16. Test Specifications

Test Condition	All speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

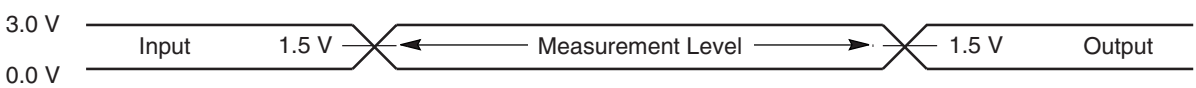


Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS
Read Operations

Parameter		Description		Test Setup		Speed Options			Unit
JEDEC	Std					60R	70R, 70	90	
t_{AVAV}	t_{RC}	Read Cycle Time			Min	60	70	90	ns
t_{AVQV}	t_{ACC}	Address Access Time		CE#=V_{IL}, OE#=V_{IL}	Max	60	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE#=V_{IL}	Max	60	70	90	ns
	t_{PACC}	Page Access Time			Max	20	25	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid			Max	20	25	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z			Max	16			ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z			Max	16			ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read			0			ns
			Toggle and Data# Polling			10			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, OE# or CE#, Whichever Occurs First (Note 1)			Min	0			ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 16 for test specifications.*

AC CHARACTERISTICS

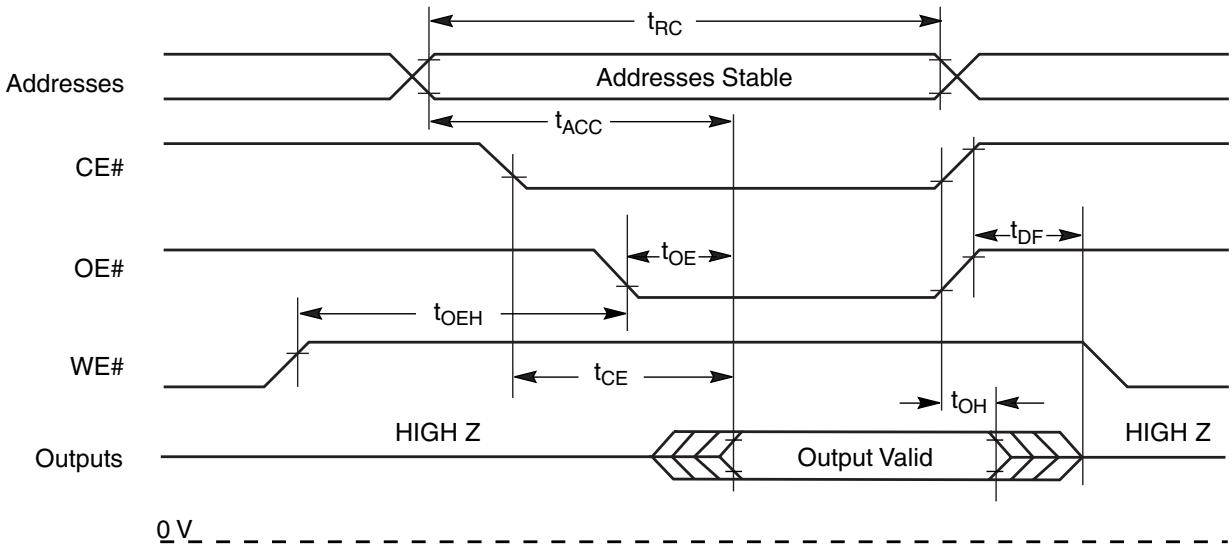
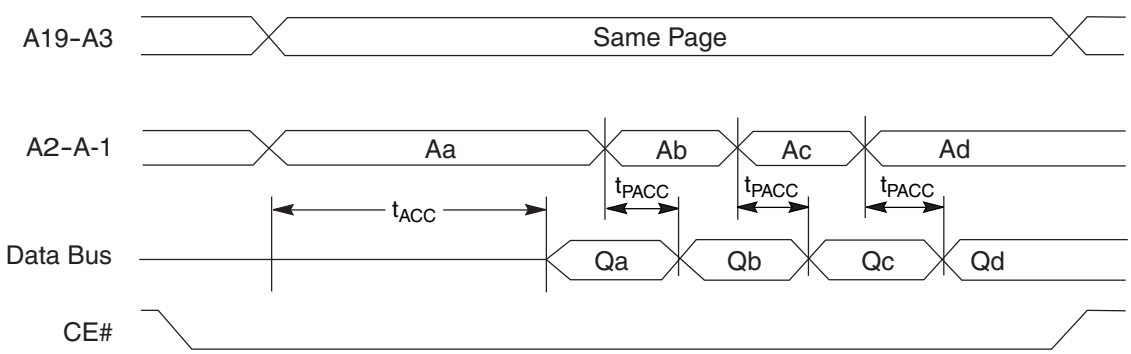


Figure 13. Conventional Read Operations Timings



Note: *Double Word Configuration: Toggle A2, A1, A0. Word Configuration: Toggle A2, A1, A0, A-1.*

Figure 14. Page Read Timings

AC CHARACTERISTICS

Double Word/Word Configuration (WORD#)

Parameter		Description		Speed Options			Unit
JEDEC	Std			60R	70R, 70	90	
	t_{ELFL}/t_{ELFH}	CE# to WORD# Switching Low or High	Max	5			ns
	t_{FLQZ}	WORD# Switching Low to Output HIGH Z	Max	16			ns
	t_{FHQV}	WORD# Switching High to Output Active	Min	60	70	90	ns

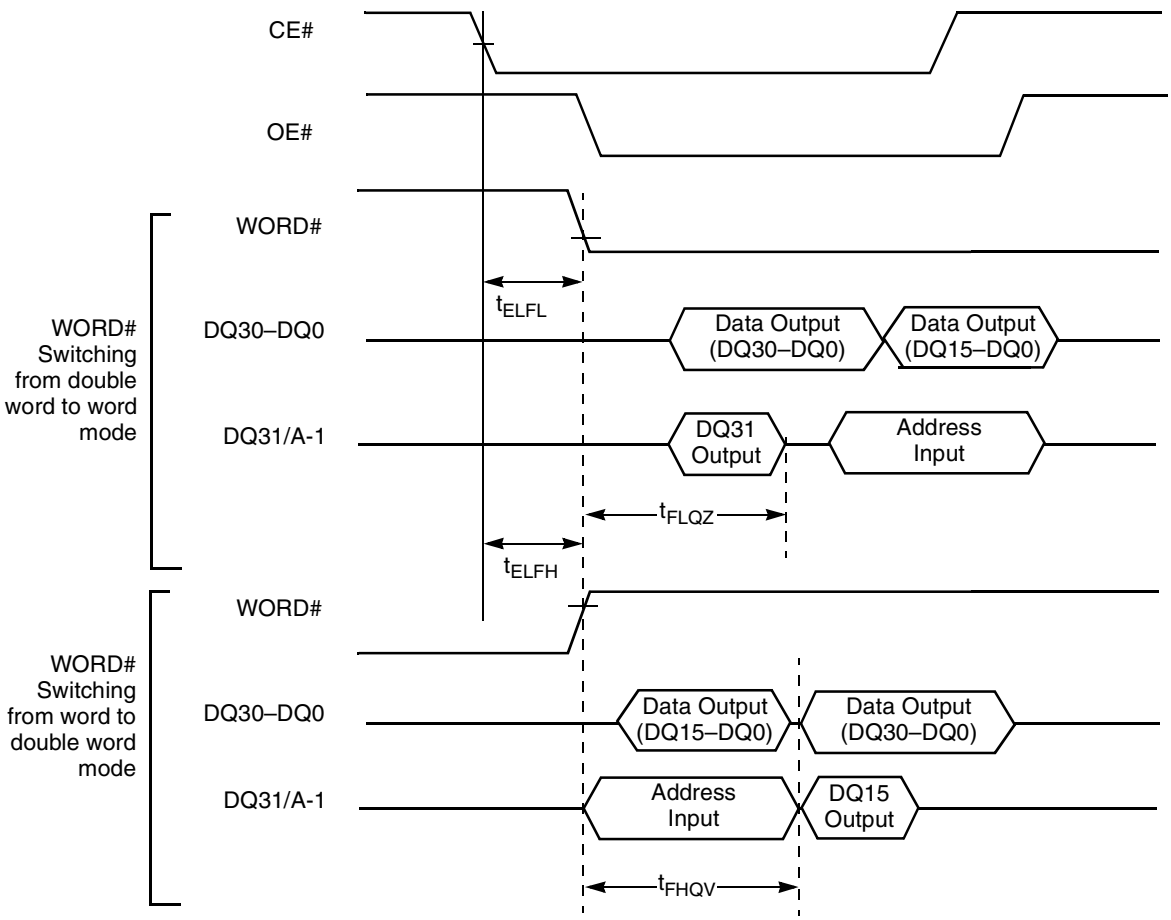
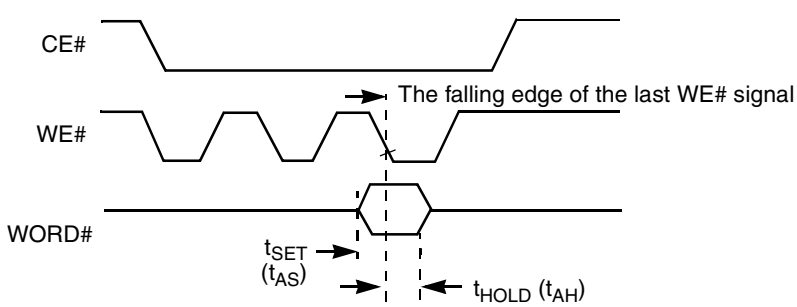


Figure 15. WORD# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 16. WORD# Timings for Write Operations

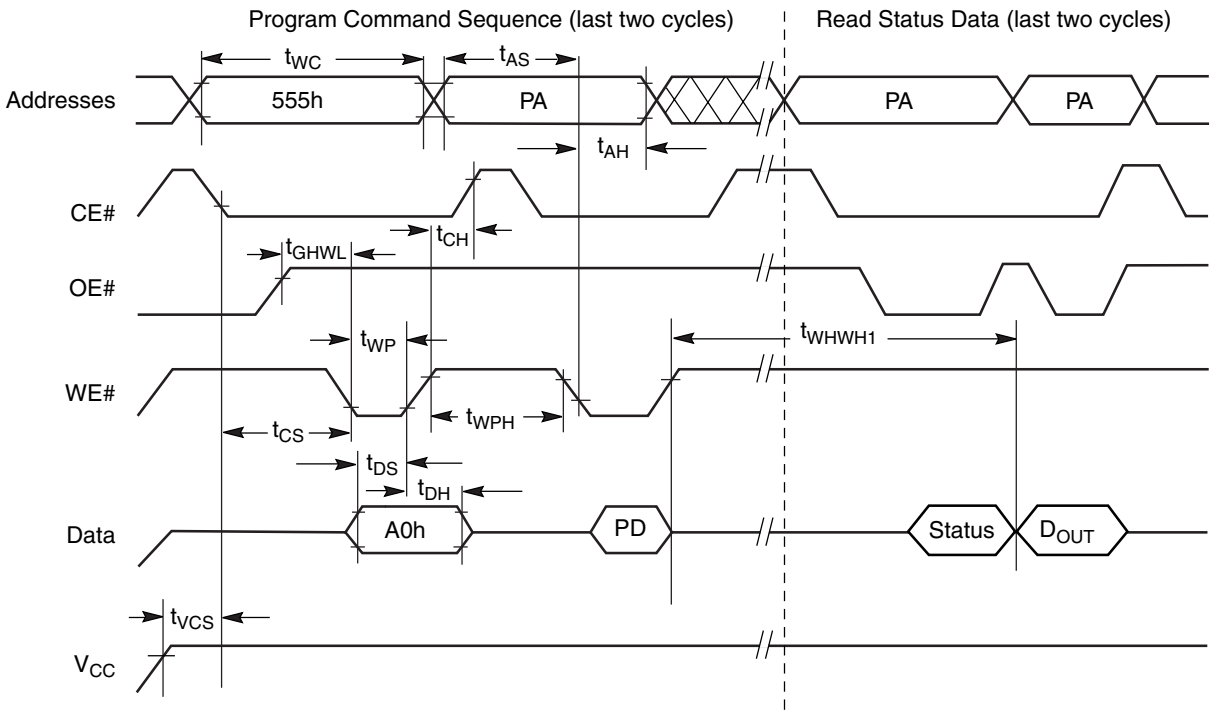
AC CHARACTERISTICS
Program/Erase Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std				60R	70R, 70	90	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	60	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OES}	Output Enable Setup Time		Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	25	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Word	Typ	14.3			µs
			Double Word	Typ	18.3			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	5			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50			µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS

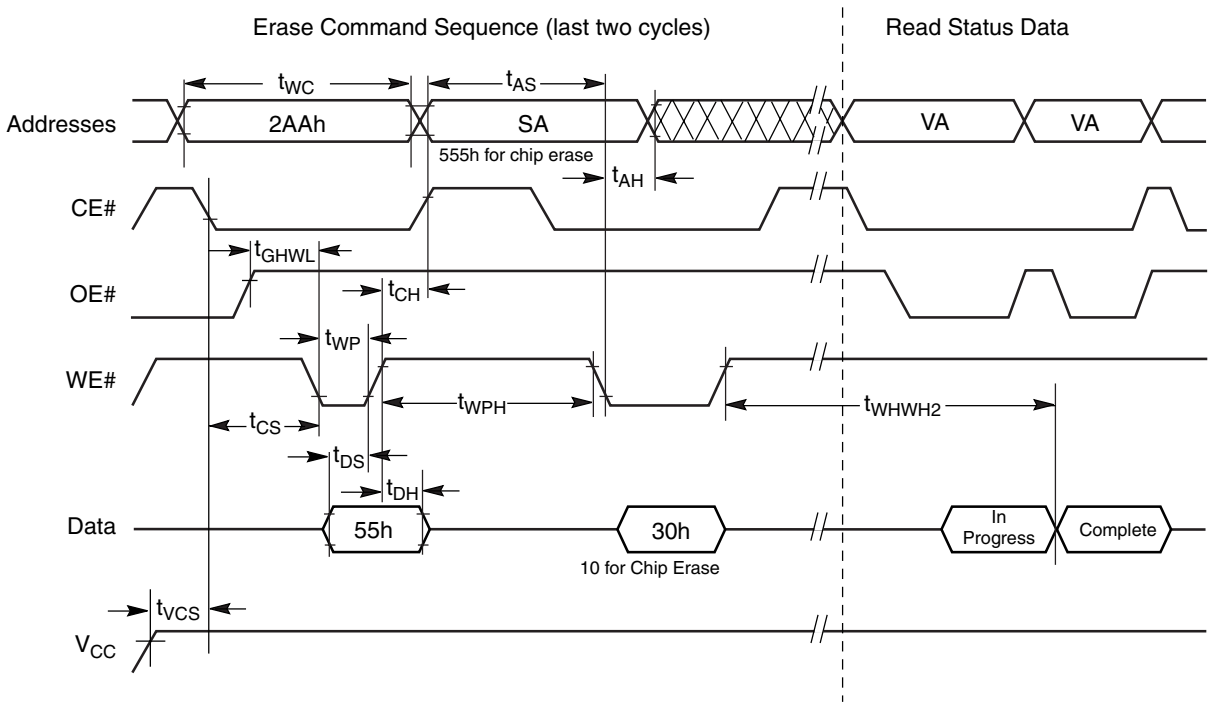


Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

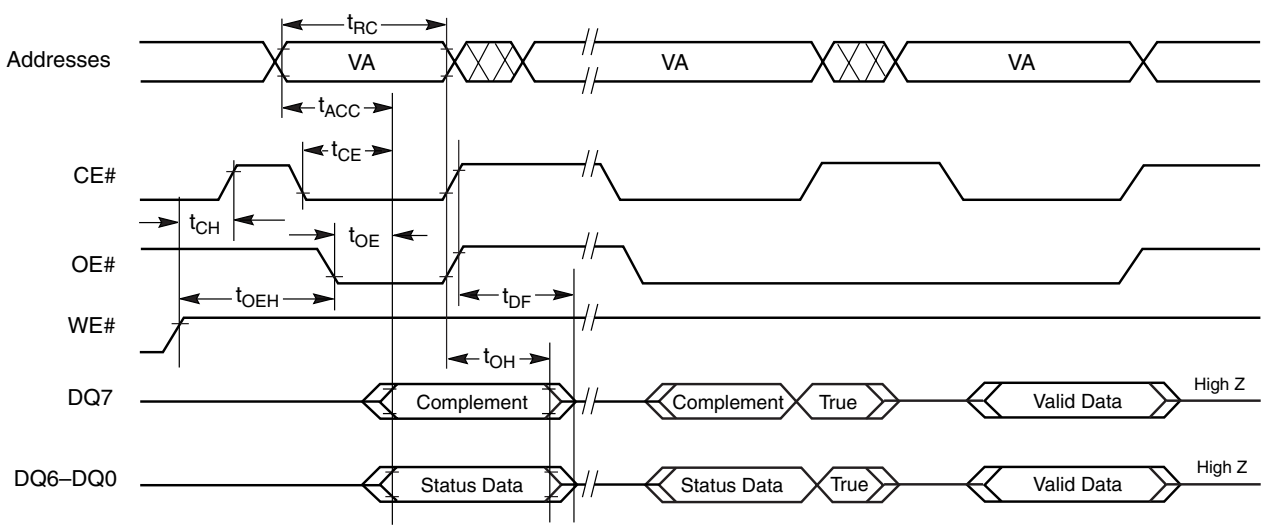
AC CHARACTERISTICS



Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*
2. *Illustration shows device in word mode.*

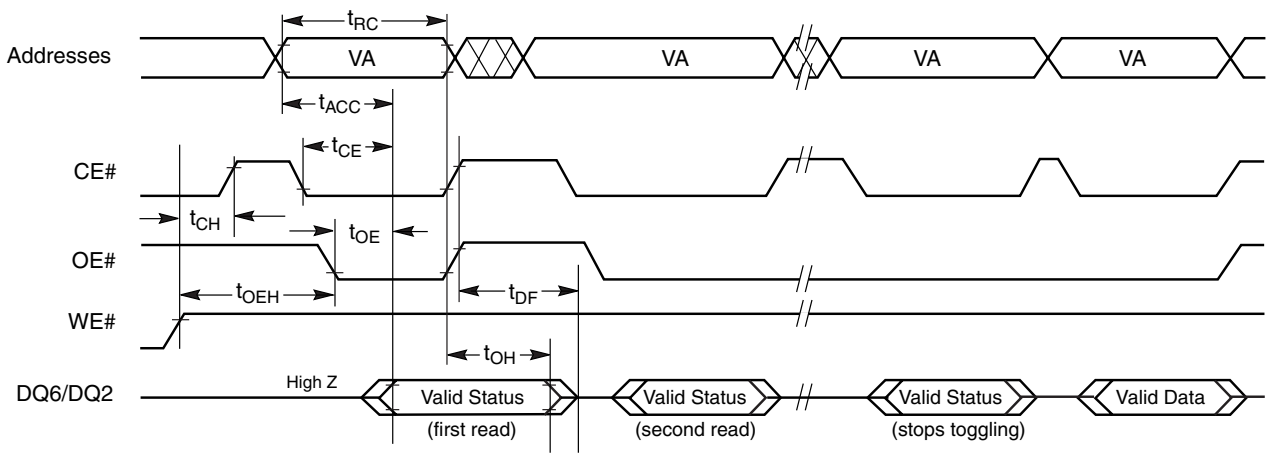
Figure 18. AC Waveforms for Chip/Sector Erase Operations



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle*

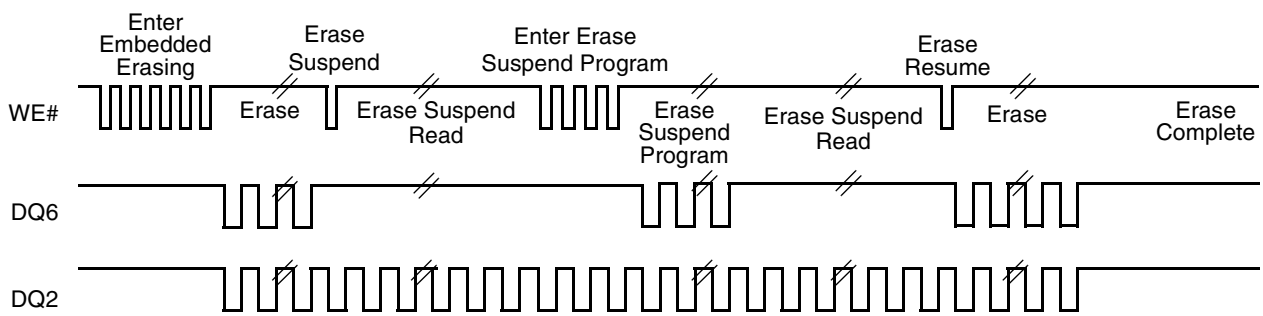
Figure 19. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 20. Toggle Bit Timings (During Embedded Algorithms)



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 21. DQ2 vs. DQ6 for Erase and Erase Suspend Operations

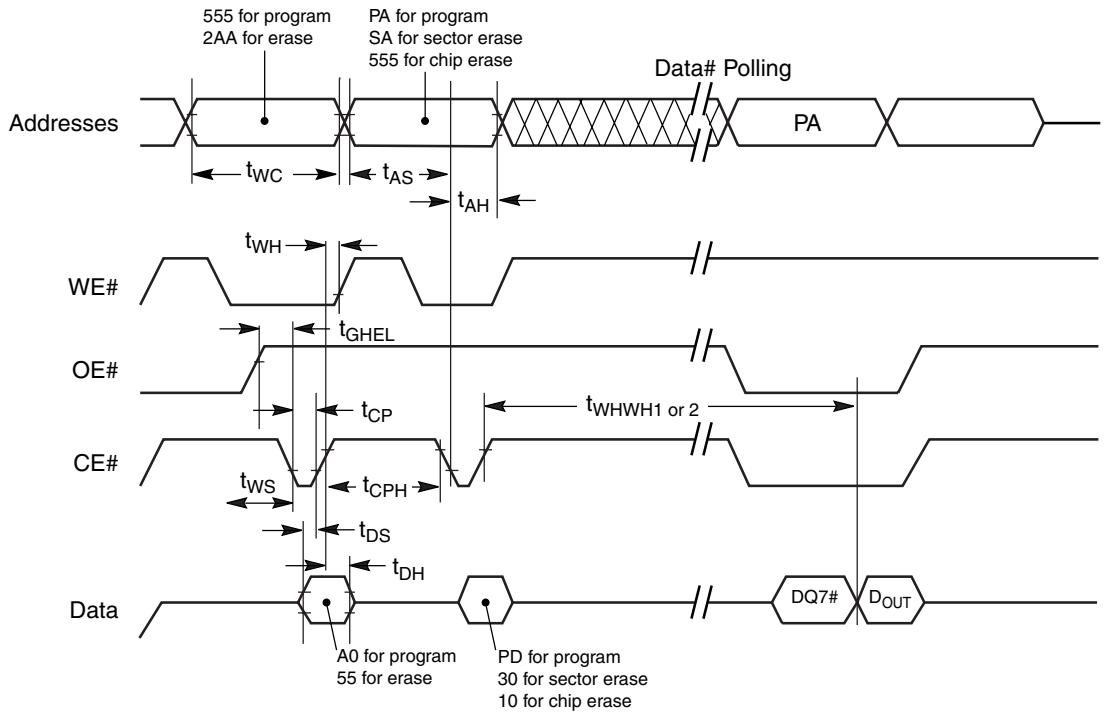
AC CHARACTERISTICS
Alternate CE# Controlled Erase/Program Operations

Parameter					Speed Options			
JEDEC	Std	Description			60R	70R, 70	90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	60	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OES}	Output Enable Setup Time		Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	25	30	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Word	Typ	14.3			µs
			Double Word	Typ	18.3			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	5			sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*
3. *Word mode address used as an example.*

Figure 22. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time, 96 and 128 KByte sector		2	60	s	Excludes 00h programming prior to erasure (Note 4)
Sector Erase Time, 8 and 16 KByte sector		0.5	60		
Chip Erase Time		33.5		s	
Word Programming Time		14.3	300	µs	Excludes system level overhead (Note 5)
Double Word Programming Time		18.3	360	µs	
Chip Programming Time (Note 3)	Word Mode	28	84	s	
	Double Word Mode	18	54	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 13 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all inputs except I/O inputs (including A9 and OE#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O inputs	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all inputs except V_{CC}. Test conditions: V_{CC} = 3.0 V, one input at a time.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

BGA PACKAGE CAPACITANCE

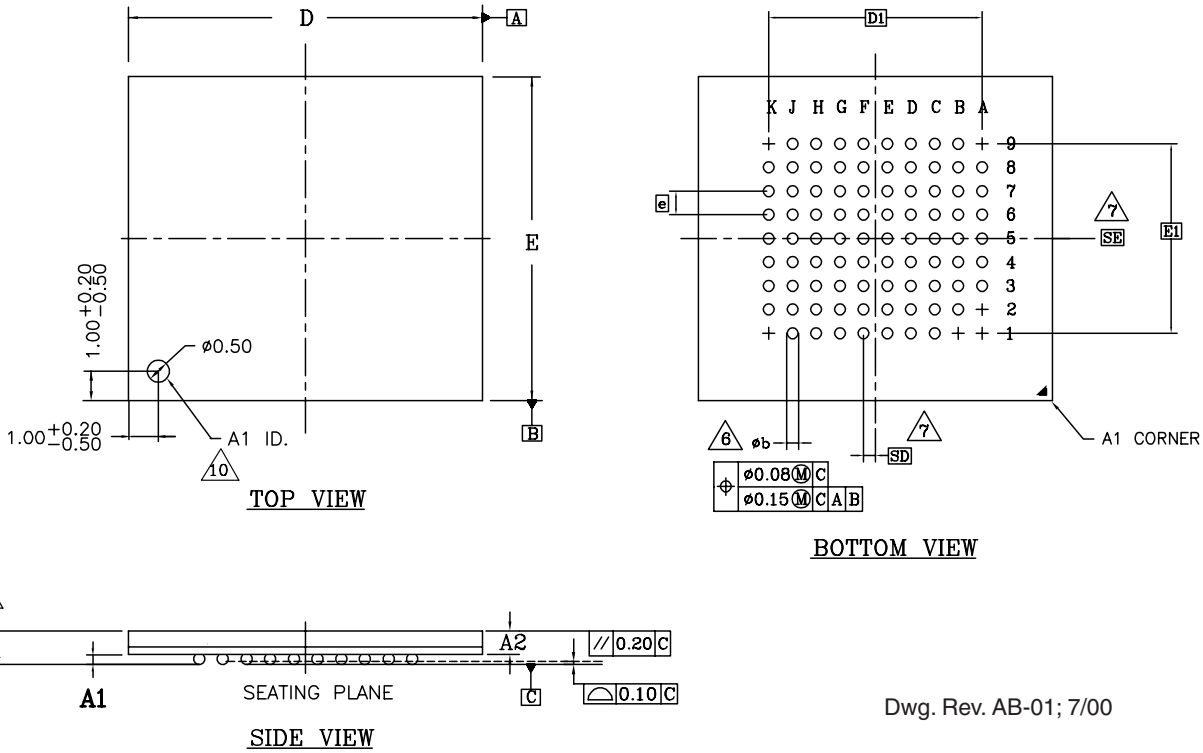
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PHYSICAL DIMENSIONS

FBF084—84-Ball Fine Pitch Ball Grid Array (FBGA) 11 x 12 mm



Dwg. Rev. AB-01; 7/00

PACKAGE	FBF084			
JEDEC	N/A			
	11.00mmx12.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.20 BSC.			BALL FOOTPRINT
E1	6.40 BSC.			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	9			ROW MATRIX SIZE E DIRECTION
N	84			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A1,A2,A9,B1,K1,K9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95−1, SPP−010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. FOR PACKAGE THICKNESS A IS THE CONTROLLING DIMENSION.

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

REVISION SUMMARY

Revision A (March 7, 2001)

Initial release.

Revision B (June 12, 2001)

Global

Added 70R speed option.

Changed data sheet status from Advance Information to Preliminary.

Distinctive Characteristics

SecSi Sector: Added note to future compatibility.

Power Consumption: Replaced stated maximum values with typical values.

General Description

Added section on SecSi Sector.

SecSi™ (Secured Silicon) Sector Flash Memory Region

Added note to indicate sector size and erase functionality for future devices.

DC Characteristics

Added typical values for I_{CC1}–I_{CC5} to table. Corrected V_{IN} test condition specification to V_{CC}.

Figure 10, Typical I_{CC1} vs. Frequency

Changed scale on Y-axis to 4 mA divisions.

Revision B+1 (August 30, 2001)

Autoselect Command Sequence

Modified section to point to appropriate tables for autoselect functions.

Accelerated Program Operation

Specified a voltage range for V_{HH}.

Table 13, Command Definitions

Corrected the autoselect device ID command sequence. The device ID is read in cycles 4, 5, and 6 of a single command sequence, not as three separate command sequences as previously shown. Separated the word and double word command sequences into two tables for easier reference.

DC Characteristics

Added V_{HH} parameter to table.

Revision C (October 22, 2002)

Global

Deleted preliminary status from data sheet.

Distinctive Characteristics

Clarified endurance specification from “write cycles” to “erase cycles.”

SecSi™ (Secured Silicon) Sector Flash Memory Region

Added text and figure on SecSi Sector Protect Verify function.

Command Definitions

Modified first paragraph to indicate device behavior when incorrect data or commands are written.

DC Characteristics

Changed V_{IL} maximum specification. Changed V_{CC} test condition for V_{ID} parameter.

BGA Ball Capacitance

Added table.

Revision C+1 (July 21, 2003)

Common Flash Interface (CFI)

Changed URL for CFI publications.

Command Definitions

Added the phrase “in the improper sequence” to cautionary text in first paragraph.

Erase and Programming Performance

Changed typical sector erase time and typical chip erase time. Added typical and maximum sector erase times pertaining to 8 and 16 Kword sectors.

Revision C+2 (October 2, 2003)

Erase Suspend/Erase Resume Commands

Modified text to “Note that unlock bypass programming is not allowed when the device is erase-suspended” in the third paragraph.

AC Characteristics - Double Word/Word Configuration (WORD#) diagram

Modified all instances of DQ14 to DQ30, DQ7 to DQ15, and DQ15 to DQ31.

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