

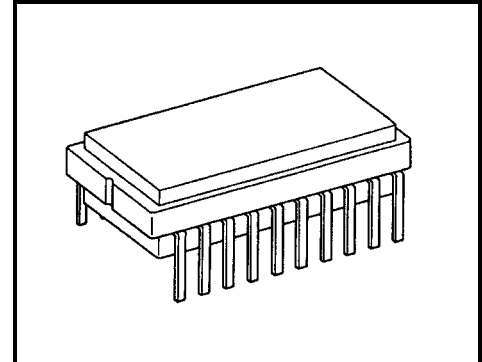
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

## TCD1001P

The TCD1001P is a high sensitive and low dark current 128-elements linear image sensor which includes CCD drive circuit, clamp circuit and sample & hold circuit. The CCD drive circuit consists of the pulse generator therefore it is possible to easy drive by applying simple pulses. The sensor is designed for scanner.

### FEATURES

- Number of Image Sensing Elements : 128 elements
- Image Sensing Element Size : 32 $\mu$ m $\times$ 32 $\mu$ m on 32 $\mu$ m centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 3 Input pulses 5V
- Internal Circuit : Sample & Hold circuit, Clamp circuit
- Package : 20 pin



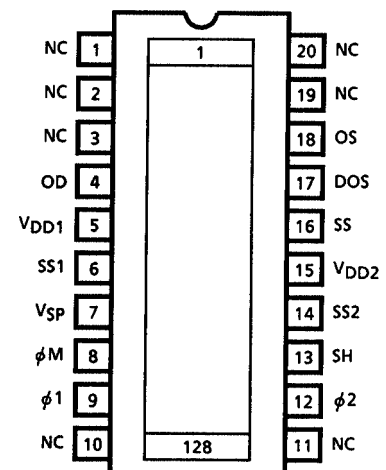
Weight: 1.0g (typ.)

### MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATING	UNIT
Master Clock Voltage	$V_{\phi M}$	-0.3~8	V
Clock Pulse Voltage	$V_{\phi}$		
Shift Pulse Voltage	$V_{SH}$		
Power Supply Voltage (Analog)	$V_{AD}$	-0.3~15	V
Power Supply Voltage (Digital)	$V_{DD1}$		
	$V_{DD2}$		
Sample & Hold Switch Voltage	$V_{SP}$	-0.3~15	V
Operating Temperature	$T_{opr}$	0~60	$^{\circ}$ C
Storage Temperature	$T_{stg}$	-25~85	$^{\circ}$ C

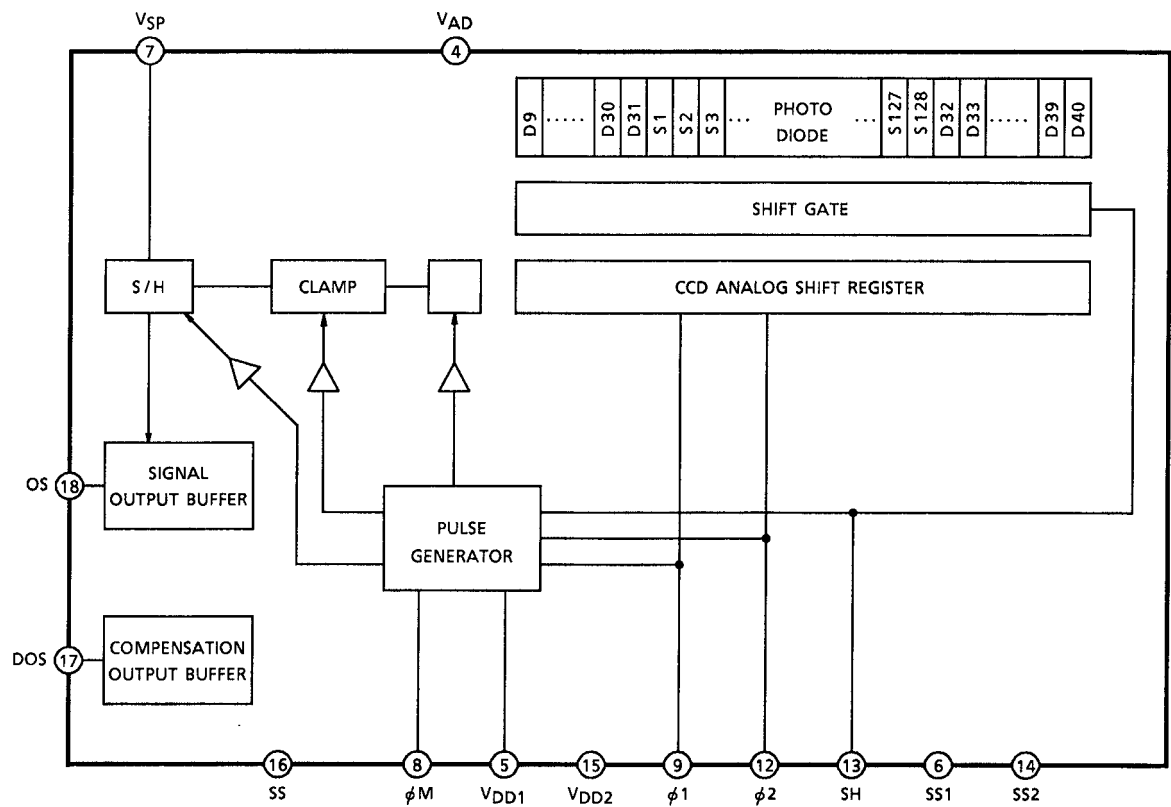
Note 1: All voltage are with respect to SS terminals(Ground).

### PIN CONNECTION



(TOP VIEW)

CIRCUIT DIAGRAM



PIN NAMES

$\phi_M$	Master Clock	$V_{AD}$	Power (Analog)
$\phi_1$	Clock (Phase 1)	$V_{DD1}$	Power (Digital, 12V)
$\phi_2$	Clock (Phase 2)	$V_{DD2}$	Power (Digital, 12V)
SH	Shift Gate	SS	Ground (Analog)
OS	Signal Output	SS1	Ground (Digital, 12V)
DOS	Compensation Output	SS2	Ground (Digital, 12V)
NC	Non Connection	$V_{SP}$	Sample and Hold Switch

## OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V<sub>AD</sub> = V<sub>DD1</sub> = V<sub>DD2</sub> = 12V, V<sub>φM</sub> = V<sub>φ</sub> = V<sub>SH</sub> = 5V (PULSE), f<sub>φ</sub> = 1.0MHz, t<sub>INT</sub> (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP, LOAD RESISTANCE = 100kΩ)

CHARACTERISTICS	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Sensitivity	R	63.7	85	106	V / lx·s	
Photo Response Non Uniformity	PRNU (1)	—	—	10	%	(Note 2)
	PRNU (3)	—	3	12	mV	(Note 3)
Saturation Output Voltage	V <sub>SAT</sub>	1.2	2.0	—	V	(Note 4)
Saturation Exposure	SE	—	0.02	—	lx·s	(Note 5)
Dark Signal Voltage	V <sub>DRK</sub>	—	4	8	mV	(Note 6)
Dark Signal Non Uniformity	D <sub>SNU</sub>	—	2	5	mV	(Note 6)
Analog Current Dissipation	I <sub>AD</sub>	—	8.0	12	mA	
Digital Current Dissipation	I <sub>DD1</sub>	—	—	1	mA	
	I <sub>DD2</sub>	—	10.0	15	mA	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	Z <sub>O</sub>	—	0.5	1.0	kΩ	
DC Signal Output Voltage	V <sub>OS</sub>	3.5	5.0	6.5	V	(Note 7)
DC Compensation Output Voltage	V <sub>DOS</sub>	3.5	5.0	6.5	V	(Note 7)
DC Differential Error Voltage	V <sub>OS</sub> - V <sub>DOS</sub>	—	—	400	mV	

Note 2: PRNU (1) is measured at 50% of SE (Typ.)

$$\text{Definition of PRNU : PRNU} = \frac{\Delta \bar{\chi}}{\bar{\chi}} \times 100(\%)$$

Where  $\bar{\chi}$  is average of total signal outputs and  $\Delta \chi$  is the maximum deviation from  $\bar{\chi}$  under uniform illumination.

Note 3: PRNU (3) is defined as maximum voltage with next pixel where measured 5% of SE (Typ.)

Note 4: V<sub>SAT</sub> is defined as minimum Saturation Output Voltage of all effective pixels.

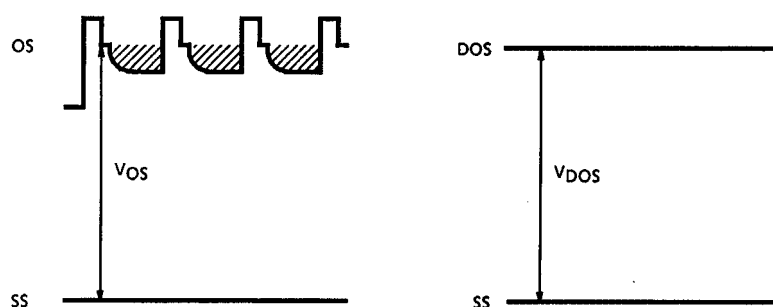
$$\text{Note 5: Definition of SE : SE} = \frac{V_{SAT}}{R} (\text{lx} \cdot \text{s})$$

Note 6: V<sub>DRK</sub> is defined as average dark signal voltage of all effective pixels.

D<sub>SNU</sub> is defined as different voltage between V<sub>DRK</sub> and V<sub>MDK</sub> when V<sub>MDK</sub> is maximum dark signal voltage.



Note 7: DC signal output voltage and DC compensation output voltage are defined as follows:



## OPERATING CONDITION

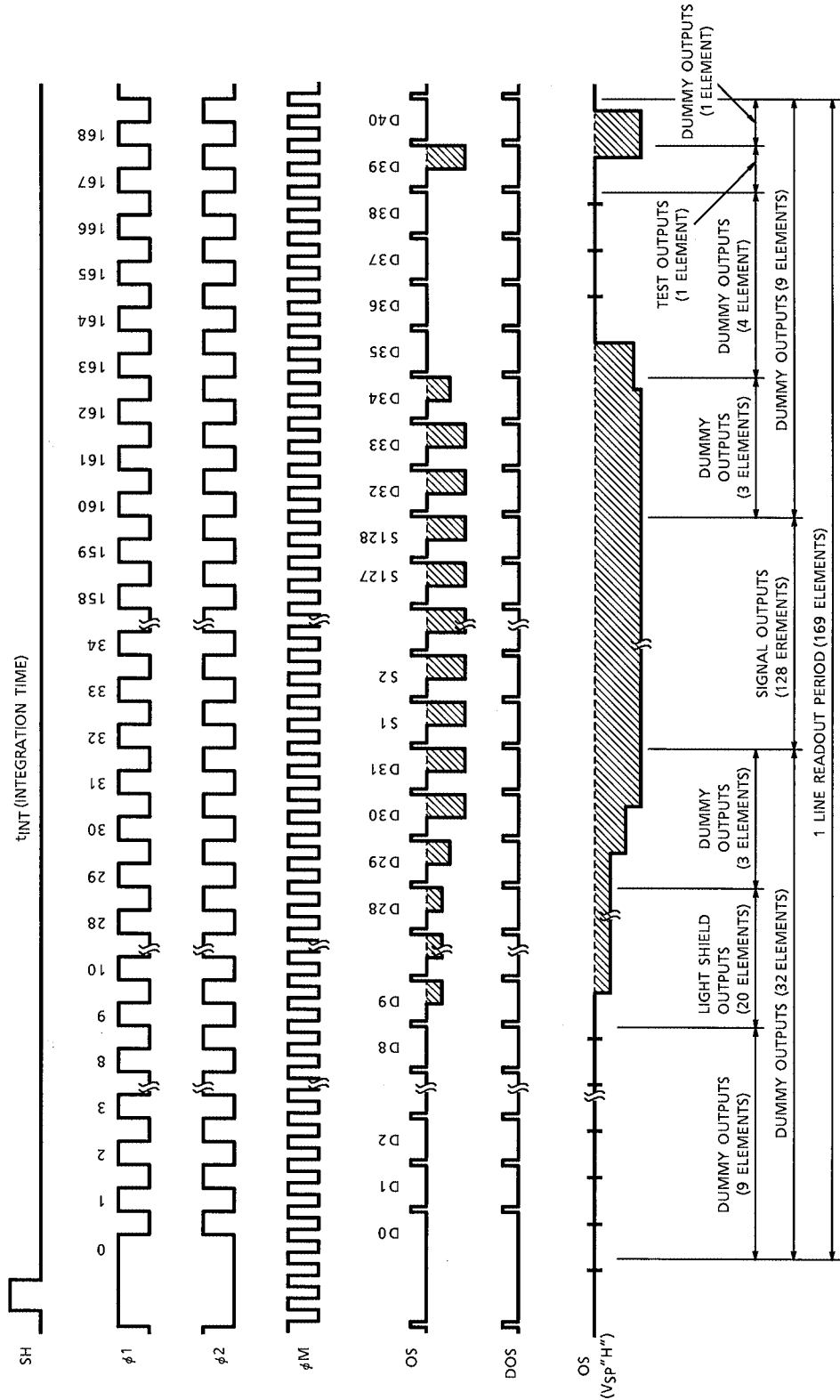
CHARACTERISTICS		SYMBOL	MIN	TYP.	MAX	UNIT
Master Clock Pulse Voltage	"H" Level	$V_{\phi M}$	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Clock Pulse Voltage	"H" Level	$V_{\phi 1}$	4.5	5.0	5.5	V
	"L" Level	$V_{\phi 2}$	0	—	0.5	
Shift Pulse Voltage	"H" Level	$V_{SH}$	$V_{\phi}-0.5$	$V_{\phi}$	$V_{\phi}$	V
	"L" Level		0	—	0.5	
Sample and Hold Switch Voltage*	"H" Level	$V_{SP}$	4.5	5.0	13.0	V
	"L" Level		0	—	0.5	
Power Supply Voltage (Analog)		$V_{AD}$	11.4	12.0	13.0	V
Power Supply Voltage (Digital)		$V_{DD1}$	11.4	12.0	13.0	V
		$V_{DD2}$	11.4	12.0	13.0	

\*: Supply "H" Level to  $V_{SP}$  terminal when sample-and-hold circuit is used, when sample-and-hold circuit is not used supply "L" Level to  $V_{SP}$  terminal.

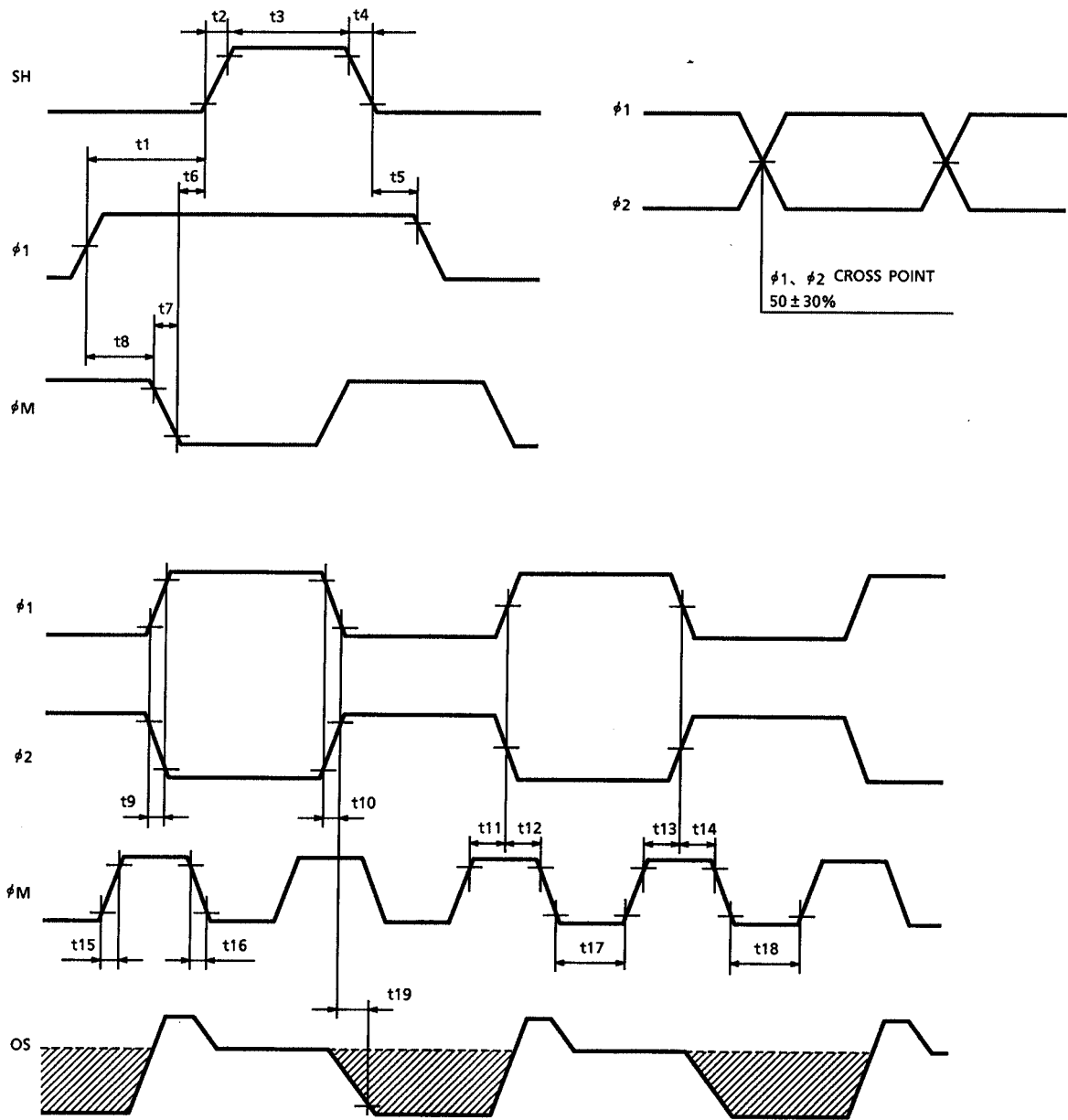
## CLOCK CHARACTERISTICS (Ta = 25°C)

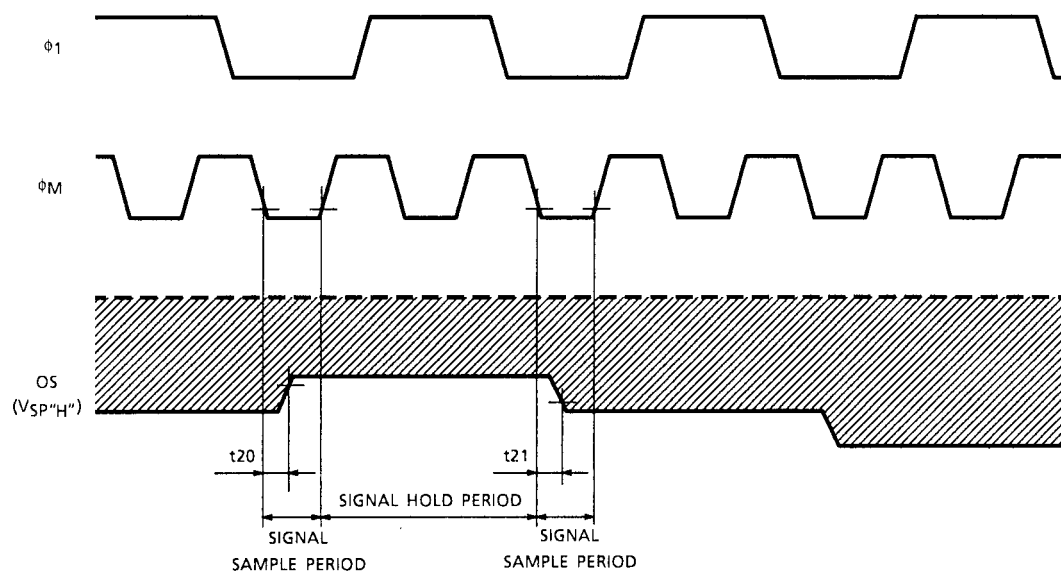
CHARACTERISTICS	SYMBOL	MIN	TYP.	MAX	UNIT
Master Clock Pulse Frequency	$f_{\phi M}$	—	2.0	6.0	MHz
Clock Pulse Frequency	$f_{\phi}$	—	1.0	3.0	MHz
Master Clock Pulse Capacitance	$C_{\phi M}$	—	10	20	pF
Clock Capacitance	$C_{\phi}$	—	100	200	pF
Shift Gate Capacitance	$C_{SH}$	—	50	100	pF

TIMING CHART



TIMING REQUIREMENTS



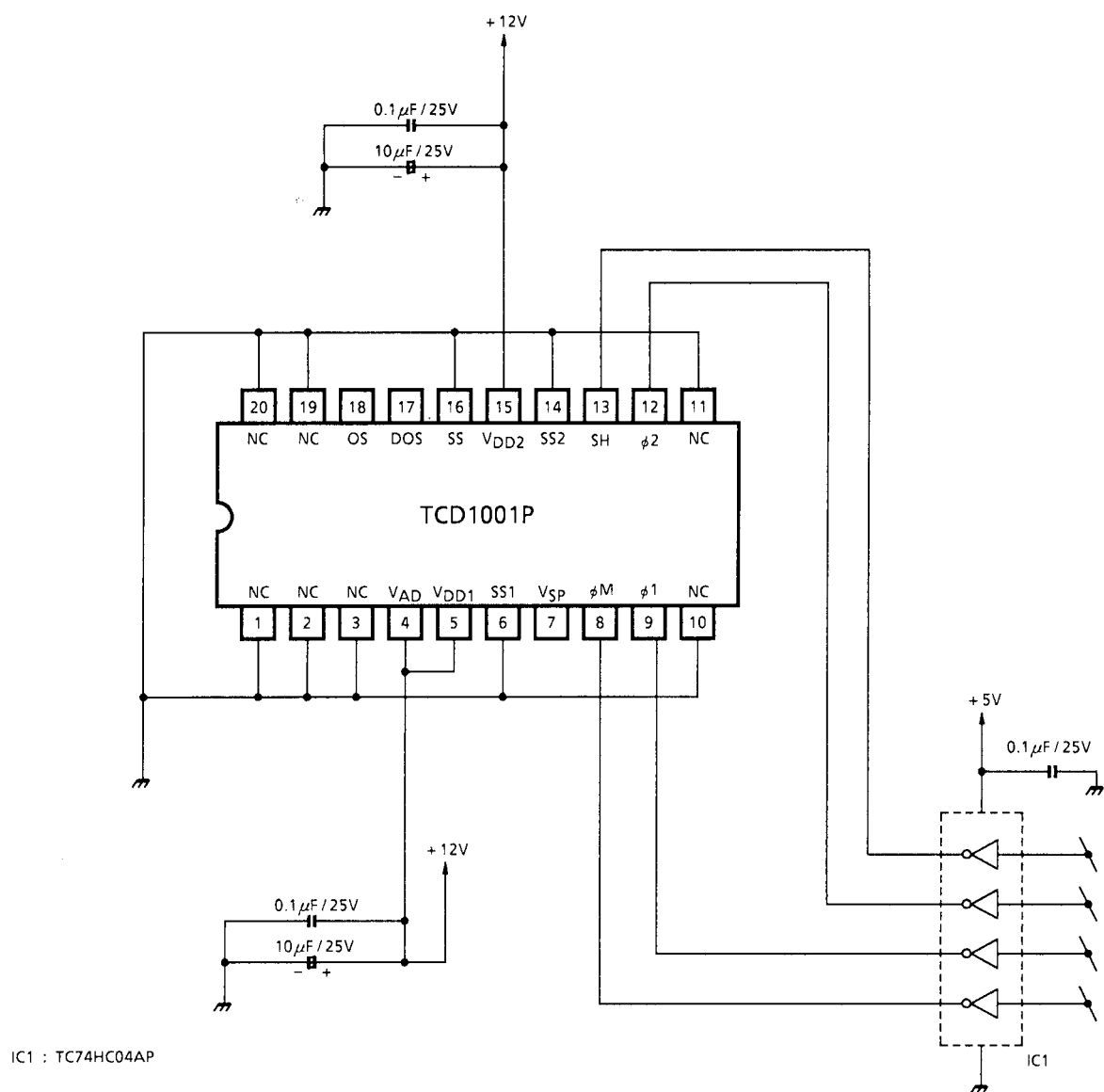


CHARACTERISTICS	SYMBOL	MIN	TYP. (Note 2)	MAX	UNIT
Pulse Timing of SH and $\phi_1$ , $\phi_2$	t1	60	300	—	ns
	t5	0	300	—	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	300	1000	—	ns
Pulse Timing of SH and $\phi_M$	t6	20	50	—	ns
$\phi_1$ , $\phi_2$ Pulse Rise Time, Fall Time	t9, t10	0	20	—	ns
Pulse Timing of $\phi_1$ , $\phi_2$ and $\phi_M$	t11, t13	20	100	—	ns
	t8, t12, t14	40	100	—	ns
$\phi_M$ Pulse Rise Time, Fall Time	t7, t15, t16	0	20	—	ns
$\phi_M$ Pulse Width	t17, t18	80	250	—	ns
Video Data Delay Time (Note 3)	t19	—	45	—	ns
S / H Video Data Delay Time	t20, t21	—	70	—	ns

Note 2: TYP. is the case of  $f_{\phi} = 1\text{MHz}$ .

Note 3: Load Resistance is 100k $\Omega$ .

## TYPICAL DRIVE CIRCUIT





**CAUTION****1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N<sub>2</sub>. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

**2. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but interior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers or pincer.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

**3. Incident Light**

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

**4. Lead Frame Forming**

Since this package is not strong against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

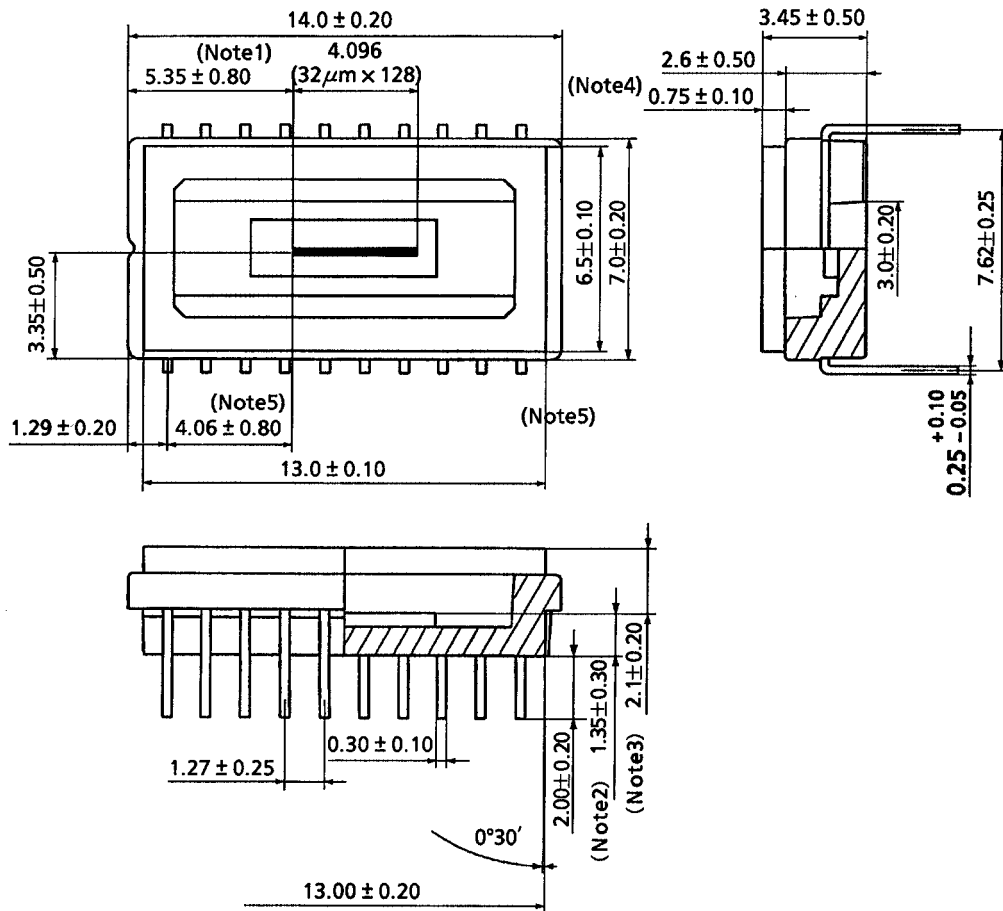
**5. Soldering**

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

## PACKAGE DIMENSIONS

Unit : mm



Note1: No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

Note2: TOP OF CHIP TO BOTTOM OF PACKAGE.

Note3: TOP OF CHIP TO OF PACKAGE.

Note4: GLASS THICKNESS ( $n = 1.5$ )

Note5: No. 1 SENSOR ELEMENT (S1) TO CENTER OF No. 1 PIN.

Weight: 1.0g (typ.)

**RESTRICTIONS ON PRODUCT USE**

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