

August 2003

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

Monolithic Quad SPST CMOS Analog Switches

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- ON-Resistance $<35\Omega$ Max
- Low Power Consumption ($P_D <35\mu W$)
- Fast Switching Action
 - $t_{ON} <175ns$
 - $t_{OFF} <145ns$
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG411/883 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON resistance ($<35\Omega$) and faster switch time ($t_{ON} <175ns$) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

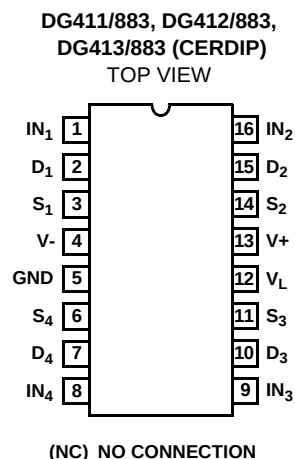
The improvements in the DG411/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V_{P-P} signals. Power supplies may be single-ended from +5V to +34V, or split from $\pm 5V$ to $\pm 20V$.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a $\pm 15V$ analog input range. The switches in the DG411/883 and DG412/883 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413/883 (#1 and #4) use the logic of the DG211 and DG411/883 (i.e. a logic "0" turns the switch ON) and the other two switches use DG212 and DG412/883 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

Part Number Information

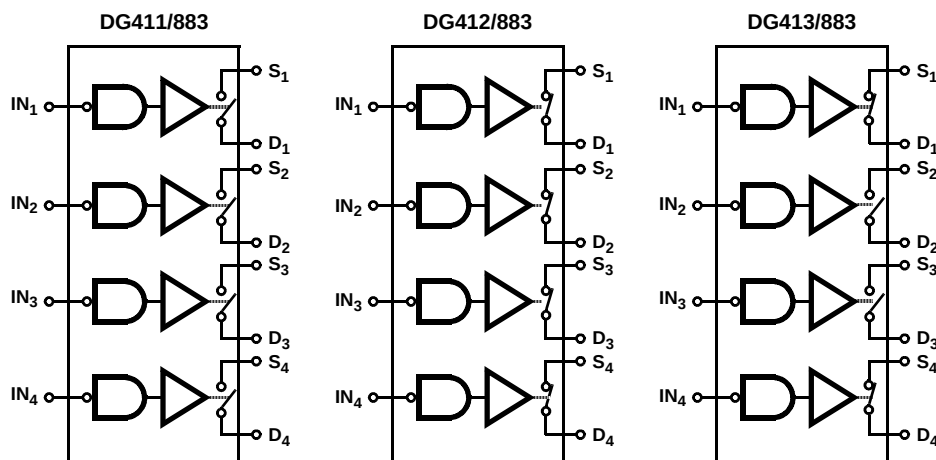
PART NUMBER	TEMP. RANGE	PACKAGE
DG411AK/883	-55°C to +125°C	16 Lead CerDIP
DG412AK/883	-55°C to +125°C	16 Lead CerDIP
DG413AK/883	-55°C to +125°C	16 Lead CerDIP

Pinout



Functional Diagrams

Four SPST Switches per Package Switches Shown for Logic "1" Input



DG411/883, DG412/883, DG413/883**Pin Description**

PIN	SYMBOL	DESCRIPTION
1	IN ₁	Logic Control for Switch 1
2	D ₁	Drain (Output) Terminal for Switch 1
3	S ₁	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S ₄	Source (Input) Terminal for Switch 4
7	D ₄	Drain (Output) Terminal for Switch 4
8	IN ₄	Logic Control for Switch 4
9	IN ₃	Logic Control for Switch 3
10	D ₃	Drain (Output) Terminal for Switch 3
11	S ₃	Source (Input) Terminal for Switch 3
12	V _L	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S ₂	Source (Input) Terminal for Switch 2
15	D ₂	Drain (Output) Terminal for Switch 2
16	IN ₂	Logic Control for Switch 2

TRUTH TABLE

LOGIC	DG411/ 883	DG412/ 883	DG413/883	
	SWITCH	SWITCH	SWITCH 1, 4	SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

Specifications DG411/883, DG412/883, DG413/883

Absolute Maximum Ratings

V+ to V-	44V
GND to V-	25V
V _L (Note 2)	(GND -0.3V) to (V+) +0.3V
Digital Inputs, V _S , V _D (Note 2)	(V-) -2V to (V+) +2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal)	30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle)	100mA
Storage Temperature Range (A Suffix)	-65°C to +125°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance (Note 3)	θ_{JA}	θ_{JC}
CerDIP Package	75°C/W	20°C/W
Junction Temperature		+175°C
Operating Temperature (A Suffix)	-55°C to +125°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	±20V Max	Input High Voltage.	2.4V Min
Operating Temperature Range.	-55°C to +125°C	Input Rise and Fall Time.	≤20ns
Input Low Voltage.	0.8V Max		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_+ = +15V$, $V_- = -15V$, $V_I = 5V$, GND = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS		
						MIN	MAX			
Drain-to-Source ON Resistance	R _{DS(ON)}	V ₊ = +13.5V, V ₋ = -13.5V, I _S = -10mA, V _D = ±8.5V	V _{IN} = 0.8V	1, 3	+25°C, -55°C	0	35	Ω		
DG411/883				2	+125°C	0	45	Ω		
DG412/883			V _{IN} = 2.4V	1, 3	+25°C, -55°C	0	35	Ω		
				2	+125°C	0	45	Ω		
DG413/883			V _{IN} = 0.8V or 2.4V (Note 1)	1, 3	+25°C, -55°C	0	35	Ω		
				2	+125°C	0	45	Ω		
DG411/883		V ₊ = +10.8V, V ₋ = -0V, I _S = -10mA, V _D = 3.0V and 8.0V	V _{IN} = 0.8V	1, 3	+25°C, -55°C	0	80	Ω		
				2	+125°C	0	100	Ω		
DG412/883			V _{IN} = 2.4V	1, 3	+25°C, -55°C	0	80	Ω		
				2	+125°C	0	100	Ω		
DG413/883			V _{IN} = 0.8V or 2.4V (Note 1)	1, 3	+25°C, -55°C	0	80	Ω		
				2	+125°C	0	100	Ω		
Source OFF Leakage Current			I _{S(OFF)}	V ₊ = 16.5V, V ₋ = -16.5V, V _D = -15.5V, V _S = 15.5V	V _{IN} = 2.4V	1	+25°C	-0.25	+0.25	nA
DG411/883						2, 3	+125°C, -55°C	-20	+20	nA
DG412/883		V _{IN} = 0.8V			1	+25°C	-0.25	+0.25	nA	
					2, 3	+125°C, -55°C	-20	+20	nA	
DG413/883	V _{IN} = 0.8V or 2.4V (Note 1)	1			+25°C	-0.25	+0.25	nA		
		2, 3			+125°C, -55°C	-20	+20	nA		
DG411/883	V ₊ = 16.5V, V ₋ = -16.5V, V _D = 15.5V, V _S = -15.5V	V _{IN} = 2.4V		1	+25°C	-0.25	+0.25	nA		
				2, 3	+125°C, -55°C	-20	+20	nA		
DG412/883		V _{IN} = 0.8V		1	+25°C	-0.25	+0.25	nA		
				2, 3	+125°C, -55°C	-20	+20	nA		
DG413/883		V _{IN} = 0.8V or 2.4V (Note 1)		1	+25°C	-0.25	+0.25	nA		
				2, 3	+125°C, -55°C	-20	+20	nA		

Specifications DG411/883, DG412/883, DG413/883

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, $GND = 0V$, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Drain OFF Leakage Current DG411/883	I _{D(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = -15.5V, V _S = 15.5V	V _{IN} = 2.4V	1	+25°C	-0.25	+0.25	nA
DG412/883				2, 3	+125°C, -55°C	-20	+20	nA
DG413/883			V _{IN} = 0.8V	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG411/883			V _{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
DG412/883		V+ = 16.5V, V- = -16.5V, V _D = 15.5V, V _S = -15.5V	V _{IN} = 2.4V	1	+25°C	-0.25	+0.25	nA
2, 3				+125°C, -55°C	-20	+20	nA	
DG413/883			V _{IN} = 0.8V	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
			V _{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.25	+0.25	nA
				2, 3	+125°C, -55°C	-20	+20	nA
Channel ON Leakage Current DG411/883	I _{D(ON)} + I _{S(ON)}	V+ = 16.5V, V- = -16.5V, V _S = V _D = ±15.5V	V _{IN} = 0.8V	1	+25°C	-0.4	+0.4	nA
2, 3				+125°C, -55°C	-40	+40	nA	
DG412/883			V _{IN} = 2.4V	1	+25°C	-0.4	+0.4	nA
DG413/883				2, 3	+125°C, -55°C	-40	+40	nA
				V _{IN} = 0.8V or 2.4V (Note 1)	1	+25°C	-0.4	+0.4
2, 3					+125°C, -55°C	-40	+40	nA
Input Current with V _{IN} Low	I _{IL}	Input Under Test = 0.8V, All Others = 2.4V		1, 2, 3	+25°C, +125°C, -55°C	-0.5	+0.5	μA
Input Current with V _{IN} High	I _{IH}	Input Under Test = 2.4V, All Others = 0.8V		1, 2, 3	+25°C, +125°C, -55°C	-0.5	+0.5	μA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5, V _{IN} = 0V or 5.0V		1	+25°C	-	+1.0	μA
				2, 3	+125°C, -55°C	-	+5.0	μA
		V+ = 13.2V, V- = 0V, V _{IN} = 0V or 5.0V V _L = 5.25V		1	+25°C	-	+1.0	μA
				2, 3	+125°C, -55°C	-	+5.0	μA
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5, V _{IN} = 0V or 5.0V		1	+25°C	-1.0	-	μA
				2, 3	+125°C, -55°C	-5.0	-	μA
		V+ = 13.2V, V- = 0V, V _{IN} = 0V or 5.0V V _L = 5.25V		1	+25°C	-1.0	-	μA
				2, 3	+125°C, -55°C	-5.0	-	μA
Logic Supply Current	I _L	V+ = 16.5V, V- = -16.5, V _{IN} = 0V or 5.0V		1	+25°C	-	+1.0	μA
				2, 3	+125°C, -55°C	-	+5.0	μA
		V+ = 13.2V, V- = 0V, V _{IN} = 0V or 5.0V V _L = 5.25V		1	+25°C	-	+1.0	μA
				2, 3	+125°C, -55°C	-	+5.0	μA
Ground Current	I _{GND}	V+ = 16.5V, V- = -16.5, V _{IN} = 0V or 5.0V		1	+25°C	-1.0	-	μA
				2, 3	+125°C, -55°C	-5.0	-	μA
		V+ = 13.2V, V- = 0V, V _{IN} = 0V or 5.0V V _L = 5.25V		1	+25°C	-1.0	-	μA
				2, 3	+125°C, -55°C	-5.0	-	μA

Specifications DG411/883, DG412/883, DG413/883

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, $GND = 0V$, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn ON Time	t_{ON}	$C_L = 35pF$, $V_S = \pm 10V$, $R_L = 300\Omega$	9, 11	+25°C, -55°C	0	175	ns
			10	+125°C	0	240	ns
		$V_+ = 12V$, $V_- = 0V$, $C_L = 35pF$, $V_S = +8V$, $R_L = 300\Omega$	9, 11	+25°C, -55°C	0	250	ns
			10	+125°C	0	400	ns
Turn OFF Time	t_{OFF}	$C_L = 35pF$, $V_S = \pm 10V$, $R_L = 300\Omega$	9, 11	+25°C, -55°C	0	145	ns
			10	+125°C	0	160	ns
		$V_+ = 12V$, $V_- = 0V$, $C_L = 35pF$, $V_S = +8V$, $R_L = 300\Omega$	9, 11	+25°C, -55°C	0	125	ns
			10	+125°C	0	140	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Tested at: $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, $GND = 0V$, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Charge Injection	Q	See Figure 2, $V_G = 0V$, $R_G = 0\Omega$, $T_A = +25^\circ C$, $C_L = 10nF$	9	+25°C	-100	+100	pC
				+25°C			pC
		See Figure 2, $V_G = 6V$, $R_G = 0\Omega$, $T_A = +25^\circ C$ $C_L = 10nF$, $V_+ = 12V$, $V_- = 0V$	9	+25°C	-100	+100	pC
				+25°C			pC

NOTES:

1. V_{IN} = Input Voltage to Perform Proper Function.
2. Signals on S_X , D_X or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. All leads soldered or welded to PC board.
4. Parameters listed in Table 3 are controlled via design or process and are not directly tested at final production. These parameters are lab characterized upon initial design release or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

2760 μm x 1780 μm x 485 $\pm$ 25 μm

METALLIZATION:

Type: SiAl

Thickness: 12k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

GLASSIVATION:

Type: Nitride

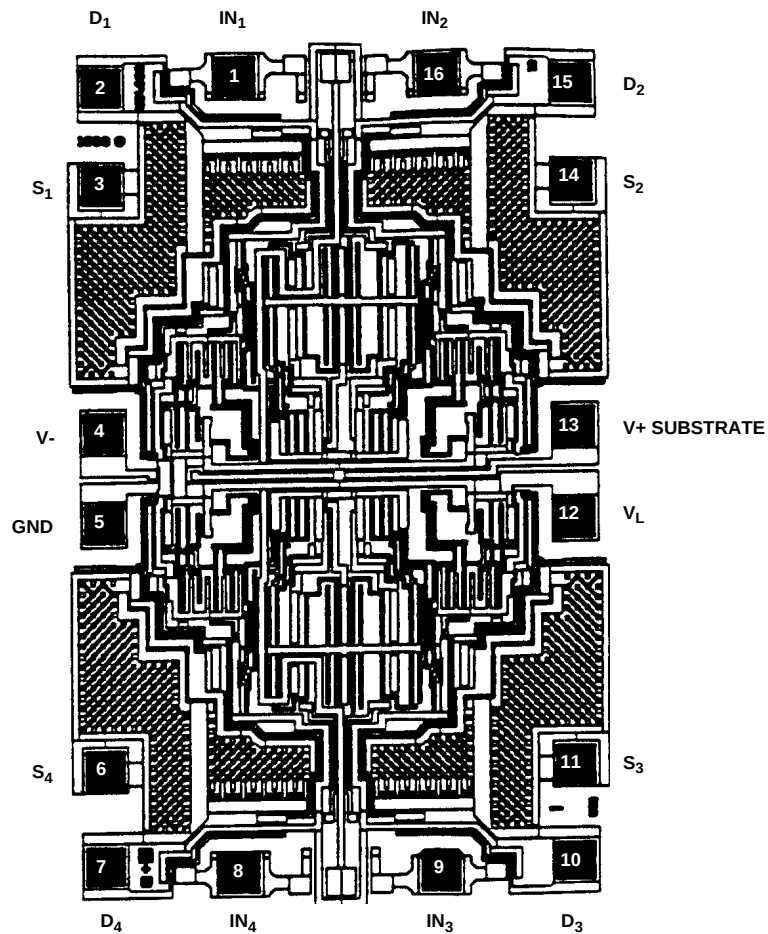
Thickness: 8k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

WORST CASE CURRENT DENSITY:

1.5 x 10⁵A/cm²

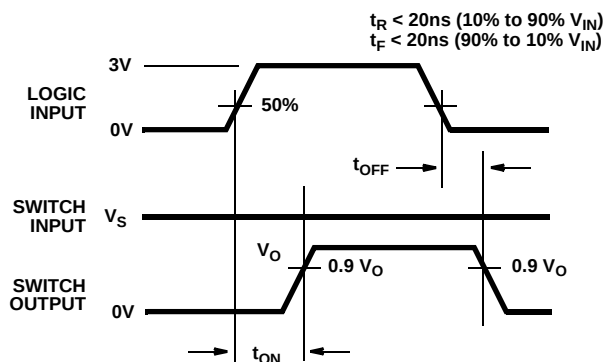
Metallization Mask Layout

DG411/883, DG412/883, DG413/883



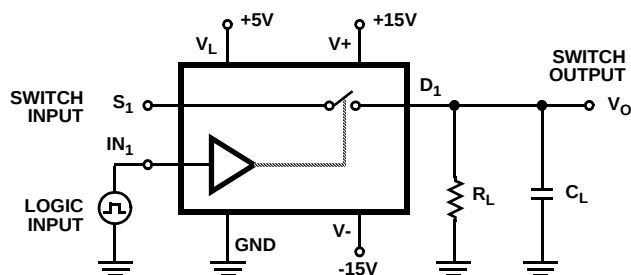
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A.



Repeat test for all IN and S .

For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

FIGURE 1B.

FIGURE 1. SWITCHING TIME

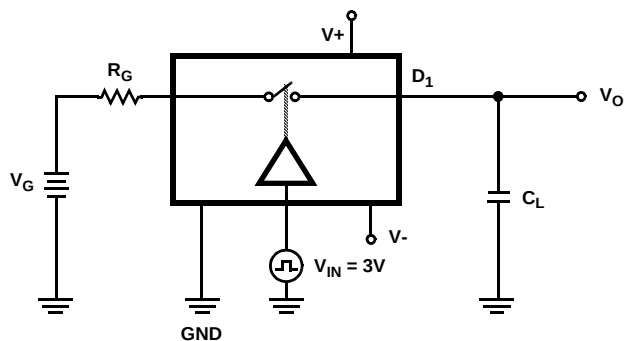
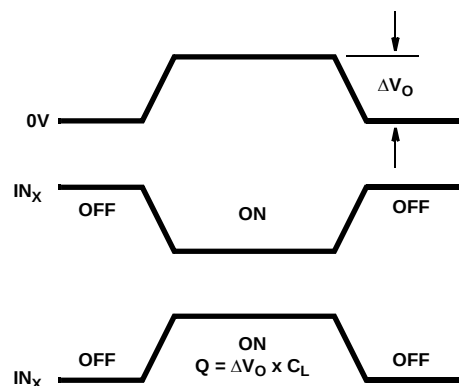


FIGURE 2A.

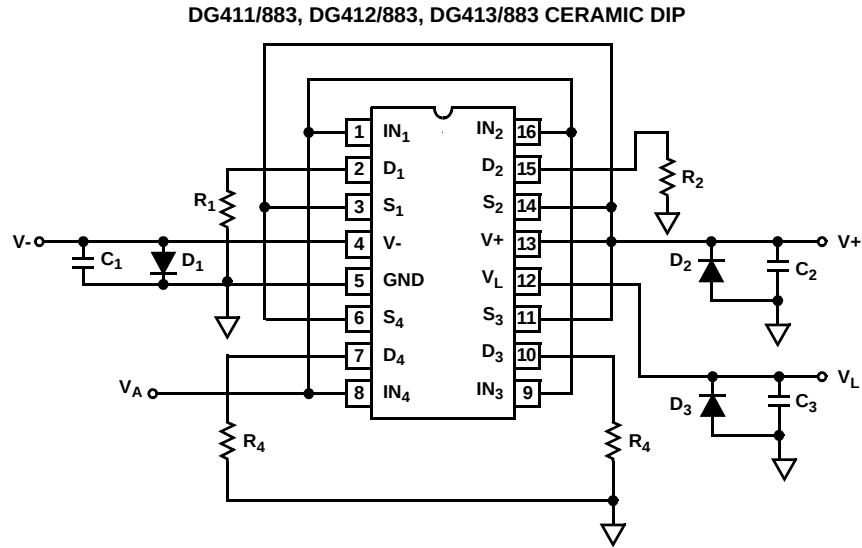


IN_X dependent on switch configuration input polarity determined by sense of switch.

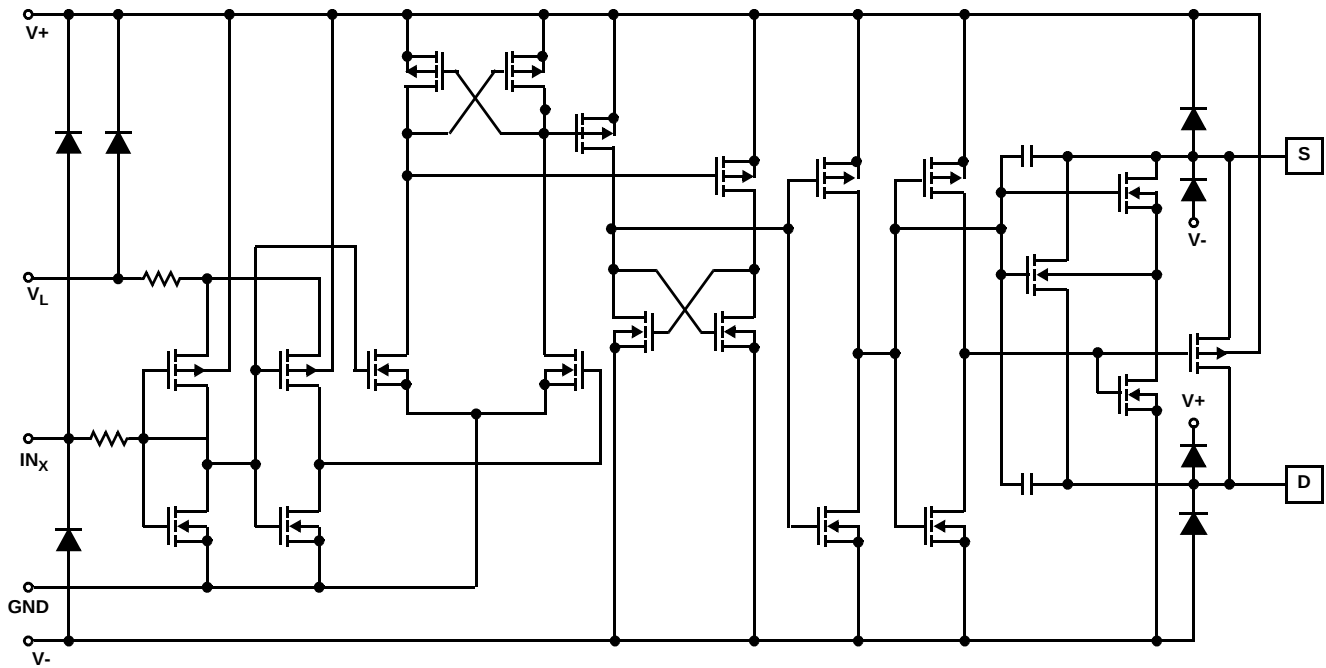
FIGURE 2B.

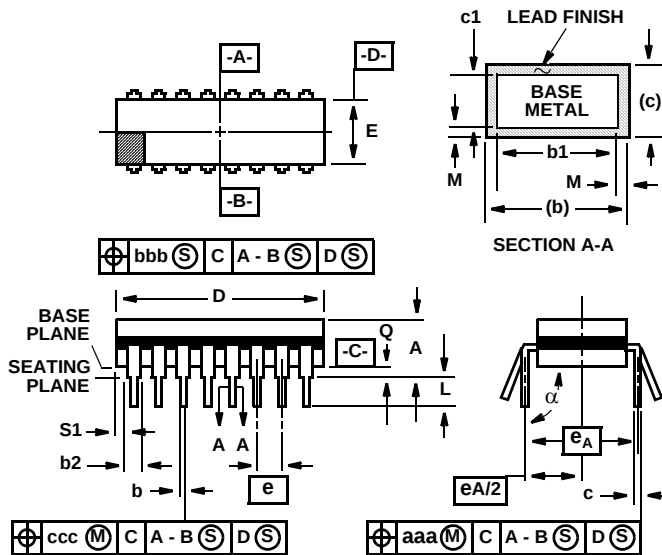
FIGURE 2. CHARGE INJECTION

Burn-In Circuit



Typical Schematic Diagram (Typical Channel)



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

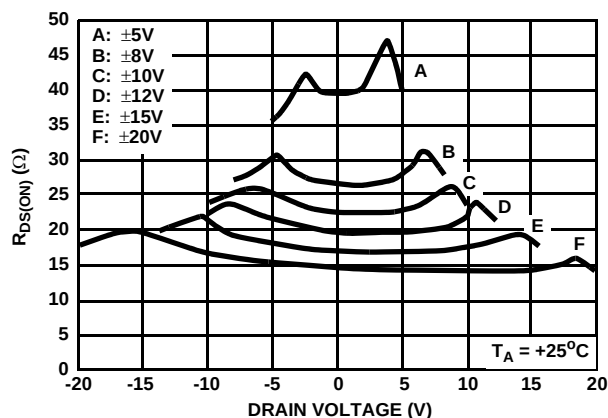
DESIGN INFORMATION

Monolithic Quad SPST CMOS Analog Switches

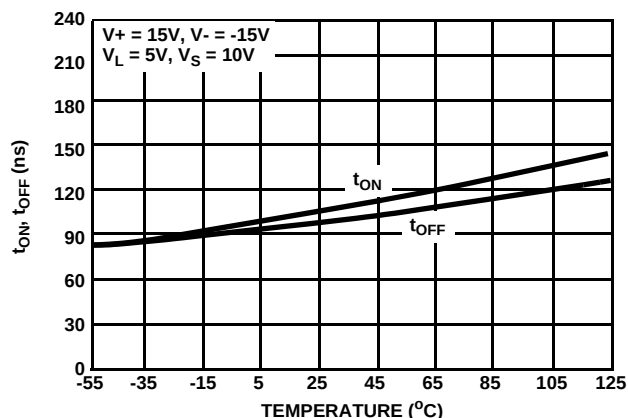
The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

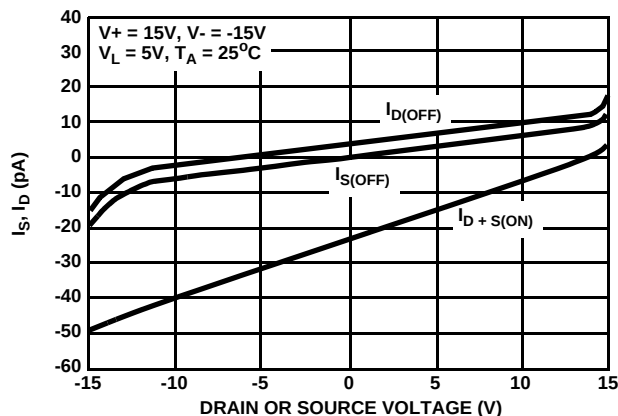
ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE



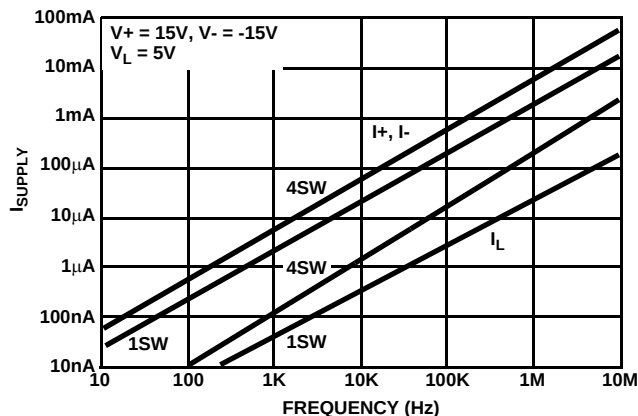
SWITCHING TIME vs TEMPERATURE



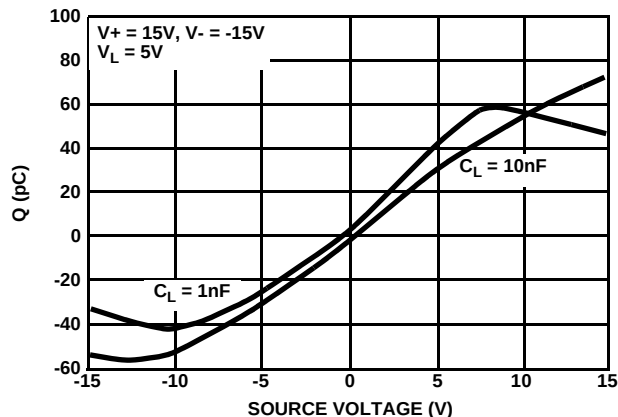
LEAKAGE CURRENT vs ANALOG VOLTAGE



SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY



CHARGE INJECTION vs ANALOG VOLTAGE (V_D)



CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

