National Semiconductor

June 1989

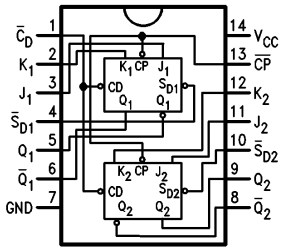
54LS114
Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

General Description

The ’LS114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

Connection Diagram

Dual-In-Line Package



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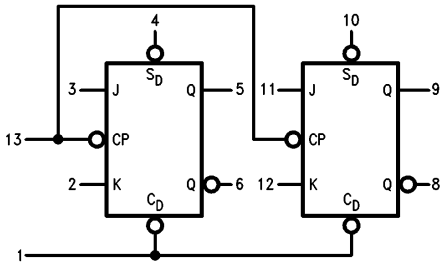
Order Number 54LS114DMQB, 54LS114FMQB or 54LS114LMQB
See NS Package Number E20A, J14A or W14B

Logic Symbol



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V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
$\overline{C}D$	Direct Clear Input (Active LOW)
$\overline{S}D1$, $\overline{S}D2$	Direct Set Inputs (Active LOW)
Q1, Q2, $\overline{Q}1$, $\overline{Q}2$	Outputs

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS114			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time Jn or Kn to $\overline{CP}$	20 20			ns
t_h (H) t_h (L)	Hold Time Jn or Kn to $\overline{CP}$	0 0			ns
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	20 15			ns
t_w	$\overline{CD}$ or $\overline{SD}$n Pulse Width	15			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.4 0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			0.1 0.3 0.6 0.8	mA mA mA mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			20 60 120 160	μA μA μA μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			−0.4 −0.8 −1.6 −1.44	mA mA mA mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{CP} = 0V			8.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2k, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		16 24	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}$ or $\overline{SD}$n to Q or $\overline{Q}$		16 24	ns

Truth Table

Inputs @ t_n		Output @ t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

Asynchronous Inputs:

LOW input to $\overline{S}$D sets Q to HIGH level

LOW input to $\overline{C}$D sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}$D and $\overline{S}$D makes both Q and $\overline{Q}$ HIGH

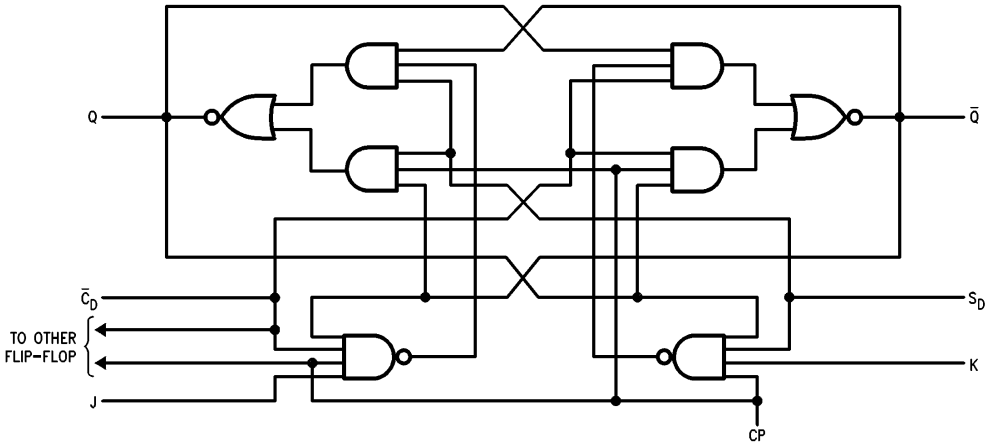
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.

Logic Diagram (one half shown)



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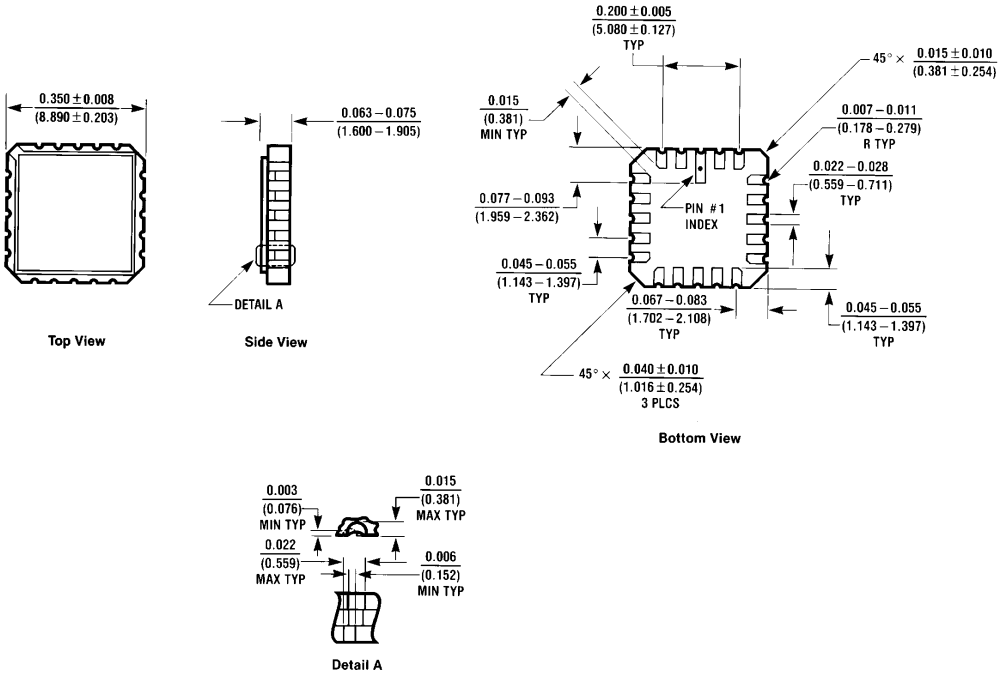
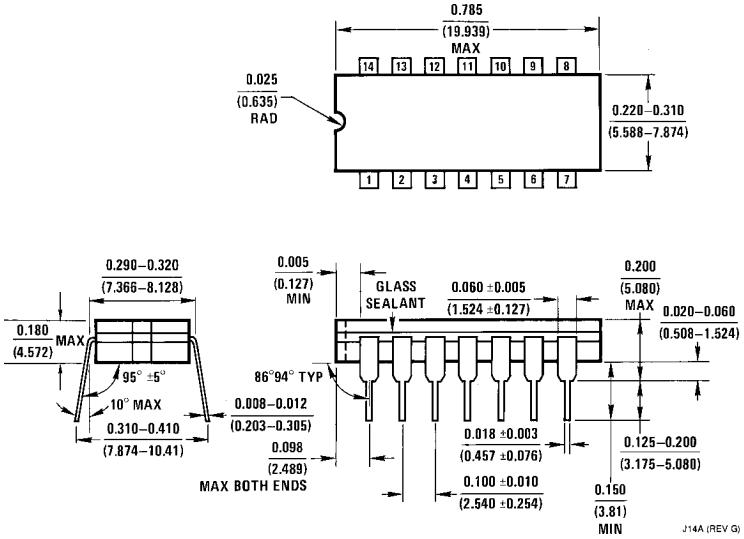
Physical Dimensions inches (millimeters)



E20A (REV D)

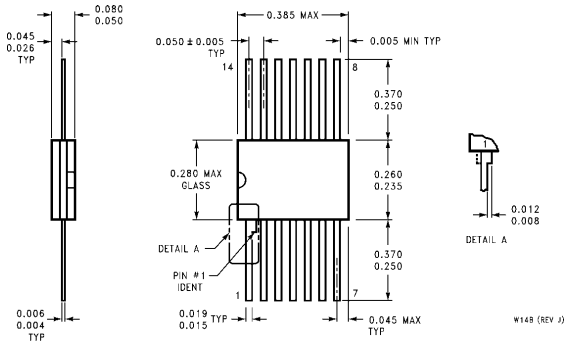
Ceramic Leadless Chip Carrier (E)
Order Number 54LS114LMQB
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS114DMQB
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS114FMQB
NS Package Number W14B

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