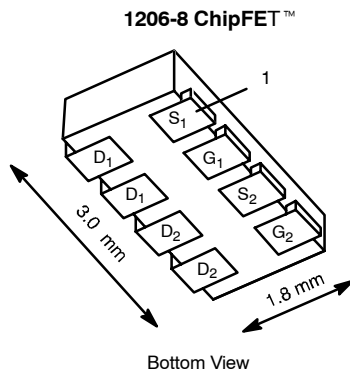




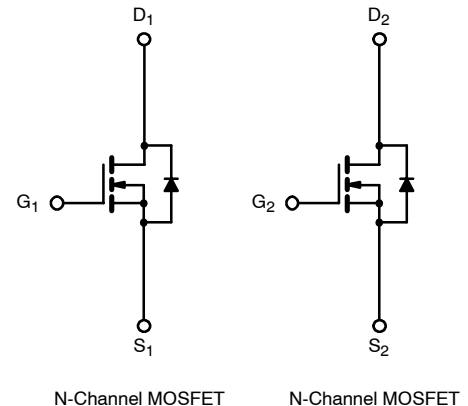
Dual N-Channel 2.5-V (G-S) MOSFET

TrenchFET®
Power MOSFETs
2.5-V Rated

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.075 @ $V_{GS} = 4.5$ V	± 4.2
	0.134 @ $V_{GS} = 2.5$ V	± 3.1



Marking Code
CB XX
Lot Traceability
and Date Code
Part # Code



N-Channel MOSFET

N-Channel MOSFET

Ordering Information: Si5904DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	5 secs	Steady State
Drain-Source Voltage		V_{DS}	20	
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	± 4.2	± 3.1
	$T_A = 85^\circ\text{C}$		± 3.0	± 2.2
Pulsed Drain Current		I_{DM}	± 10	
Continuous Source Current (Diode Conduction) ^a		I_S	1.8	0.9
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.1	1.1
	$T_A = 85^\circ\text{C}$		1.1	0.6
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	
Soldering Recommendations (Peak Temperature) ^{b, c}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	50	60	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)		R_{thJF}	30	40	

Notes

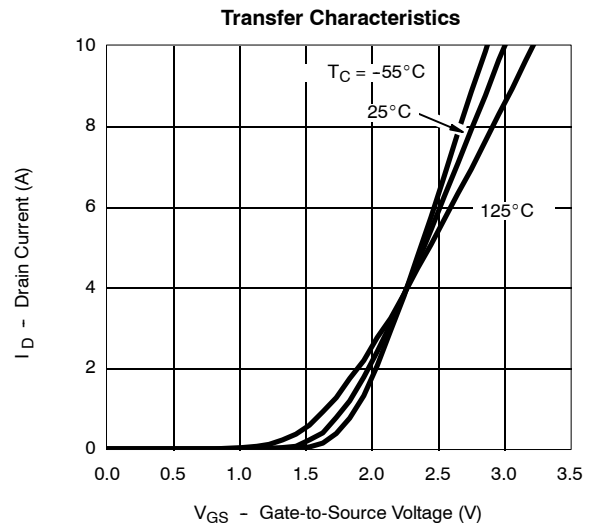
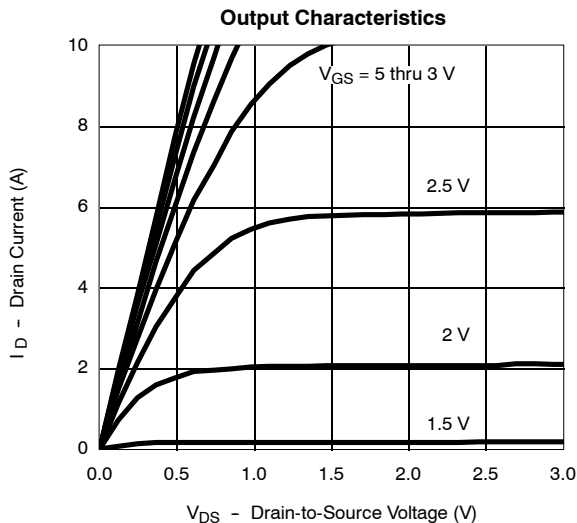
- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 16\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 3.1\ \text{A}$		0.065	0.075	Ω
		$V_{GS} = 2.5\ \text{V}$, $I_D = 2.3\ \text{A}$		0.115	0.143	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 3.1\ \text{A}$		8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 3.1\ \text{A}$		4	6	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_G = 6\ \Omega$		12	18	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			19	30	
Fall Time	t_f			9	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 0.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		40	80	

Notes

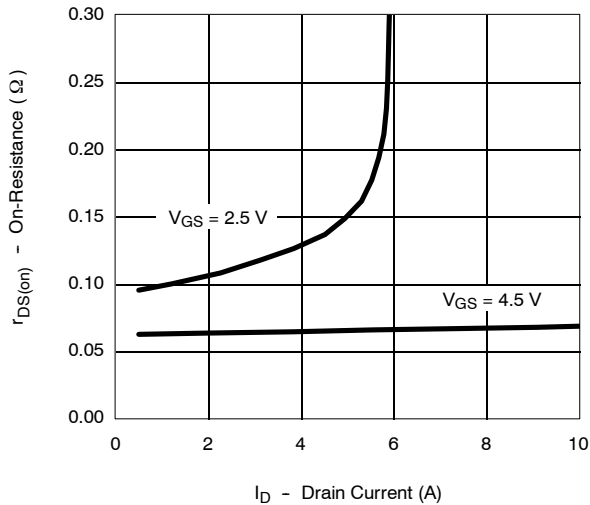
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

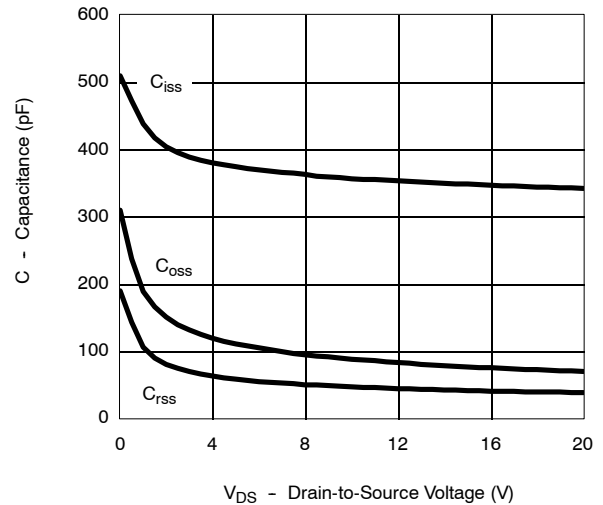


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

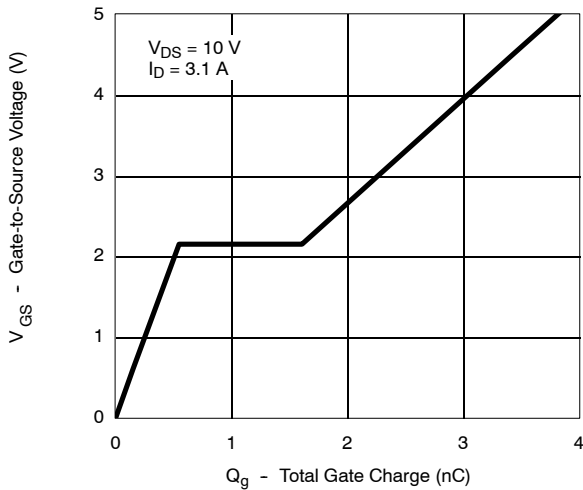
On-Resistance vs. Drain Current



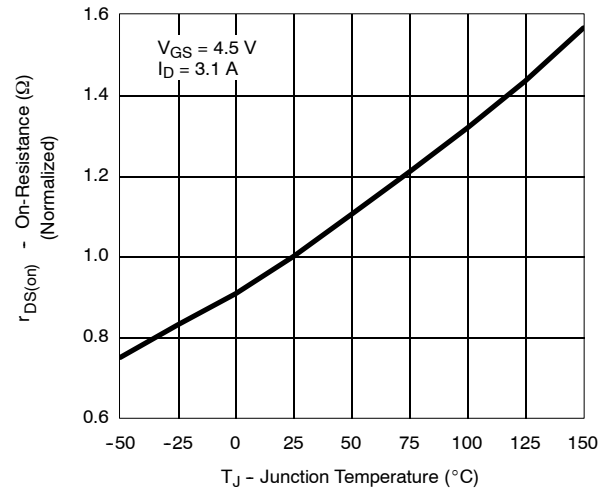
Capacitance



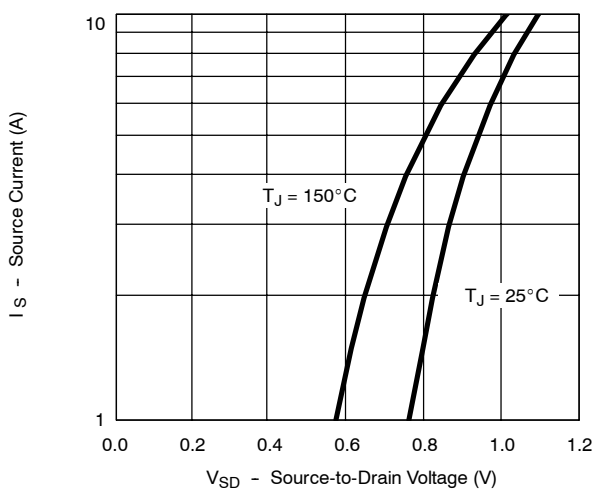
Gate Charge



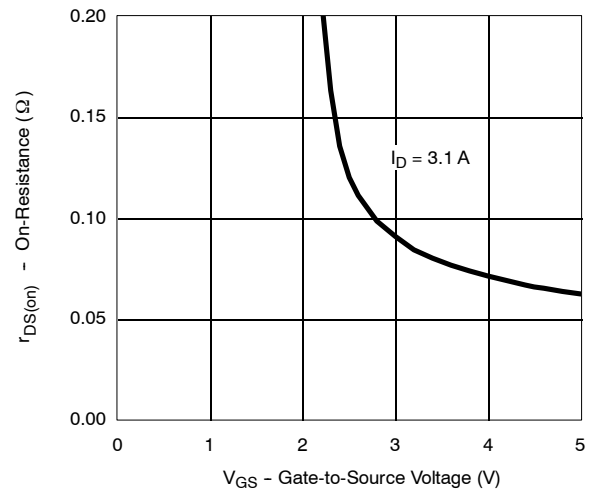
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

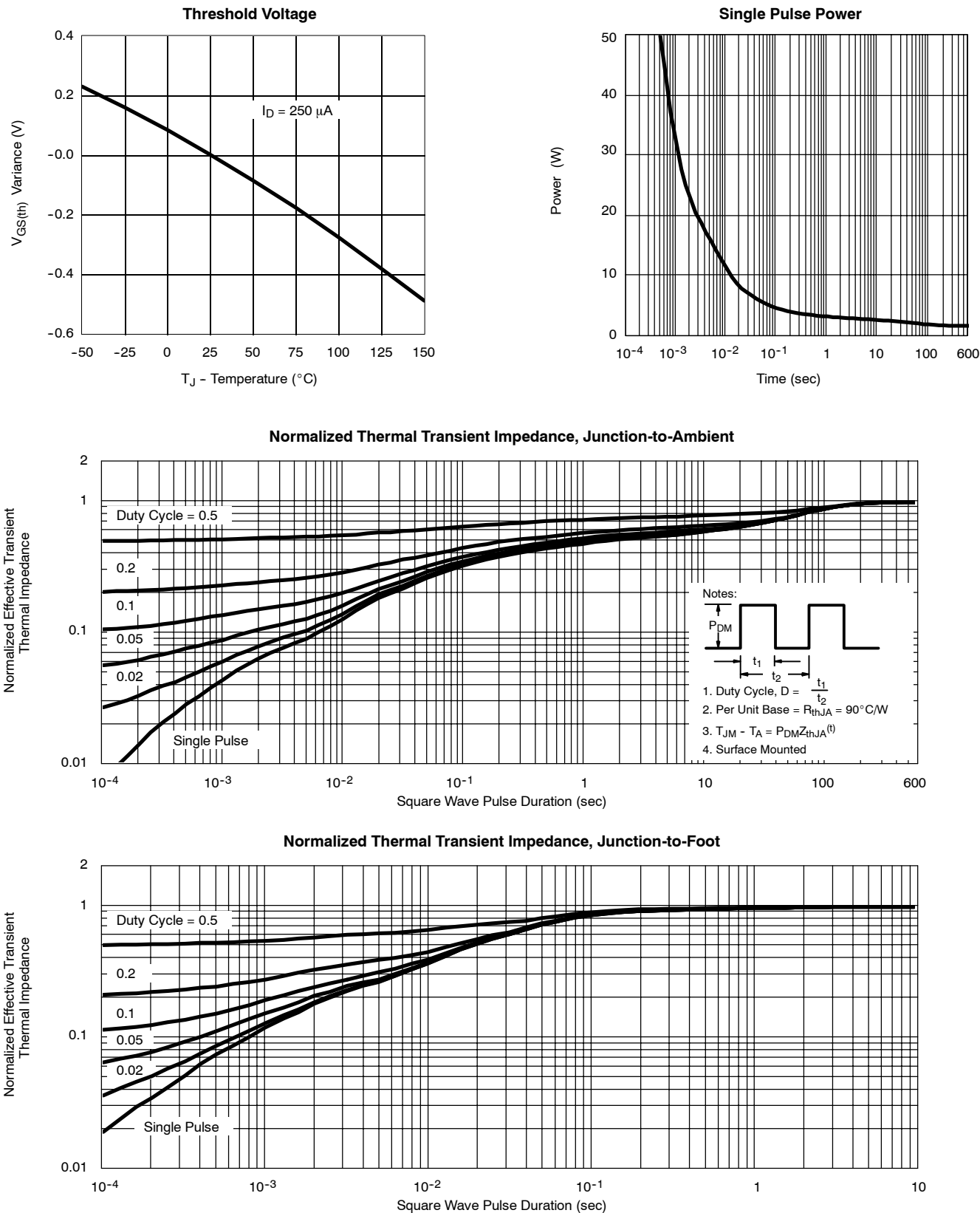


On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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