

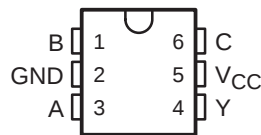
SN74AUP1T97

SINGLE-SUPPLY VOLTAGE LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

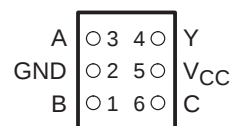
SCES613A – OCTOBER 2004 – REVISED DECEMBER 2004

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Single-Supply Voltage Translator
 - 1.8 V to 3.3 V (at $V_{CC} = 3.3$ V)
 - 2.5 V to 3.3 V (at $V_{CC} = 3.3$ V)
 - 1.8 V to 2.5 V (at $V_{CC} = 2.5$ V)
 - 3.3 V to 2.5 V (at $V_{CC} = 2.5$ V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μ A)
- 200-ns/V Input Rise/Fall Time Allows Slow Transition of Input Signal
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SOT-23 (DBV), SC-70 (DCK), WCSP (NanoFree)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Related Devices: AUP1T98/57/58

DBV OR DCK PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T97 is designed for logic level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog-mixed mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and also allow for slow input signal transition.

The AUP1T97 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection Table). Up to nine commonly used logic gate functions can be performed.

I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage will occur to the device under these conditions.

AUP1T97 is designed with optimized current drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high drive outputs.

Nanostar™ and Nanofree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SINGLE-SUPPLY VOLTAGE LEVEL TRANSLATOR

WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

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description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUP1T97YEPR	____TH_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUP1T97YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74AUP1T97DBVR	HT4_
	SOT (SC-70) – DCK	Tape and reel	SN74AUP1T97DCKR	TH_

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	5
2-input AND gate	6
2-input OR gate with one inverted input	7
2-input NAND gate with one inverted input	7
2-input AND gate with one inverted input	8
2-input NOR gate with one inverted input	8
2-input OR gate	9
Inverter	10
Noninverted buffer	11

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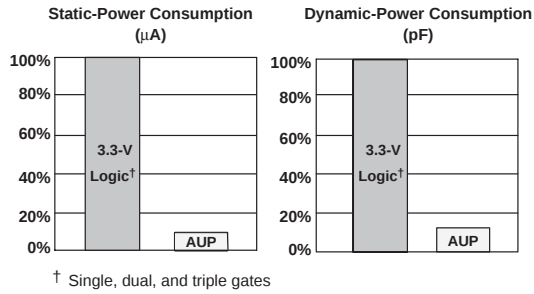


Figure 1. AUP - The Lowest-Power Family

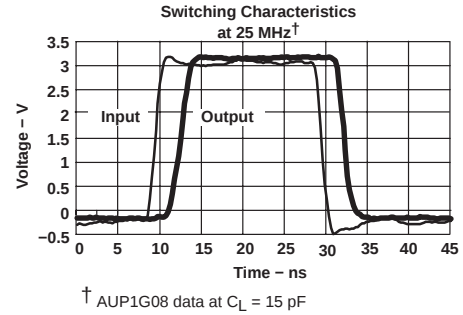


Figure 2. Excellent Signal Integrity

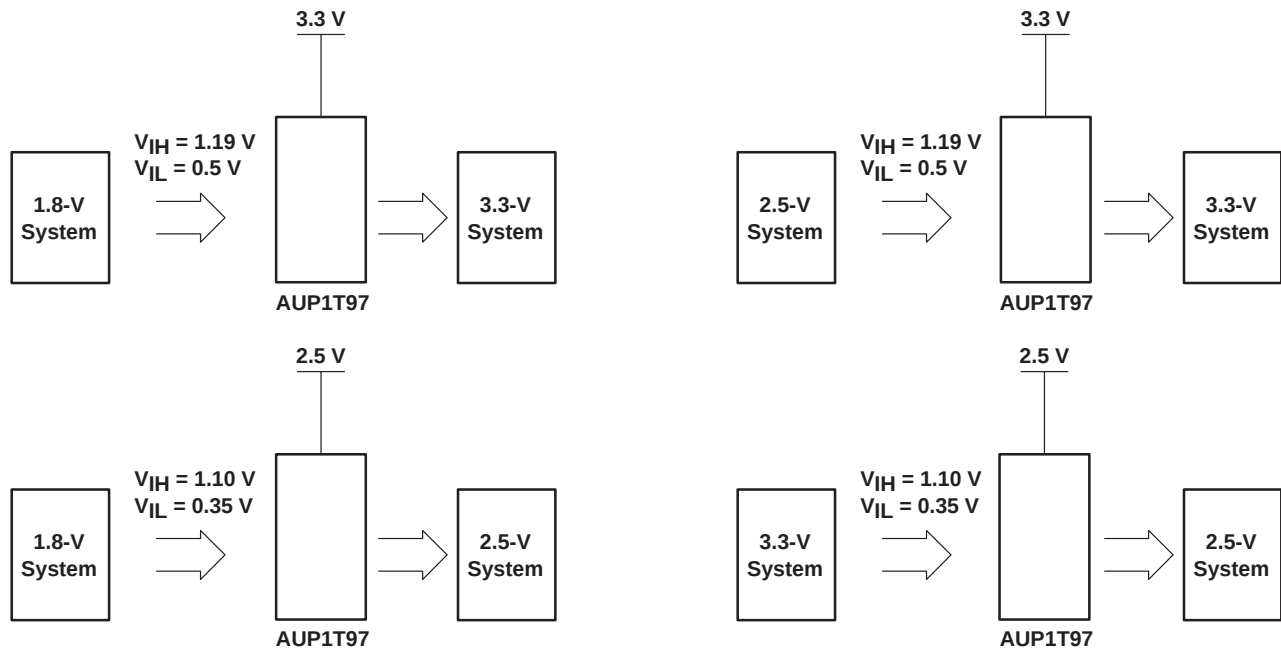


Figure 3. Possible Voltage Translation Combinations

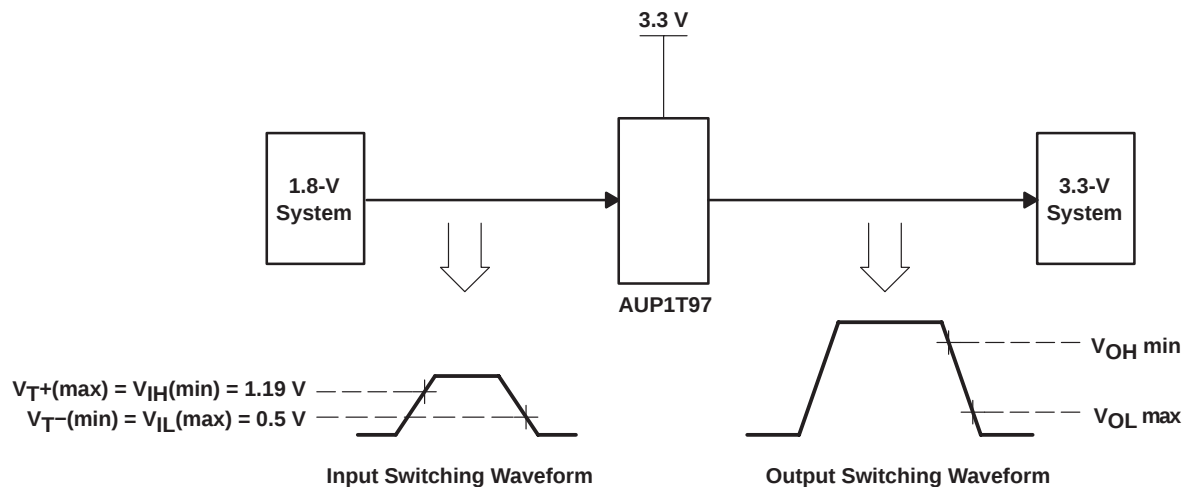


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

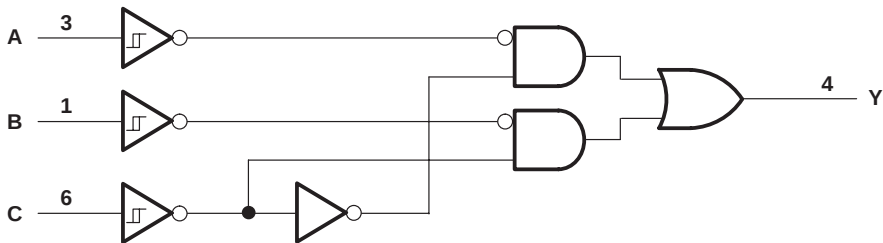
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FUNCTION TABLE

INPUTS			OUTPUT Y
C	B	A	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

logic diagram (positive logic)



logic configurations

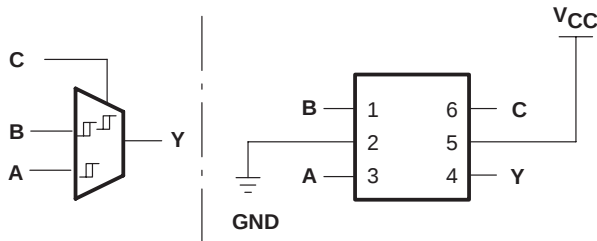


Figure 5. 157: 2-to-1 Data Selector/MUX
 When C is L, Y = B
 When C is H, Y = A

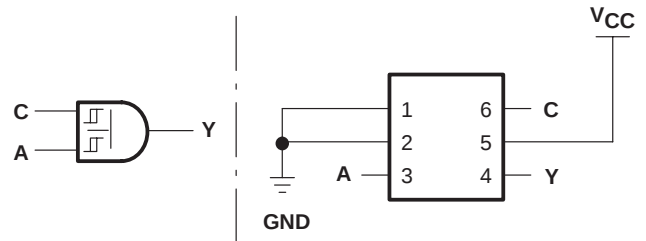


Figure 6. 08: 2-Input AND Gate

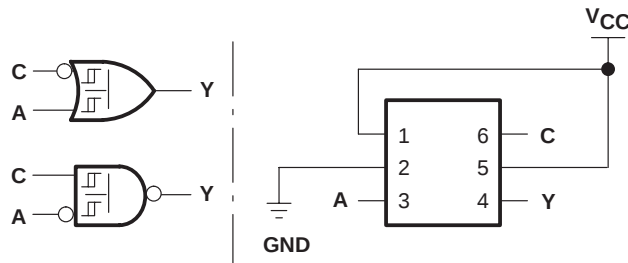


Figure 7. 14+32/14+00: 2-Input OR/NAND Gate
 With One Inverted Input

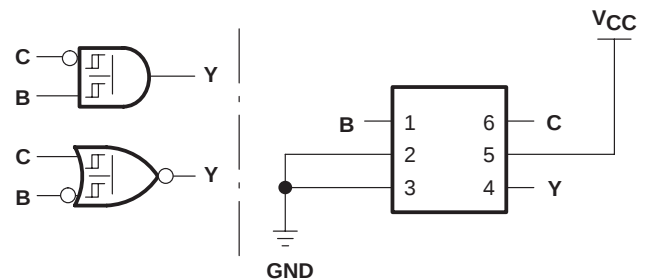


Figure 8. 14+08/14+02: 2-Input AND/NOR
 Gate With One Inverted Input

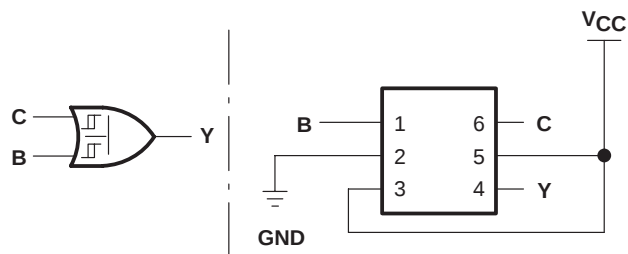


Figure 9. 32: 2-Input OR Gate

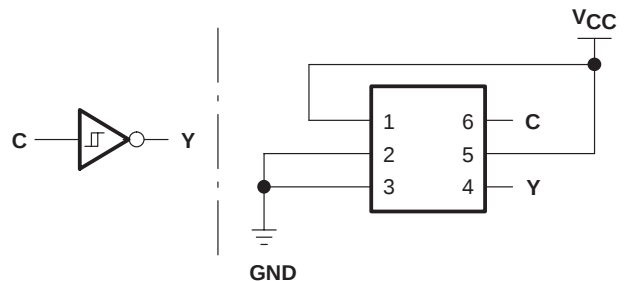


Figure 10. 04/14: Inverter

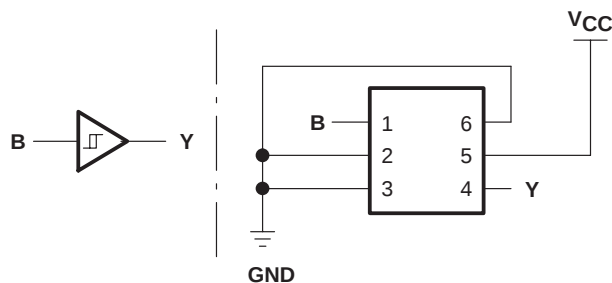


Figure 11. 17/34: Noninverted Buffer

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 4.6 V
Output voltage range in the high or low state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	–3.1	mA
		$V_{CC} = 3$ V	–4	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	3.1	mA
		$V_{CC} = 3$ V	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 3.6 V	200	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT	
				MIN	TYP	MAX	MIN	MAX		
V _{T+} Positive-going input threshold voltage			2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V	
			3 V to 3.6 V	0.75		1.16	0.75	1.19		
V _{T-} Negative-going input threshold voltage			2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V	
			3 V to 3.6 V	0.5		0.85	0.5	0.85		
ΔV _T Hysteresis (V _{T+} - V _{T-})			2.3 V to 2.7 V	0.23		0.6	0.17	0.6	V	
			3 V to 3.6 V	0.25		0.56	0.21	0.56		
V _{OH}		I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1			V _{CC} - 0.1		V	
		I _{OH} = -2.3 mA	2.3 V	2.05			1.97			
		I _{OH} = -3.1 mA		1.9			1.85			
		I _{OH} = -2.7 mA	3 V	2.72			2.67			
		I _{OH} = -4 mA		2.6			2.55			
V _{OL}		I _{OL} = 20 μA	2.3 V to 3.6 V	0.1			0.1		V	
		I _{OL} = 2.3 mA	2.3 V	0.31			0.33			
		I _{OL} = 3.1 mA		0.44			0.45			
		I _{OL} = 2.7 mA	3 V	0.31			0.33			
		I _{OL} = 4 mA		0.44			0.45			
I _I	All inputs	V _I = 3.6 V or GND	0 V to 3.6 V		0.1		0.5		μA	
I _{off}		V _I or V _O = 0 V to 3.6 V		0 V		0.1		0.5		μA
ΔI _{off}		V _I or V _O = 5.5 V		0 V to 0.2 V		0.2		0.5		μA
I _{CC}		V _I = 3.6 V or GND, I _O = 0		2.3 V to 3.6 V		0.5		0.9		μA
ΔI _{CC}		One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , I _O = 0		2.3 V to 2.7 V				4		μA
		One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , I _O = 0		3 V to 3.6 V				12		
C _i		V _I = V _{CC} or GND		3.3 V		1.5				pF
C _O		V _O = V _{CC} or GND		3.3 V		3				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_I = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

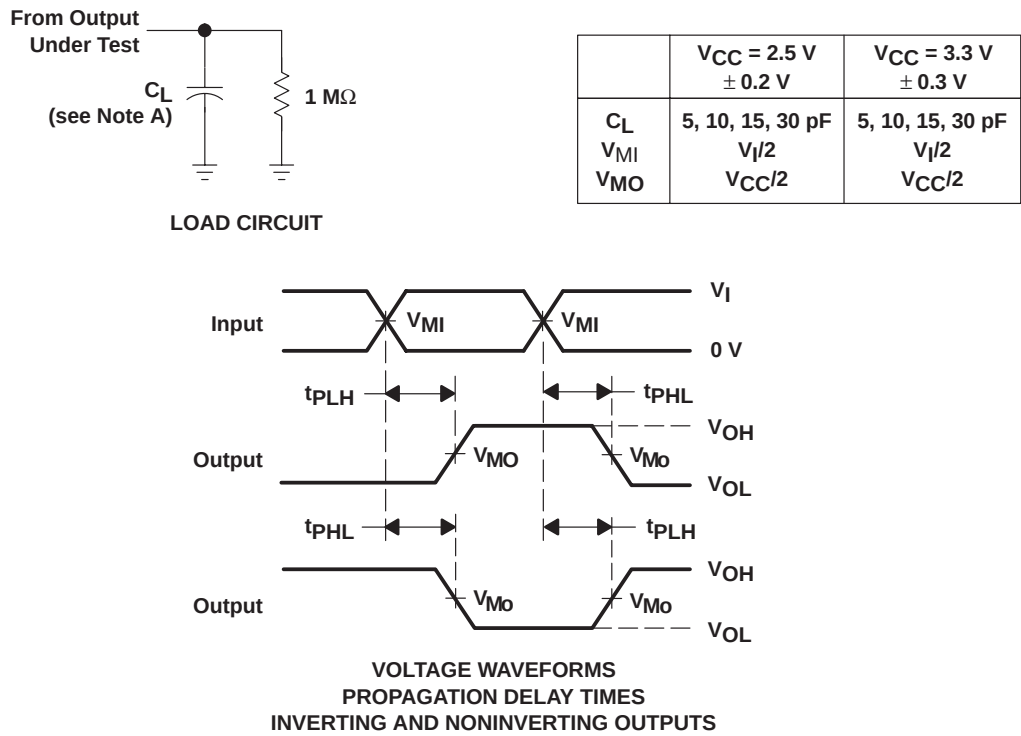
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

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PARAMETER MEASUREMENT INFORMATION

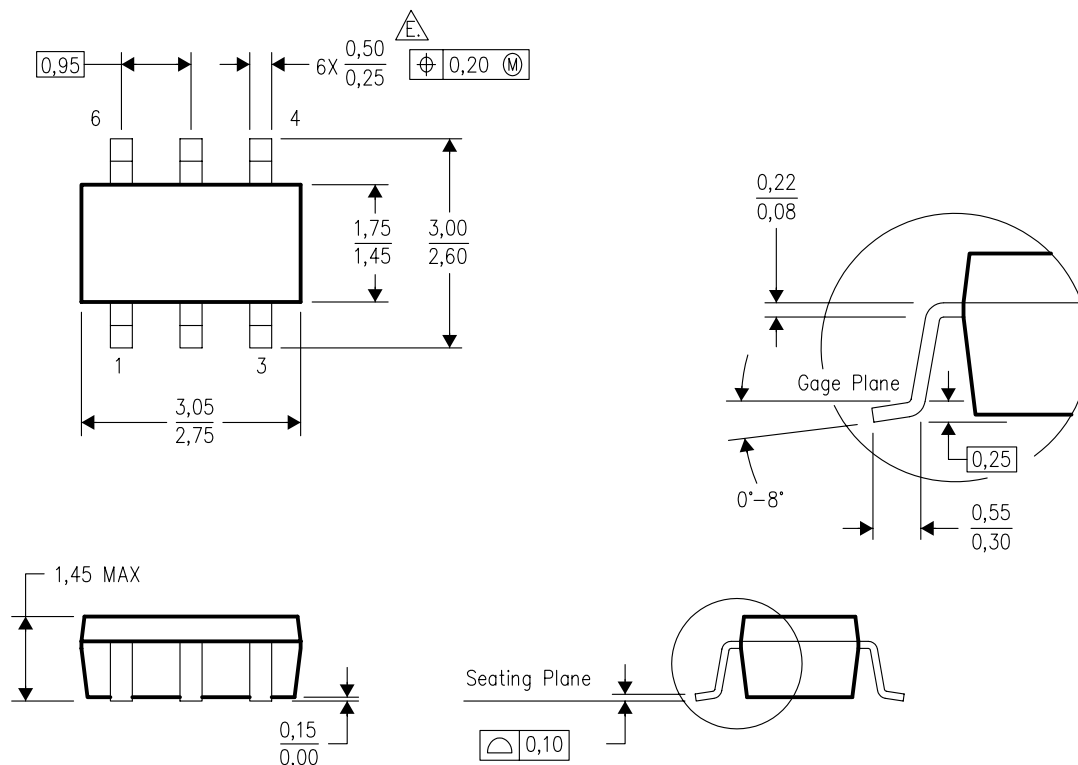


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, slew rate $\geq 1\text{ V/ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 12. Load Circuit and Voltage Waveforms

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

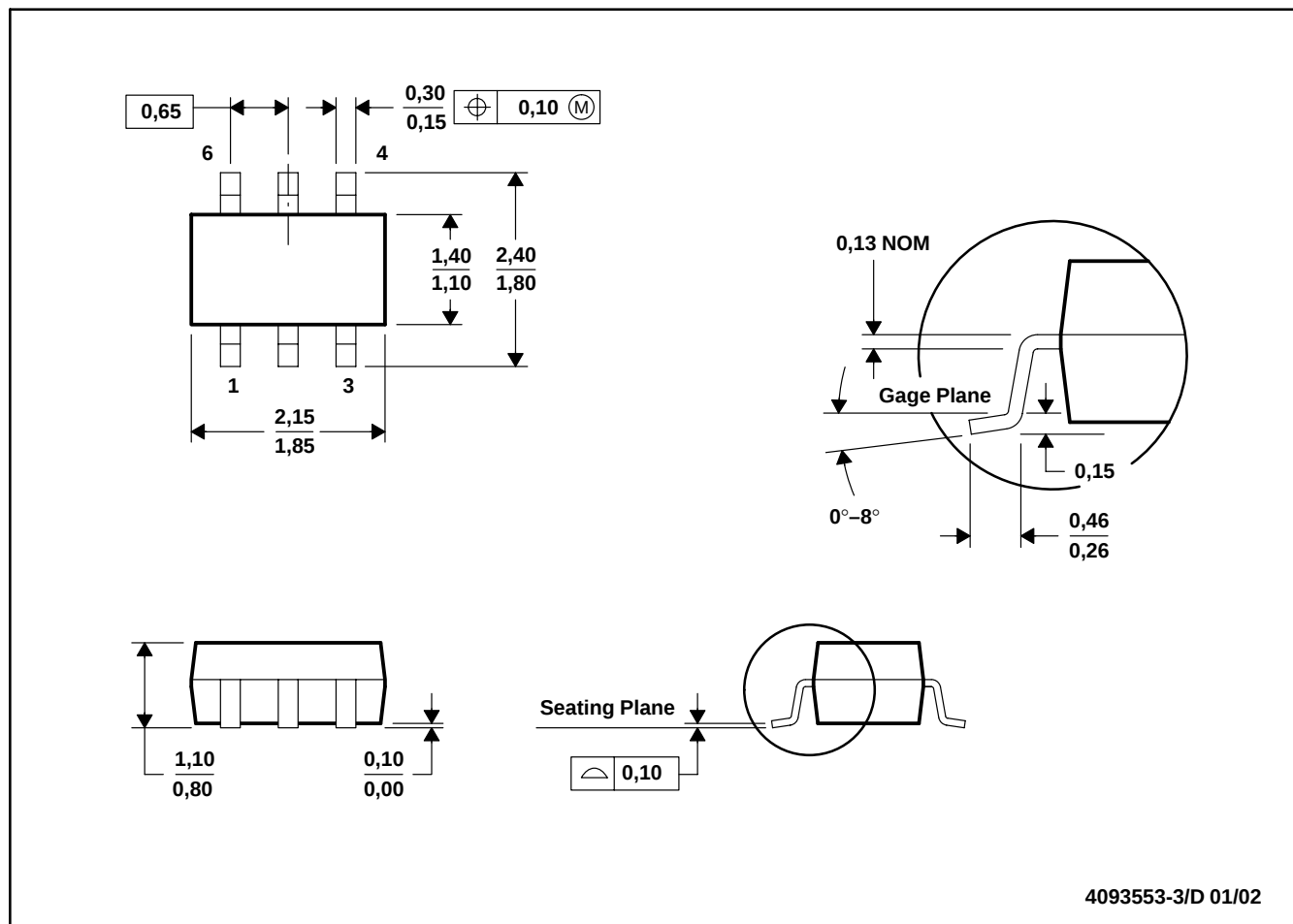


4073253-5/1 04/2005

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
-  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DCK (R-PDSO-G6)

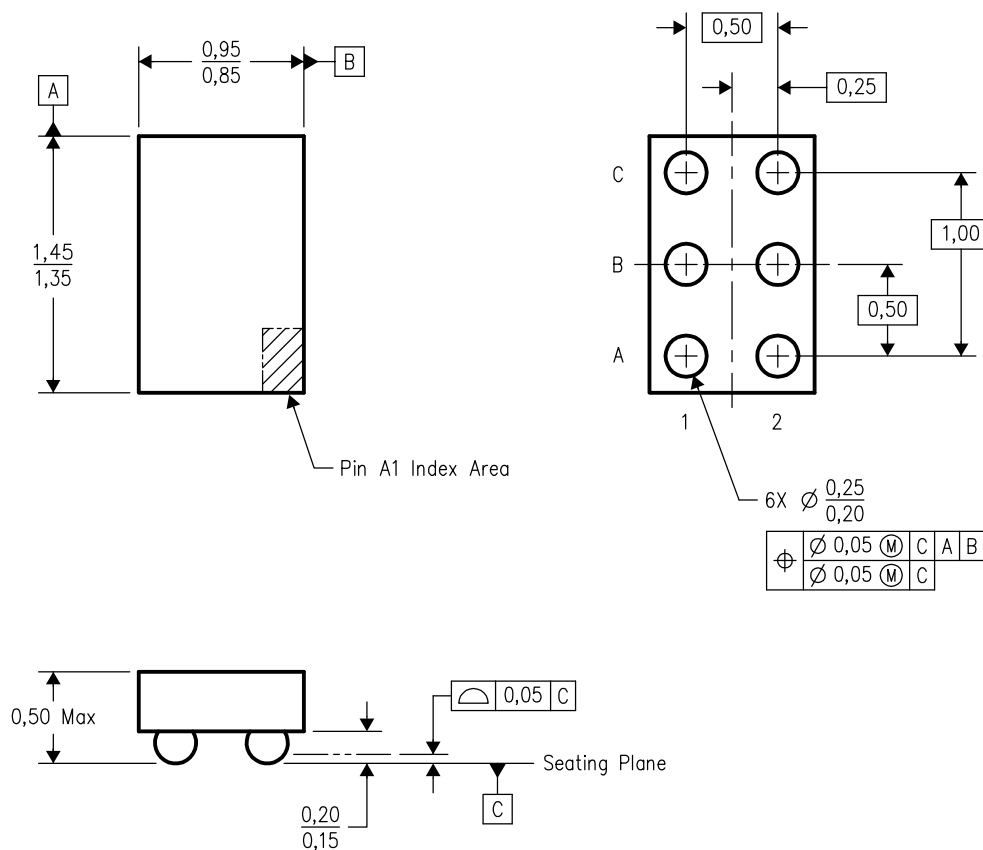
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-203

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



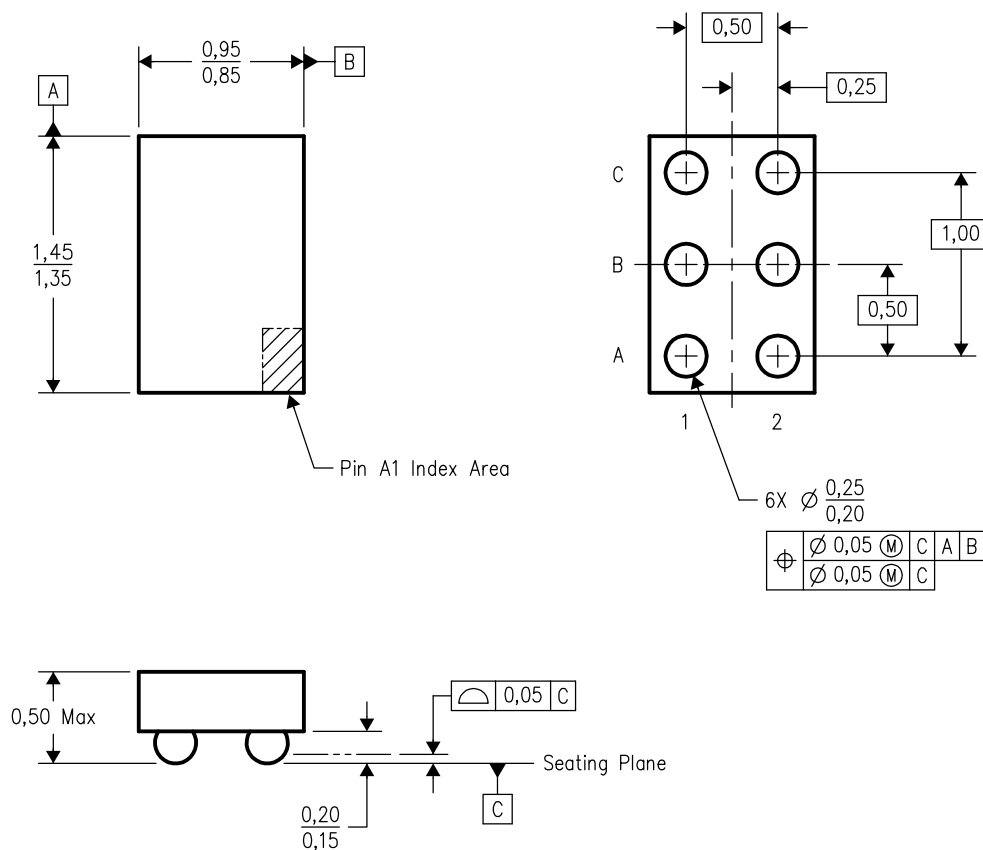
4204741-3/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204725-3/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead-free.

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