High Current Quad Output Regulator for TFT LCD Panels

September 2003

FEATURES

- **4 Integrated Switches: 2.4A Buck, 2.6A Boost, 0.35A Boost, 0.35A Inverter (Guaranteed Minimum Current Limit)**
- **Fixed Frequency, Low Noise Outputs**
- **Soft Start for all Outputs**
- **Externally Programmable V_{ON} Delay**
- Integrated Schottky Diode for V_{ON} Output
- PGOOD Pin for AV_{DD} Output Disconnect
- 4.5V to 22V Input Voltage Range
- PanelProtect™ Circuitry Disables V_{ON} Upon Fault
- Thermally Enhanced 28-Lead TSSOP

APPLICATIONS

- Large TFT-LCD Desktop Monitor Displays
- Flat Panel Televisions

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PannelProtect is a trademark of Linear Technology Corporation.

DESCRIPTION

The LT®1943 quad output adjustable switching regulator provides power for large TFT LCD panels. The device, housed in a low profile 28 pin thermally enhanced TSSOP package, can generate a 3.3V or 5V logic supply along with the triple output supply required for the TFT LCD panel. Operating from an input range of 4.5V to 22V, a step-down regulator provides a low voltage output V_{LOGIC} with up to 2A current. A high-power step-up converter, a lower-power step-up converter and an inverting converter provide the three independent output voltages AV_{DD}, V_{ON} and V_{OFF} required by the LCD panel. A high-side PNP provides delayed turn-on of the V_{ON} signal and can handle up to 30mA. Protection circuitry ensures V_{ON} is disabled if any of the four outputs are more than 10% below normal voltage.

All switchers are synchronized to the internal 1.2MHz clock, allowing the use of low profile inductors and ceramic capacitors throughout. A current mode architecture provides excellent transient response. For best flexibility, all outputs are adjustable. Soft-start is included in all four channels. A PGOOD pin can drive an optional PMOS pass device to provide output disconnect for the AV_{DD} output.

TYPICAL APPLICATION

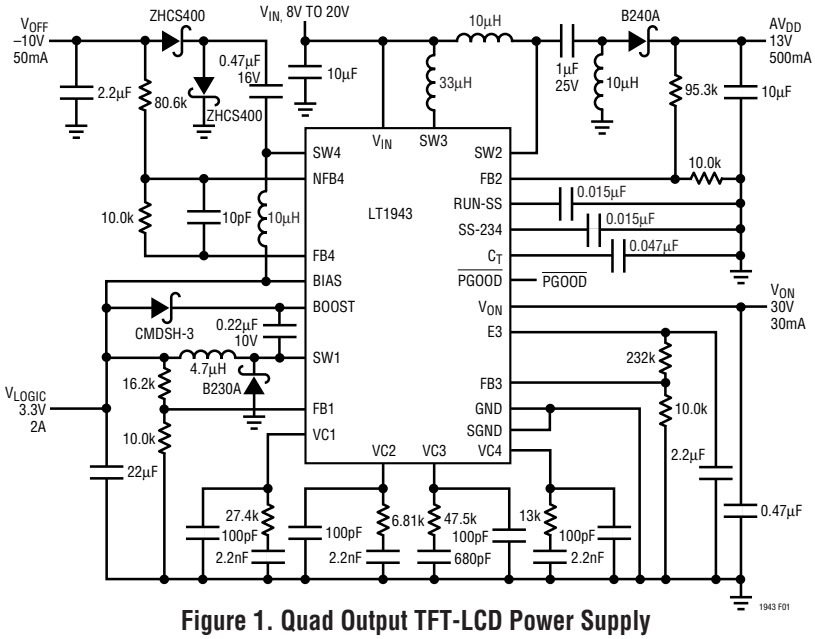
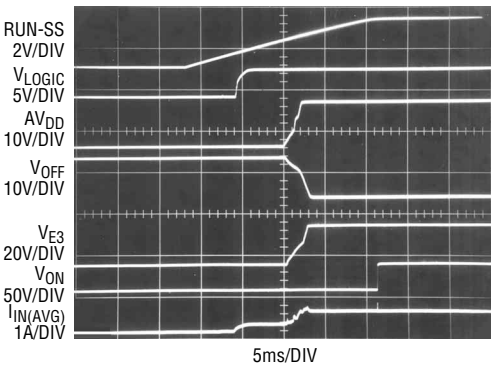


Figure 1. Quad Output TFT-LCD Power Supply

Startup Waveforms

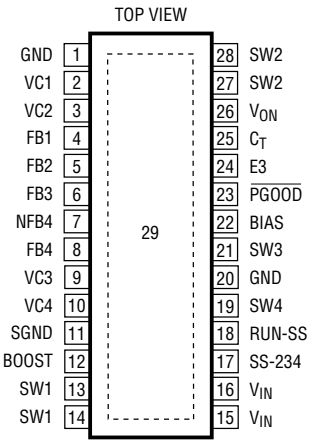


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 25V
BOOST Voltage 36V
BOOST Voltage Above SW1 ..... 25V
BIAS Pin Voltage 18V
SW2, SW4 Pin Voltages 40V
SW3 Voltage 36V
FB1, FB2, FB3, FB4 Voltages 4V
NFB4 Voltage ..... +6V, –0.6V
VC1, VC2, VC3, VC4 Pin Voltages 6V
RUN-SS, SS-234 Pin Voltages 6V
PGOOD Pin Voltage 36V
E3 Pin Voltage 36V
V_{ON} Voltage 36V
C_T Pin Voltage 6V
Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 29) IS GROUND
(MUST BE SOLDERED TO PCB)

T_{JMAX} = 150°C, θ_{JA} = 25°C/W, θ_{JC} = 7.5°C/W

ORDER PART NUMBER
LT1943EFE
FE PART MARKING
1943EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			4.5	V
Maximum Input Voltage					22	V
Quiescent Current	Not Switching RUN-SS = SS-234 = 0V			10 35	14 45	mA µA
RUN-SS, SS-234 Pin Current	RUN-SS, SS-234 = 0.4V			1.7		µA
RUN-SS, SS-234 Threshold				0.8		V
BIAS Pin Voltage to Begin SS-234 Charge		●	2.4	2.8	3.15	V
BIAS Pin Current	BIAS = 3.1V, All Switches Off			10.5	15	mA
FB Threshold Offset to Begin C_T Charge	(Note 3)		90	125	160	mV
C_T Pin Current Source	All FB Pins = 1.5V		16	20	25	µA
C_T Threshold to Power V_{ON}	All FB Pins = 1.5V		1.0	1.1	1.2	V
V_{ON} Switch Drop	V_{ON} Current = 30mA			180	240	mV
Maximum V_{ON} Current	V_{E3} = 30V	●	30	60		mA
PGOOD Threshold Offset			90	125	160	mV
PGOOD Pin Leakage	V_{PGOOD} = 36V				1	µA
Master Oscillator Frequency		 ●	1.1 1.0	1.2	1.35 1.46	MHz MHz
Foldback Switching Frequency	All FB Pins = 0V			250		kHz
Frequency Shift Threshold on FB	Δ200kHz			0.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH 1 (2.4A BUCK)						
FB1 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB1 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB1 Pin Bias Current	(Note 4)	●		100	600	nA
Error Amplifier 1 Voltage Gain				200		V/V
Error Amplifier 1 Transconductance	ΔI = 5μA			450		μmhos
Switch 1 Current Limit	Duty Cycle = 35%	●	2.4	3.2	4.3	A
Switch 1 V_{CESAT}	I_{SW} = 2A			310	470	mV
Switch 1 Leakage Current	FB1 = 1.5V			0.1	10	μA
Minimum BOOST Voltage Above SW1 Pin	I_{SW} = 1.5A			1.8	2.5	V
BOOST Pin Current	I_{SW} = 1.5A			30	50	mA
Maximum Duty Cycle (SW1)		●	82	92		%
SWITCH 2 (2.6A BOOST)						
FB2 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB2 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB2 Pin Bias Current	(Note 4)	●		220	1000	nA
Error Amplifier 2 Voltage Gain				200		V/V
Error Amplifier 2 Transconductance	ΔI = 5μA			450		μmhos
Switch 2 Current Limit		●	2.6	3.8	4.9	A
Switch 2 V_{CESAT}	I_{SW2} = 2A			360	540	mV
Switch 2 Leakage Current	FB2 = 1.5V			0.1	1	μA
BIAS Pin Current	I_{SW2} = 2A			45		mA
Maximum Duty Cycle (SW2)		●	85	92		%
SWITCH 3 (350mA BOOST)						
FB3 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB3 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB3 Pin Bias Current	(Note 4)	●		100	600	nA
Error Amplifier 3 Voltage Gain				200		V/V
Error Amplifier 3 Transconductance	ΔI = 5μA			450		μmhos
Switch 3 Current Limit		●	0.35	0.5	0.7	A
Switch 3 V_{CESAT}	I_{SW3} = 0.2A			180	280	mV
Switch 3 Leakage Current	FB3 = 1.5V			0.1	1	μA
BIAS Pin Current	I_{SW3} = 0.2A			14		mA
Maximum Duty Cycle (SW3)		 ●	84 83	88		% %
Schottky Diode Drop	I = 170mA			700		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH 4 (350mA INVERTER)						
FB4 Voltage			1.23	1.25	1.27	V
		●	1.22		1.27	V
FB4 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB4 Pin Bias Current	(Note 4)	●		100	600	nA
NFB4 Voltage (V_{FB4}-V_{NFB4})			1.215	1.245	1.275	V
		●	1.205		1.275	V
NFB4 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
NFB4 Pin Bias Current	(Note 5)			100	600	nA
Error Amplifier 4 Voltage Gain				200		V/V
Error Amplifier 4 Transconductance	ΔI = 5μA			450		μmhos
Switch 4 Current Limit		●	0.35	0.5	0.7	A
Switch 4 V_{CESAT}	I_{SW4} = 0.3A			260	390	mV
Switch 4 Leakage Current				0.1	1	μA
BIAS Pin Current due to SW4	I_{SW4} = 0.3A			15		mA
Maximum Duty Cycle (SW4)			84	88		%
		●	83			%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1943E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization, and correlation with statistical process controls.

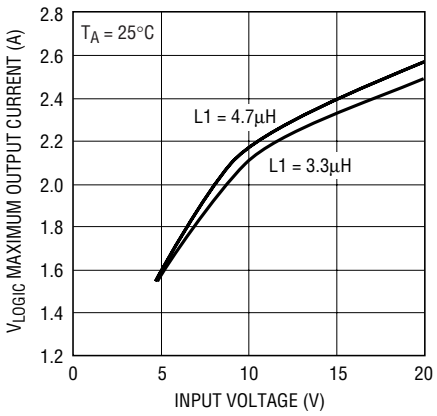
Note 3: The C_T pin is held low until FB1, FB2, FB3 and FB4 all ramp above the FB threshold offset.

Note 4: Current flows into FB1, FB2, FB3 and FB4 pins.

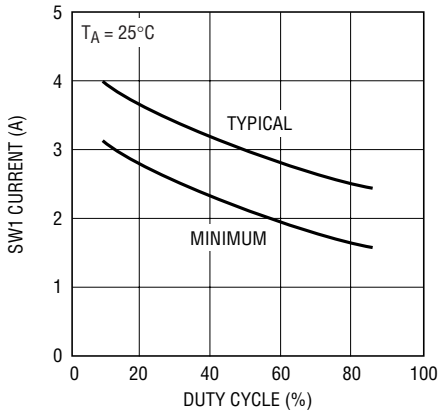
Note 5: Current flows out of NFB4 pin.

TYPICAL PERFORMANCE CHARACTERISTICS

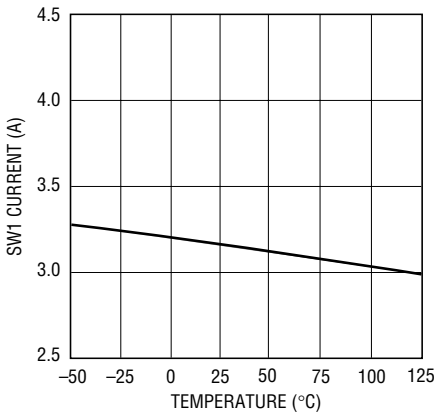
Maximum Output Current for V_{LOGIC}



SW1 Current Limit vs Duty Cycle

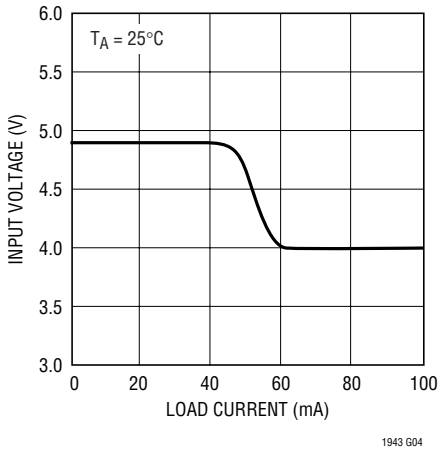


SW1 Current Limit

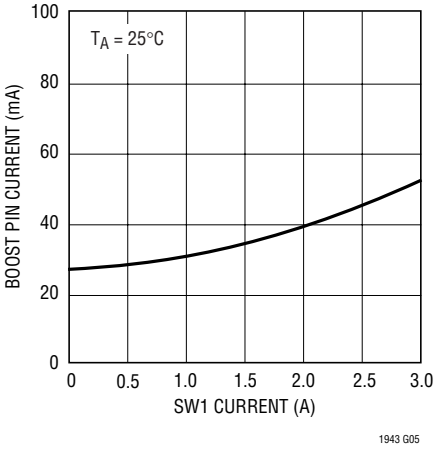


TYPICAL PERFORMANCE CHARACTERISTICS

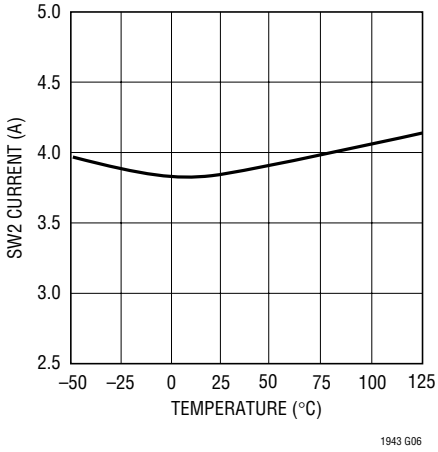
MINIMUM Input Voltage to Start, V_{OUT} = 3.3V



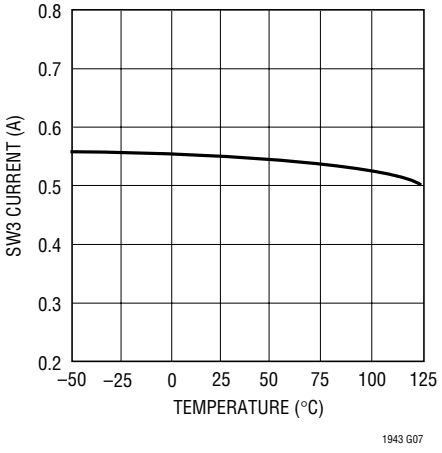
BOOST Pin Current



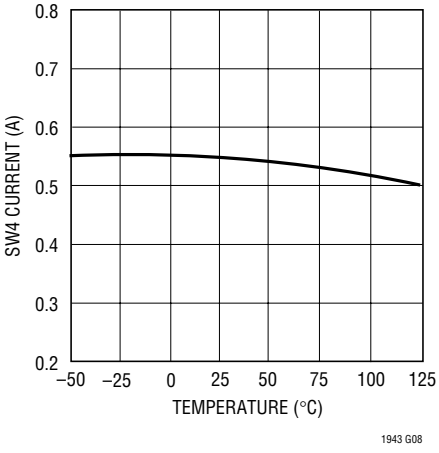
SW2 Current Limit



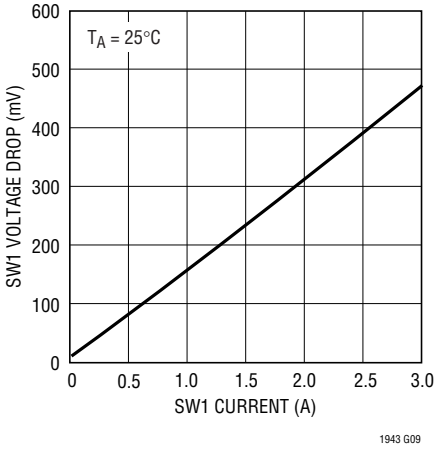
SW3 Current Limit



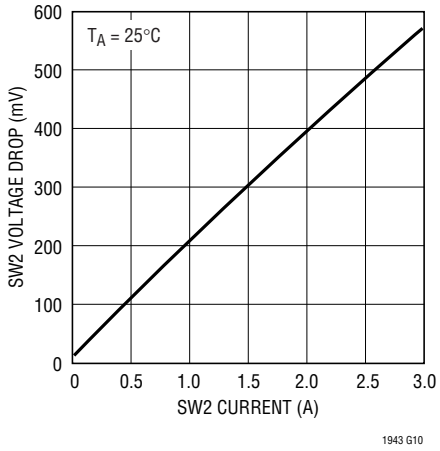
SW4 Current Limit



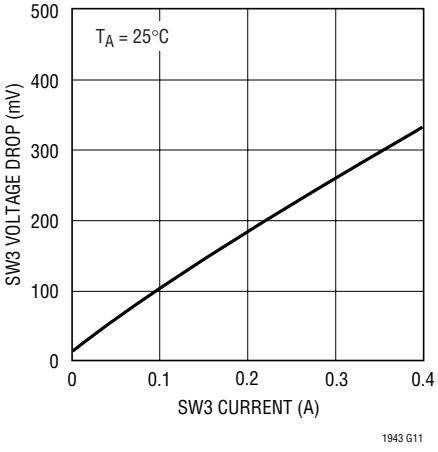
SW1 V_{CESAT}



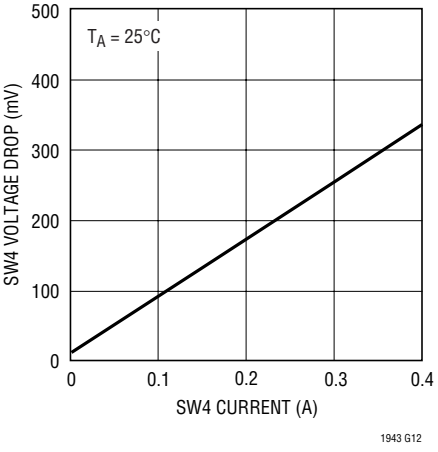
SW2 V_{CESAT}



SW3 V_{CESAT}

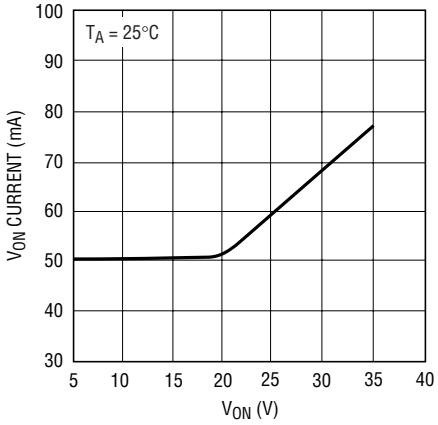


SW4 V_{CESAT}



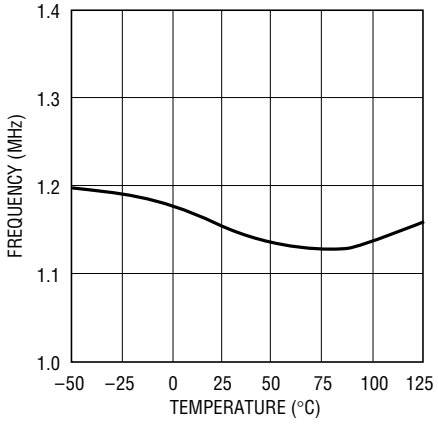
TYPICAL PERFORMANCE CHARACTERISTICS

V_{ON} Current Limit



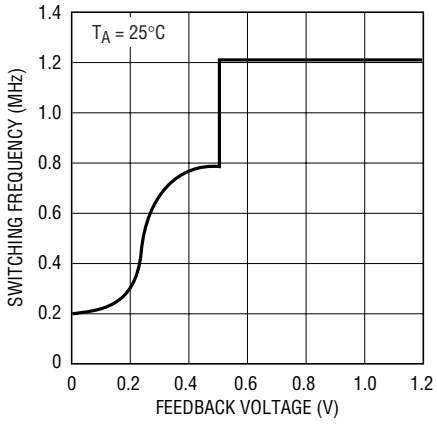
1943 G13

Oscillator Frequency



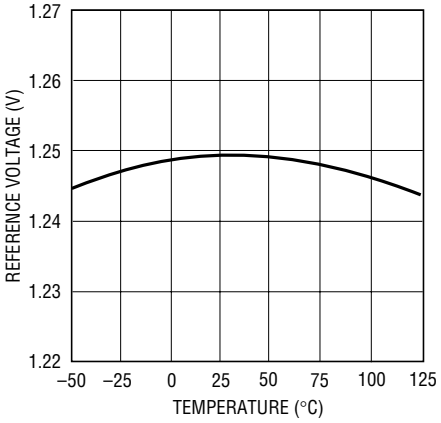
1943 G14

Frequency Foldback



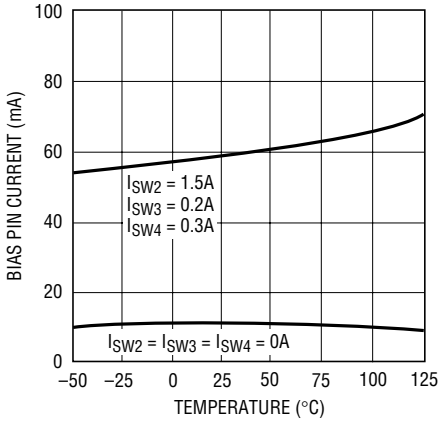
1943 G14

Reference Voltage



1943 G16

Bias Pin Current



1943 G17

PIN FUNCTIONS

GND (Pins 1, 20, Exposed Pad Pin 29): Ground. Tie both GND pins and the exposed pad directly to local ground plane. The ground metal to the exposed pad should be as wide as possible for better heat dissipation. Multiple vias (to ground plane under the ground backplane) placed close to the exposed pad can further aid in reducing thermal resistance.

VC1 (Pin 2): Switching Regulator 1 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

VC2 (Pin 3): Error Amplifier Compensation for Switcher 2. Connect a resistor/capacitor network in series with this pin.

FB1 (Pin 4): Switching Regulator 1 Feedback. Tie the resistor divider tap to this pin and set V_{LOGIC} according to $V_{LOGIC} = 1.25 \bullet (1 + R2/R1)$. Reference designators refer to Figure 2.

FB2 (Pin 5): Feedback for Switch 2. Tie the resistor divider tap to this pin and set AV_{DD} according to $AV_{DD} = 1.25 \bullet (1 + R6/R5)$.

FB3 (Pin 6): Switching Regulator 3 Feedback. Tie the resistor divider tap to this pin and set V_{ON} according to $V_{ON} = 1.25 \bullet (1 + R9/R8) – 150mV$.

NFB4 (Pin 7): Switching Regulator 4 Negative Feedback. Switcher 4 can be used to generate a positive or negative output. When regulating a negative output, tie the resistor divider tap to this pin. Negative output voltage can be set by the equation $V_{OFF} = –1.25 \bullet (R3/R4)$ with R4 set to 10k. Tie the NFB4 pin to FB4 for positive output voltages.

FB4 (Pin 8): Feedback for Switch 4. When generating a positive voltage from switch 4, tie the resistor divider tap to this pin. When generating a negative voltage, tie a 10k resistor between FB4 and NFB4 (R4).

VC3 (Pin 9): Switching Regulator 3 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

VC4 (Pin 10): Switching Regulator 4 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

SGND (Pin 11): Signal Ground. Return ground trace from the FB resistor networks and V_C pin compensation components directly to this pin and then tie to ground.

BOOST (Pin 12): The BOOST pin is used to provide a drive voltage, higher than V_{IN}, to the switch 1 drive circuit.

SW1 (Pins 13, 14): The SW1 pins are the emitter of the internal NPN bipolar power transistor for switching regulator 1. These pins must be tied together for proper operation. Connect these pins to the inductor, catch diode and boost capacitor.

V_{IN} (Pins 15, 16): The V_{IN} pins supply current to the LT1943's internal regulator and to the internal power transistor for switch 1. These pins must be tied together and locally bypassed.

SS-234 (Pin 17): This is the soft-start pin for switching regulators 2, 3 and 4. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When the BIAS pin reaches 2.8V, a 1.7μA current source begins charging the capacitor. When the capacitor voltage reaches 0.8V, switches 2, 3 and 4 turn on and begin switching. For slower start-up, use a larger capacitor. When this pin is pulled to ground, switches 2, 3 and 4 are disabled. For complete shutdown, tie RUN-SS to ground.

RUN-SS (Pin 18): This is the soft-start pin for switching regulator 1. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When power is applied to the V_{IN} pin, a 1.7μA current source charges the capacitor. When the voltage at this pin reaches 0.8V, switch 1 turns on and begins switching. For slower start-up, use a larger capacitor. For complete shutdown, tie RUN-SS to ground.

SW4 (Pin 19): This is the collector of the internal NPN bipolar power transistor for switching regulator 4. Minimize metal trace area at this pin to keep EMI down.

PIN FUNCTIONS

SW3 (Pin 21): This is the collector of the internal NPN bipolar power transistor for switching regulator 3. Minimize metal trace area at this pin to keep EMI down.

BIAS (Pin 22): The BIAS pin is used to improve efficiency when operating at higher input voltages. Connecting this pin to the output of switching regulator 1 forces most of the internal circuitry to draw its operating current from V_{LOGIC} rather than V_{IN}. Switches 2, 3 and 4 drivers are supplied by BIAS and will not switch until this pin reaches approximately 2.8V. BIAS must be tied to V_{LOGIC}.

$\overline{\text{PGOOD}}$ (Pin 23): Power Good Comparator Output. This is the open collector output of the power good comparator and can be used in conjunction with an external P-Channel MOSFET to provide output disconnect for AV_{DD}. When switcher 2's output reaches approximately 90% of its programmed voltage, $\overline{\text{PGOOD}}$ will be pulled to ground. This will pull down on the gate of the MOSFET, connecting AV_{DD}. A 100k pull-up resistor between the source and drain of the P-channel MOSFET keeps it off when switcher 2's output is low.

E3 (Pin 24): This is switching regulator 3's output and the emitter of the output disconnect PNP. Tie the output capacitor and resistor divider here.

C_T (Pin 25): Timing Capacitor Pin. This is the input to the V_{ON} timer and programs the time delay from all four feedback pins reaching 1.125V to V_{ON} turning on. The C_T capacitor value can be set using the equation $C = (20\mu A \bullet t_{DELAY})/1.1V$.

V_{ON} (Pin 26): This is the delayed output for switching regulator 3. V_{ON} reaches its programmed voltage after the internal C_T timer times out. Protection circuitry ensures V_{ON} is disabled if any of the four outputs are more than 10% below normal voltage.

SW2 (Pins 27, 28): The SW2 pins are the collector of the internal NPN bipolar power transistor for switching regulator 2. These pins must be tied together. Minimize trace area at these pins to keep EMI down.

BLOCK DIAGRAM

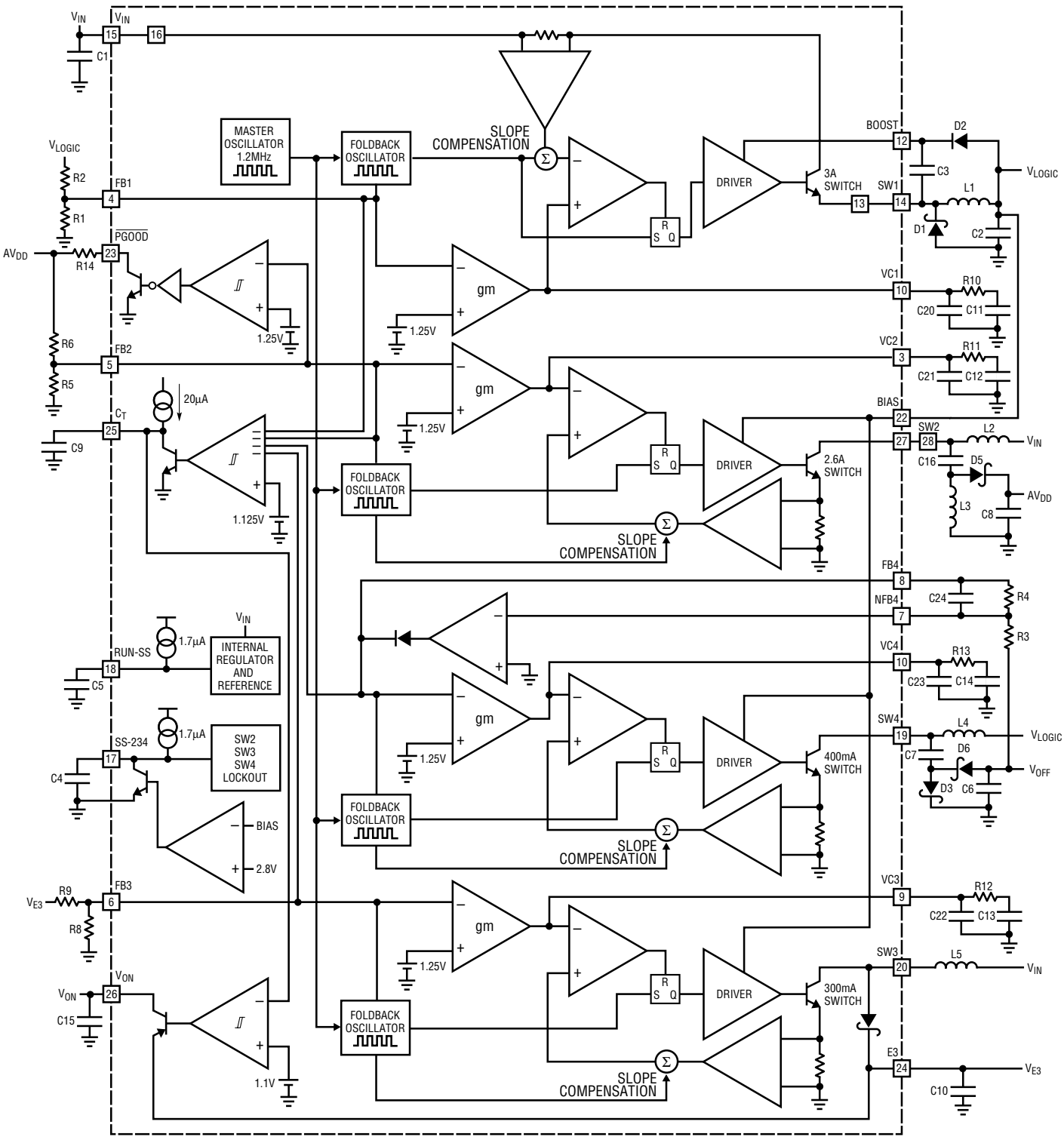


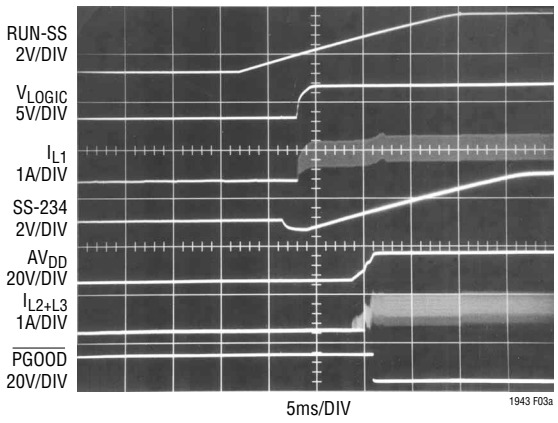
Figure 2.

OPERATION

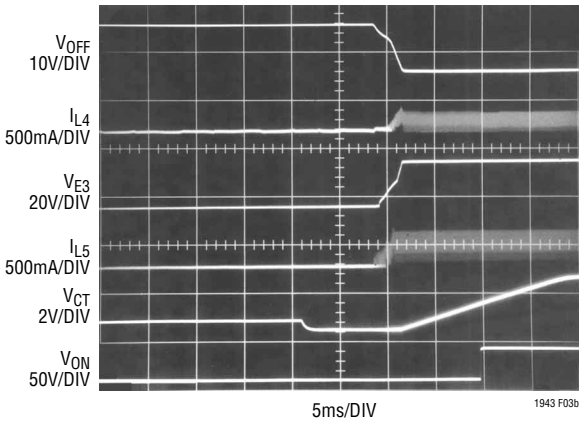
The LT1943 is a highly integrated power supply IC containing four separate switching regulators. All four switchers have their own oscillator with frequency foldback and use current mode control. Switching regulator 1 consists of a step-down regulator with a current limit of 2.4A. Switching regulator 2 is a boost regulator with a current limit of 2.6A and switchers 3 and 4 are 0.35A boost regulators. Switching regulator 4 has two feedback pins (FB4 and NFB4) and can directly regulate positive or negative output voltages.

When power is applied to V_{IN}, the RUN-SS pin starts charging and when its voltage reaches 0.8V, switcher 1 is enabled. (See Figure 2) The RUN-SS pin is used for soft-start and limits the ramp-rate for V_{LOGIC}. Using a larger capacitor at the RUN-SS pin will cause V_{LOGIC} to start more slowly. Switching regulators 2, 3 and 4 are driven by the BIAS pin which must be connected to V_{LOGIC}. V_{LOGIC} is the first to come up and when it reaches 2.8V, the SS-234 pin will begin charging to enable switches 2, 3 and 4. AV_{DD} and V_{OFF} will then begin rising and their ramp rate is determined by the capacitor tied to the SS-234 pin. When AV_{DD} reaches approximately 90% of its programmed voltage, the $\overline{PGOOD}$ pin will be pulled low. When all outputs reach 90% of their programmed voltages, the C_T timer will trigger and a 20μA current source begins to charge the C_T pin. When the C_T pin reaches 1.1V, the output disconnect PNP turns on, connecting V_{ON}. In the event of any of the 4 outputs dropping below 10% of its normal voltage, PanelProtect circuitry pulls the C_T pin to ground, disabling V_{ON}.

When needed, the $\overline{PGOOD}$ pin can be used to drive the gate of a P-channel MOSFET that functions as output disconnect for AV_{DD}. For complete shutdown, the RUN-SS pin must be pulled to ground.



(3a)

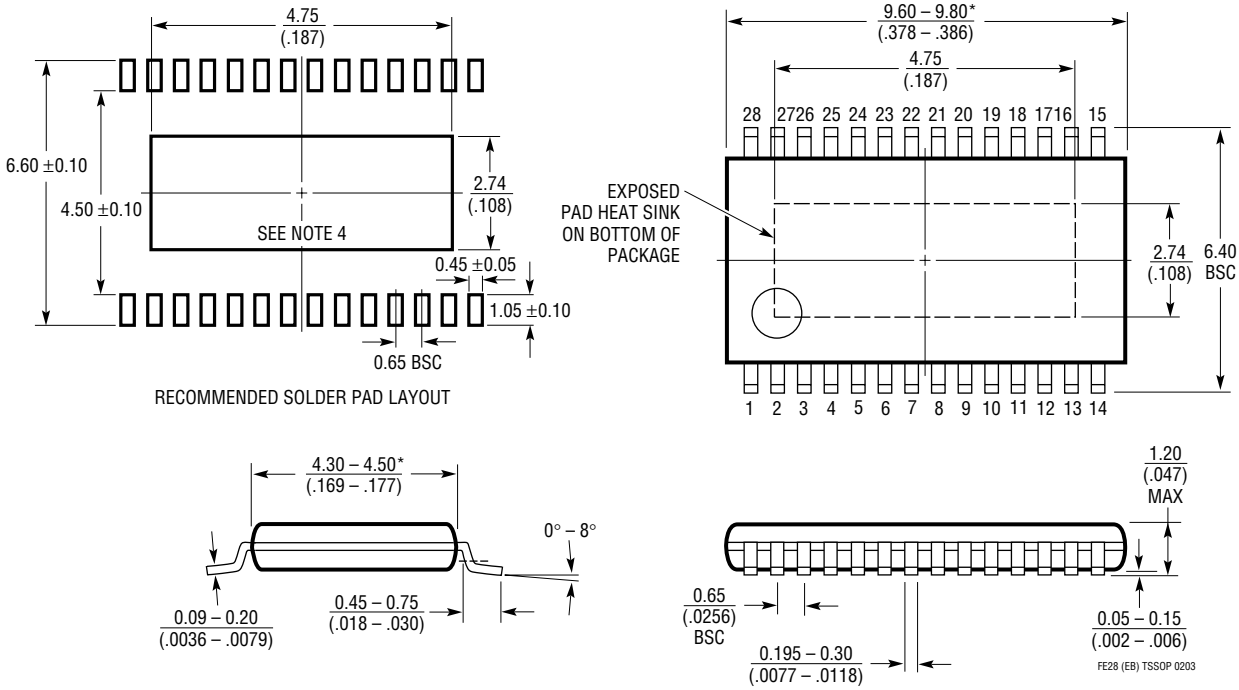


(3b)

Figure 3. LT1943 Power-Up Sequence. (Traces From Both Photos are Synchronized to the Same Trigger)

PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EB

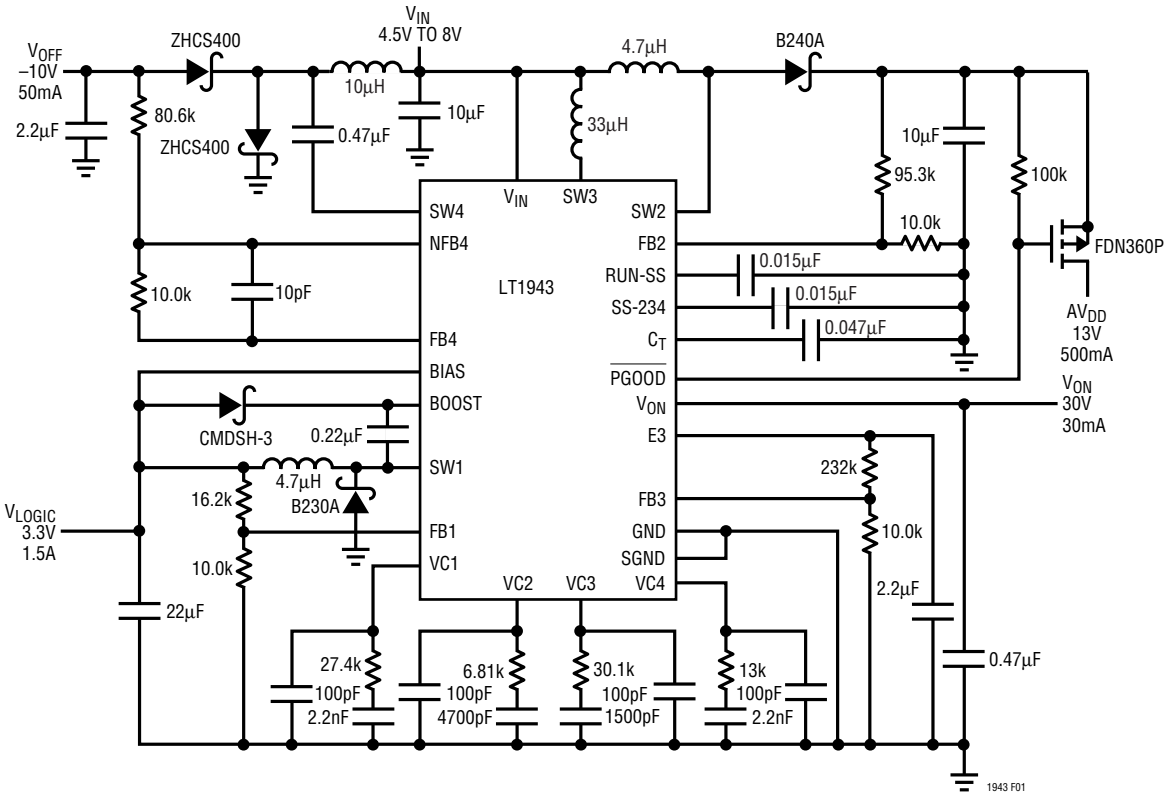


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

5V Input, Quad Output TFT-LCD Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1615/LT1615-1	300mA/80mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converters	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, ThinSOT™ Package
LT1940	Dual Output 1.4A (I_{OUT}), Constant 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.2V, I_Q: 2.5mA, I_{SD}: <1µA, TSSOP-16E Package
LT1944/LT1944-1	Dual Output 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1945	Dual Output, Pos/Neg, 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: ±34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1946/LT1946A	1.5mA (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.75V to 16V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1947	1.1A, 3MHz, TFT-LCD Triple Output Switching Regulator	V_{IN}: 2.7V to 8V, $V_{OUT(MAX)}$: 34V, I_Q: 9.5mA, I_{SD}: <1µA, MS Package
LT3464	85mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottky and Output Disconnect PNP	V_{IN}: 2.3V to 10V, $V_{OUT(MAX)}$: 34V, I_Q: 25µA, I_{SD}: <0.5µA, ThinSOT Package

ThinSOT is a trademark of Linear Technology Corporation.

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