

TC55257BPL/BFL/BSPL/BFTL/BTRL-85L/10L(LV)

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257BPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is $2\mu A$ at room temperature. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, while an output enable input ($\overline{OE}$) provides fast memory access. The TC55257BPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257BPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: $2\mu A$ (max.) at $T_a = 25^\circ C$
- Single 5V power supply
- Access time (max.)

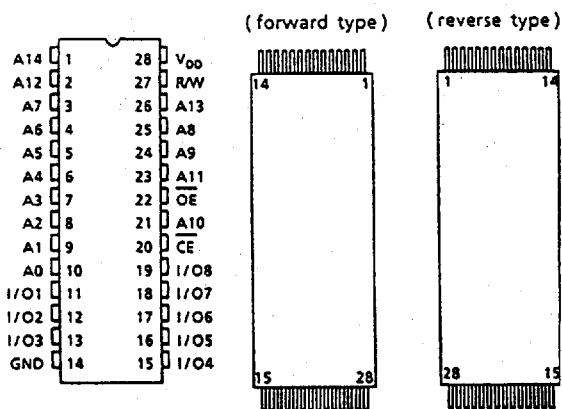
	TC55257BPL/BFL/BSPL/BFTL/BTRL	
	-85L(LV)	-10L(LV)
Access Time	85ns	100ns
Chip Enable Access Time	85ns	100ns
Output Enable Time	45ns	50ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257BPL : DIP28-P-600
 - TC55257BFL : SOP28-P-450
 - TC55257BSPL : DIP28-P-300B
 - TC55257BFTL : TSOP28-P
 - TC55257BTRL : TSOP28-P-A

Pin Names

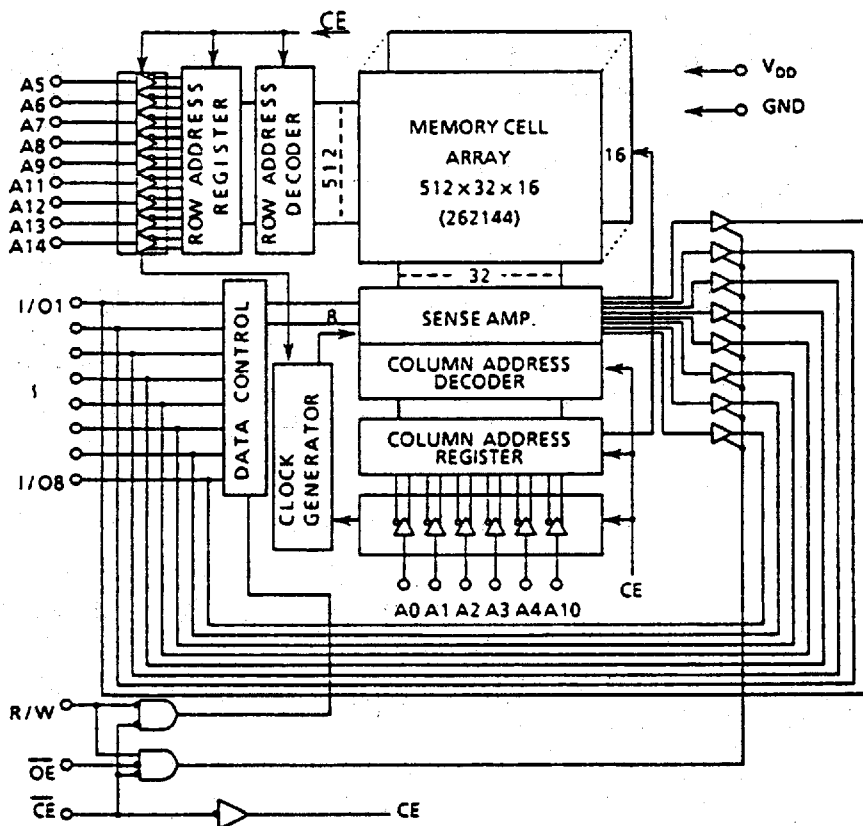
A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

Pin Connection (Top View)



PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V_{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A ₁₀

Block Diagram



Operating Mode

MODE	PIN	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read		L	L	H	D _{OUT}	I _{DDO}
Write		L	*	L	D _{IN}	I _{DDO}
Output Deselect		L	H	H	High-Z	I _{DDO}
Standby		H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	—	—	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	
I_{DDO2}		$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	3	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$T_a = 0 \sim 70^\circ\text{C}$	—	—	30
			$T_a = 25^\circ\text{C}$	—	—	2

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO}	$\overline{CE}$ Access Time	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	
t _{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	
t _{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

Write Cycle

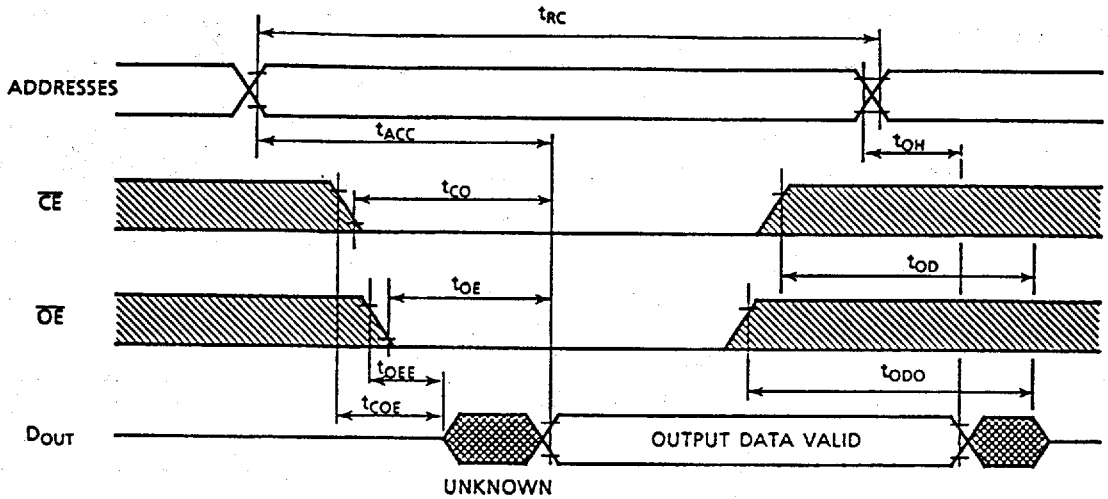
SYMBOL	PARAMETER	TC55257BPL/BFL/BSPL/BFTL/BTRL				UNIT
		-85L(LV)		-10L(LV)		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	
t _{ODW}	R/W to Output in High-Z	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	
t _{DS}	Data Setup Time	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC Test Conditions

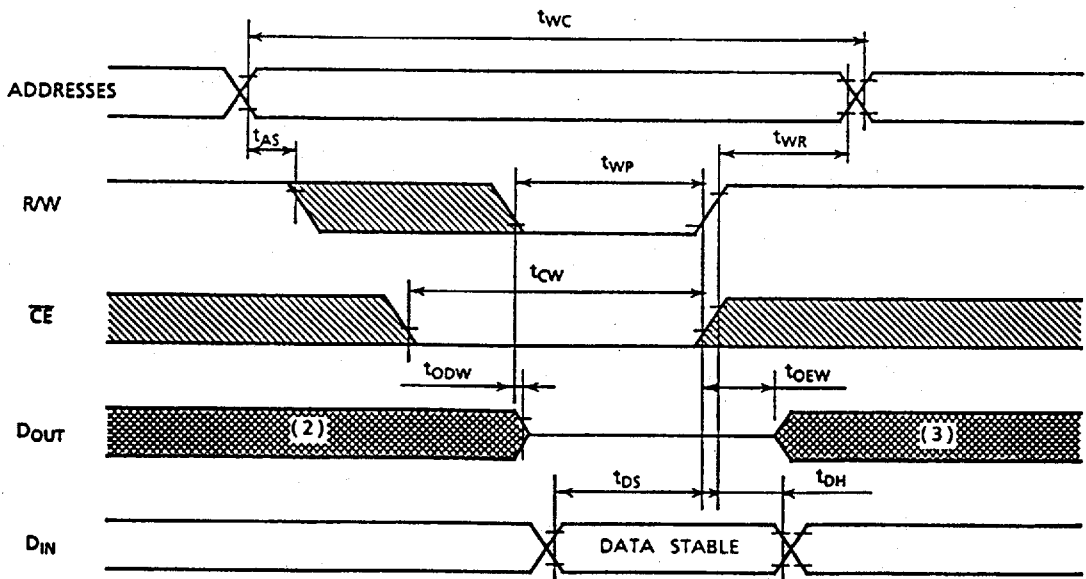
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.2V/0.8V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

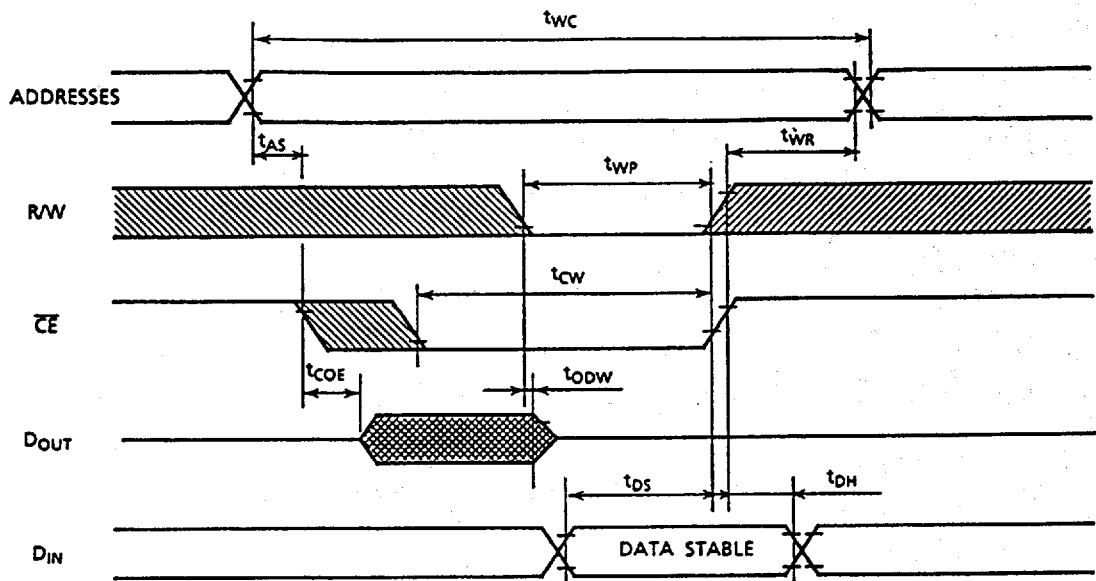
Timing Waveforms

Read Cycle ⁽¹⁾



Write Cycle 1 ⁽⁴⁾ (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{CE}$ Controlled Write)

Notes:

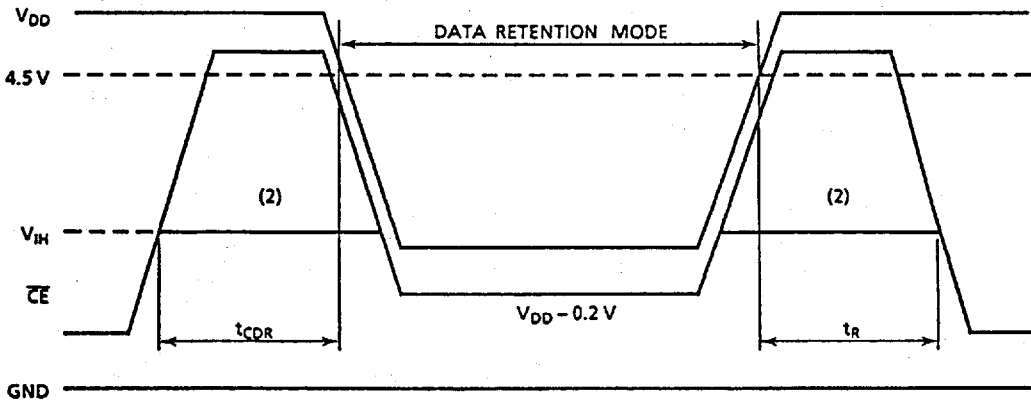
1. R/W is high for read cycles.
2. If the $\overline{CE}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{CE}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{OE}$ is high during a write cycle, the outputs are in a high impedance state during this period.

Data Retention Characteristics ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0\text{V}$	—	20	μA
		$V_{DH} = 5.5\text{V}$	—	30	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	μs
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

$\overline{\text{CE}}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	$V_{DD} - 0.2$	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	—	0.2	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		—	—	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$		—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.2V$		-0.1	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.2V$		0.1	—	—	mA
I_{DDO2}	Operating Current	$\overline{CE} = 0.2V$ $R/W = V_{DD} - 0.2V$ $I_{OUT} = 0\text{mA}$ Other Inputs = $V_{DD} - 0.2V/0.2V$	t_{cycle} Min.	—	—	20	mA
			1 μs	—	—	5	
I_{DDs2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$	$T_a = 0 \sim 70^\circ\text{C}$	—	—	20	μA
			$T_a = 25^\circ\text{C}$	—	1	2	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

3V Operation**DC Characteristics** ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 3V \pm 10\%$)**Read Cycle**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	200	—	ns
t_{ACC}	Address Access Time	—	200	
t_{CO}	$\overline{CE}$ Access Time	—	200	
t_{OE}	Output Enable to Output in Valid	—	100	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	—	100	
t_{ODO}	Output Enable to Output in High-Z	—	80	
t_{OH}	Output Data Hold Time	10	—	

Write Cycle

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	200	—	ns
t_{WP}	Write Pulse Width	150	—	
t_{CW}	Chip Selection to End of Write	180	—	
t_{AS}	Address Setup Time	0	—	
t_{WR}	Write Recovery Time	5	—	
t_{ODW}	R/W to Output in High-Z	—	100	
t_{OEW}	R/W to Output in Low-Z	5	—	
t_{DS}	Data Setup Time	90	—	
t_{DH}	Data Hold Time	0	—	

AC Test Conditions

Input Pulse Levels	$V_{DD} - 0.2V/0.2V$
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	$C_L = 100\text{pF}$