SMP Controller For High Performance Process Power Supplies

FEATURES

- Runs on 3.3- or 5-V Supplies
- Adjustable, High Precision Output Voltage
- High Frequency Operation (>1 MHz)
- High Efficiency Synchronous Switching
- Full Set of Protection Circuitry
- 2000-V ESD Rating (Si9140CQ/DQ)

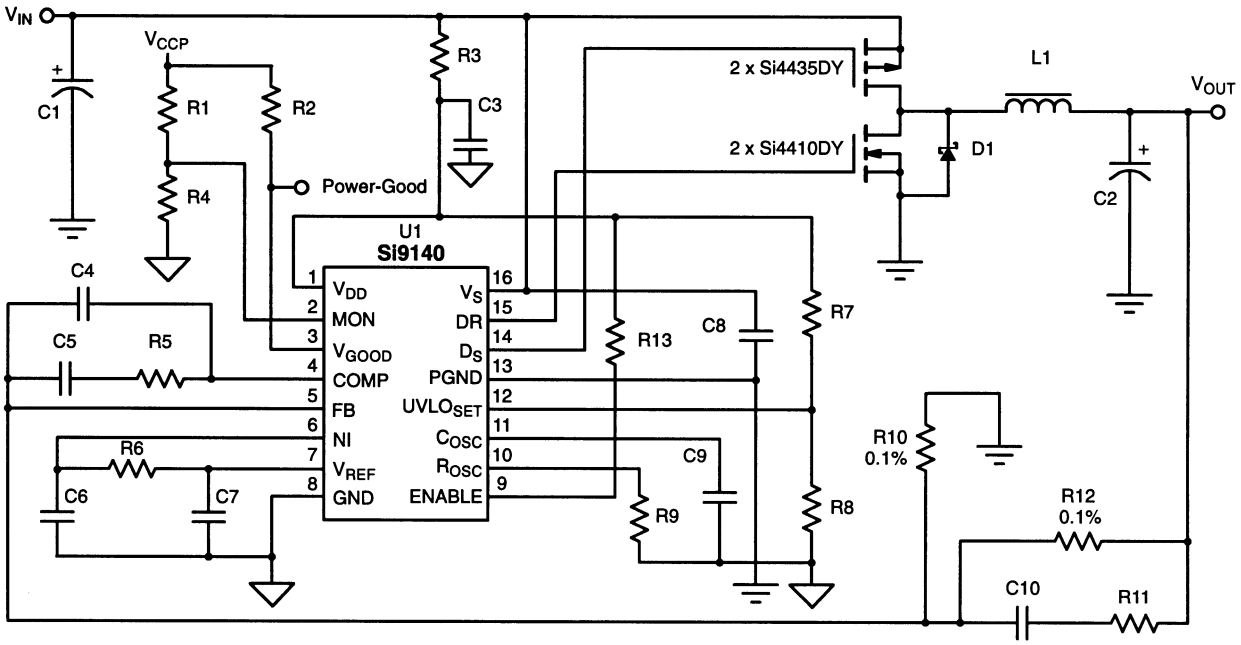
DESCRIPTION

Siliconix' Si9140 Buck converter IC is a high-performance, surface-mount switchmode controller made to power the new generation of low-voltage, high-performance microprocessors. The Si9140 has an input voltage range of 3 to 6.5 V to simplify power supply designs in desktop PCs. Its high-frequency switching capability and wide bandwidth feedback loop provide tight, absolute static and transient load regulation. Circuits using the Si9140 can be implemented with low-profile, inexpensive inductors, and will dramatically minimize power supply output and processor decoupling capacitance. The Si9140 is designed to meet the stringent regulation requirements of new and future high-frequency microprocessors, while improving the overall efficiency in new "green" systems.

Today's state-of-the-art microprocessors run at frequencies over 100 MHz. Processor clock speeds are going up and so are current requirements, but operating voltages are going down. These simultaneous changes have made dedicated, high-frequency, point-of-use buck converters an essential part of any system design. These point-of-use converters must operate at higher frequencies and provide wider feedback bandwidths than existing converters, which typically operate at less than 250 kHz and have feedback bandwidths of less than 50 kHz. The Si9140's 100-kHz feedback loop bandwidth ensures a minimum improvement of one-half the required output/decoupling capacitance, resulting in a tremendous reduction in board size and cost of implementation.

With the microprocessing power of any PC representing an investment of hundreds of dollars, designers need to ensure that the reliable operation of the processor will not be affected by the power supply. The Si9140 provides this assurance. A demo board, the Si9140DB, is available.

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND.

V_{DD}, V_S . . . . . 8 V
P_{GND} . . . . . ±0.3 V
V_{DD} to V_S . . . . . -0.3 V
Linear Inputs . . . . . -0.3 V to V_{DD} +0.3 V
Logic Inputs . . . . . -0.3 V to V_{DD} +0.3 V
Peak Output Drive Current . . . . . 350 mA
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature . . . . . 150°C
Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] . . . . . 900 mW
16-Pin TSSOP (Q Suffix)[c] . . . . . 925 mW

Thermal Impedance (Θ_{JA})
16-Pin SOIC (Y Suffix) . . . . . 140°C/W
16-Pin TSSOP (Q Suffix). . . . . 135°C/W
Operating Temperature
C Suffix . . . . . 0° to 70°C
D Suffix . . . . . -40° to 85°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.
c. Derate 7.4 mW/°C above 25°C.

** Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.*

RECOMMENDED OPERATING RANGE

Voltages Referenced to GND.

V_{DD} . . . . . 3 V to 6.5 V
V_S. . . . . 3 V to 6.5 V
f_{OSC} . . . . . 20 kHz to 2 MHz
R_{OSC} . . . . . 5 kΩ to 250 kΩ
C_{OSC} . . . . . 47 pF to 200 pF
Linear Inputs . . . . . 0 to V_{DD}
Digital Inputs . . . . . 0 to V_{DD}
V_{REF} Load Resistance . . . . . >150 kΩ

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] $3\ V \le V_{DD} \le 6.5\ V$, $V_{DD} = V_S$, GND = P_{GND}	Limits C Suffix 0 to 70°C, D Suffix -40 to 85°C Min[b]	Typ	Max[b]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = -10 µA	1.455		1.545	V
		T_A = 25°C	1.477	1.50	1.523	
Oscillator						
Maximum Frequency[c]	f_{MAX}	V_{DD} = 5 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ	2.0			MHz
Accuracy	f_{OSC}	V_{DD} = 5 V, C_{OSC} = 100 pF, R_{OSC} = 7.50 kΩ, T_A = 25°C	0.85	1.0	1.15	
R_{OSC} Voltage	V_{ROSC}			1.0		V
Voltage Stability[c]	Δf/f	4 V ≤ V_{DD} ≤ 6 V, Ref to 5 V, T_A = 25°C	-8		8	%
Temperature Stability[c]		Referenced to 25°C		±5		
Error Amplifier (C_{OSC} = GND, OSC Disabled)						
Input Bias Current	I_{FB}	$V_{NI} = V_{REF}$, V_{FB} = 1.0 V	-1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	$V_{NI} = V_{REF}$	-15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{EA}	Source (V_{FB} = 1 V, NI = V_{REF})		-2.0	-1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	P_{SRR}	3 V < V_{DD} < 6.5 V		60		dB

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 3 V ≤ V_{DD} ≤ 6.5 V, V_{DD} = V_S GND = P_{GND}	Limits C Suffix 0 to 70°C D Suffix -40 to 85°C Min[b]	Typ	Max[b]	Unit
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysteresis	V_{HYS}	V_{UVLOLH} - V_{UVLOHL}		175		mV
UVLO Input Current	$I_{UVLO(SET)}$	V_{UVLO} = 0 to V_{DD}	-100		100	nA
Output Drive (D_R AND D_S)						
Output High Voltage	V_{OH}	V_S = V_{DD} = 5 V, I_{OUT} = -10 mA	4.7	4.8		V
Output Low Voltage	V_{OL}	V_S = V_{DD} = 5 V, I_{OUT} = 10 mA		0.2	0.3	
Peak Output Current	I_{SOURCE}	V_S = V_{DD} = 5 V, V_{OUT} = 0 V		-380	-260	mA
Peak Output Current	I_{SINK}	V_S = V_{DD} = 5 V, V_{OUT} = 5 V	200	300		
Break-Before-Make	t_{BBM}	V_{DD} = 6.5 V		40		nS
Logic						
ENABLE Turn-On Delay	t_{dEN}	ENABLE Delay to Output, EN_{LH}, V_{DD} = 5 V		1.5		µs
ENABLE Logic Low	V_{ENL}				0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}		0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}	-1.0		1.0	µA
V_{GOOD} Comparator (Voltage-Good Comparator)						
Input Offset Voltage	V_{OS}	V_{IN} Common Mode Voltage = V_{REF}, V_{DD} = 5 V	-45	0	45	mV
Input Hysteresis	V_{INHYS}			10		
Input Bias Current	I_{BMON}	V_{IN} = V_{REF}, V_{DD} = 5 V	-1	0	1	µA
Output Sink I	I_{SINK}	V_{OUT} = 5 V, V_{DD} = 5 V	6	9		mA
Output Low Voltage	V_{OL}	I_{OUT} = 2 mA, V_{DD} = 5 V		350	500	mV
Supply						
Supply Current-Normal Mode	I_{DD}	f_{OSC} = 1 MHz, R_{OSC} = 7.50 kΩ		1.6	2.3	mA
Supply Current-Standby Mode		ENABLE < 0.4 V		250	330	µA

Notes

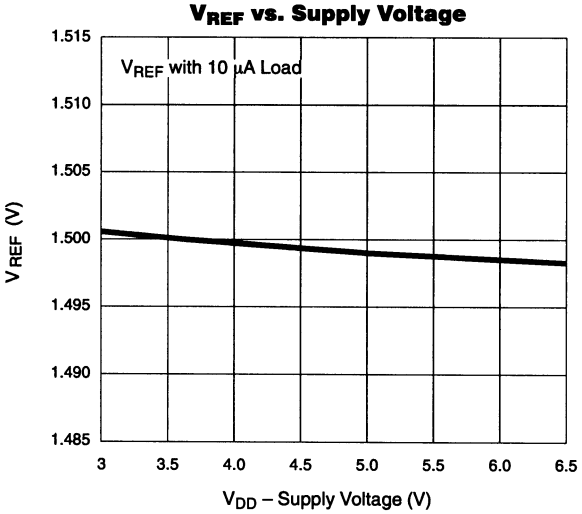
a. 100 pF includes C_{STRAY} on C_{OSC}.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

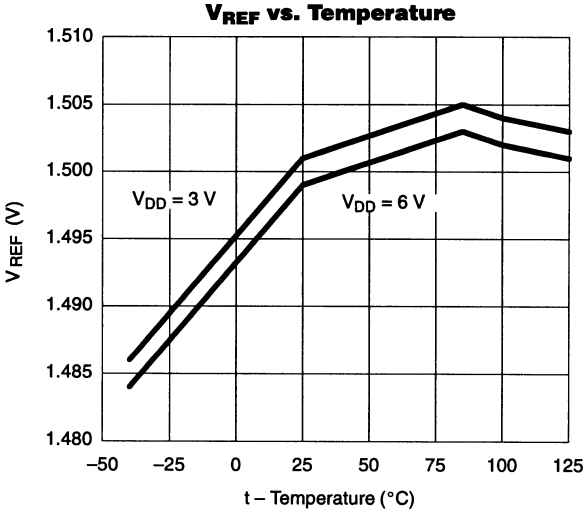
c. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

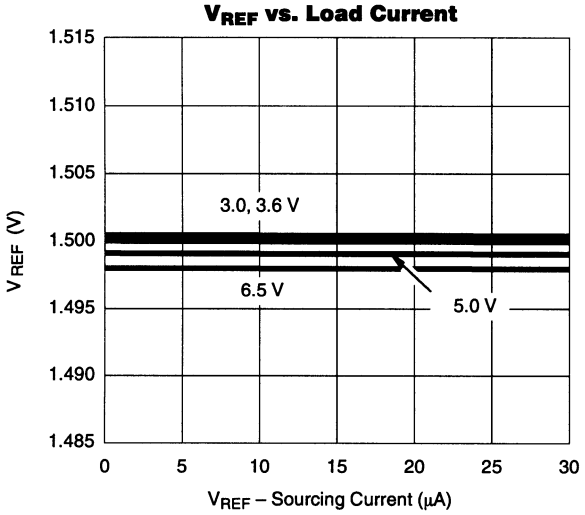
V_{REF} vs. Supply Voltage



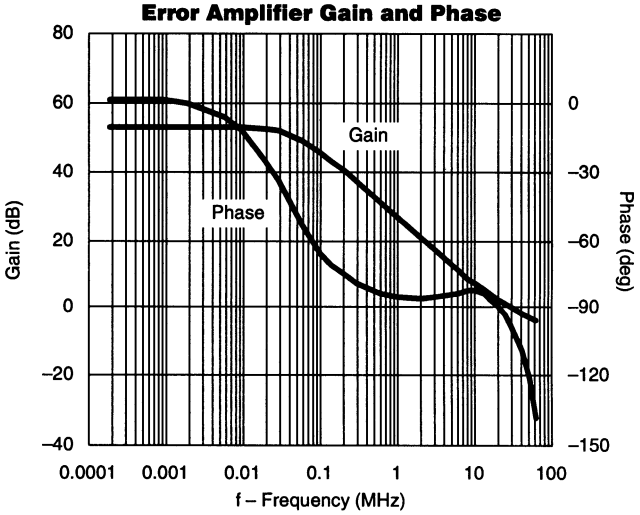
V_{REF} vs. Temperature



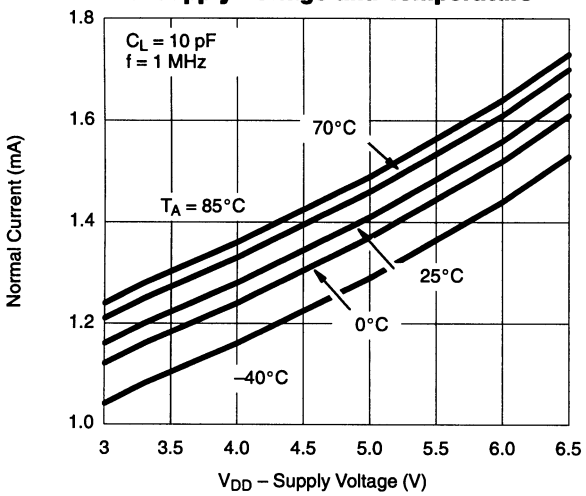
V_{REF} vs. Load Current



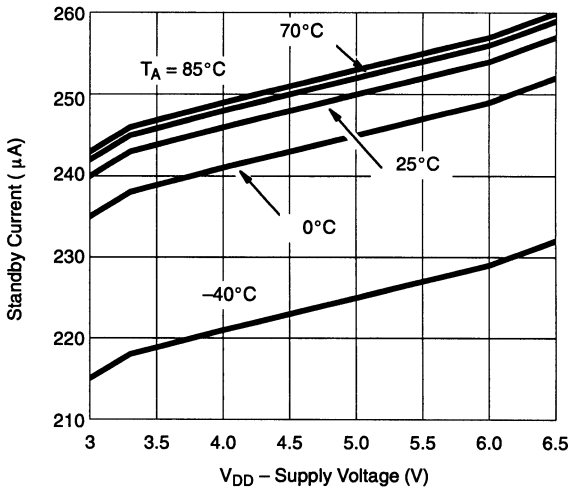
Error Amplifier Gain and Phase



Supply Current vs. Supply Voltage and Temperature

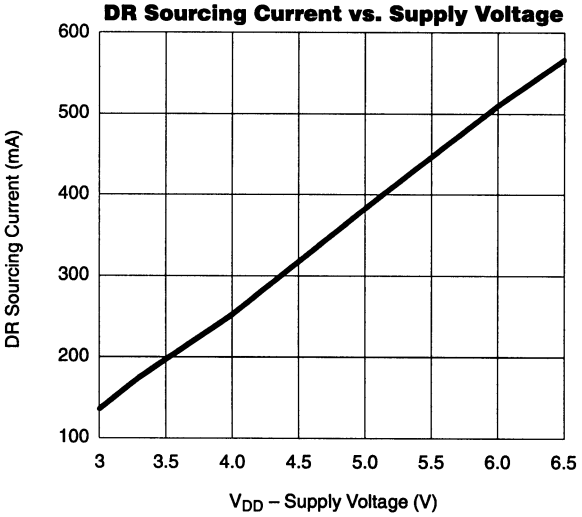


Standby Current vs. Supply Voltage and Temperature

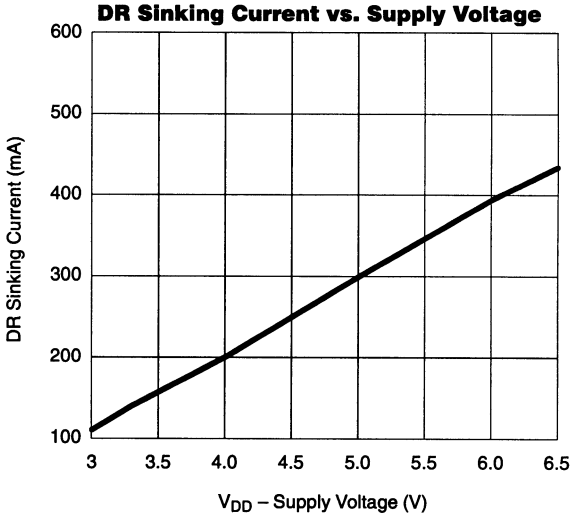


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

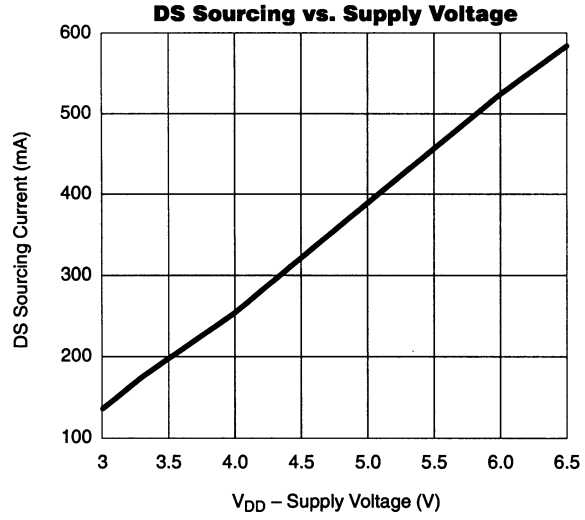
DR Sourcing Current vs. Supply Voltage



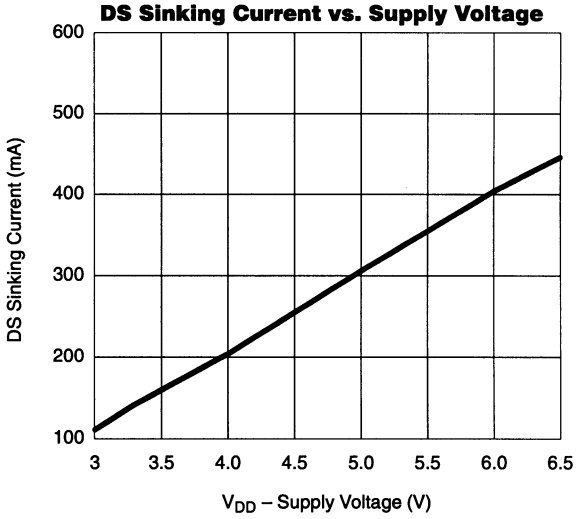
DR Sinking Current vs. Supply Voltage



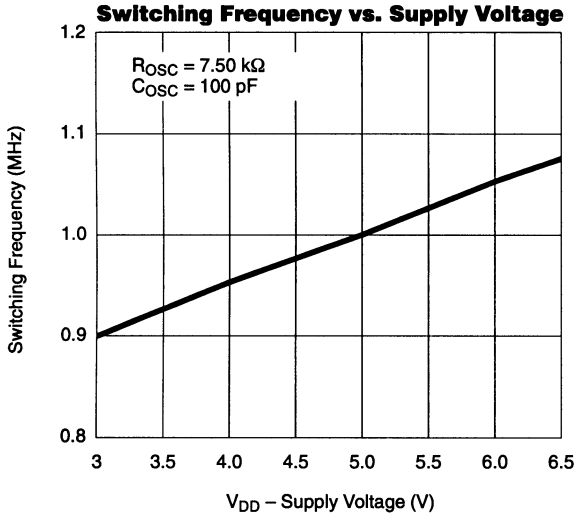
DS Sourcing vs. Supply Voltage



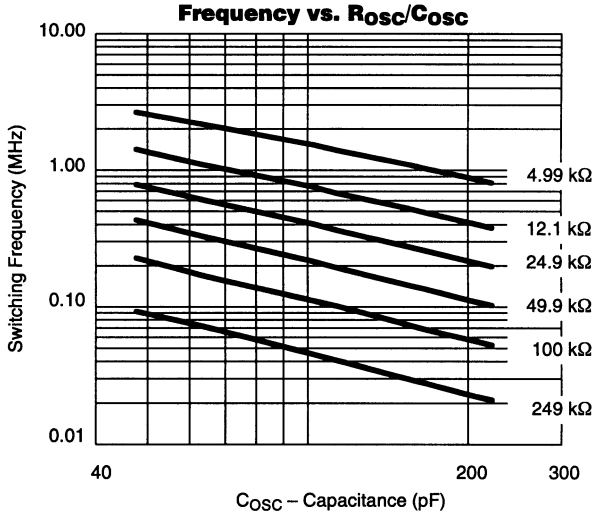
DS Sinking Current vs. Supply Voltage



Switching Frequency vs. Supply Voltage

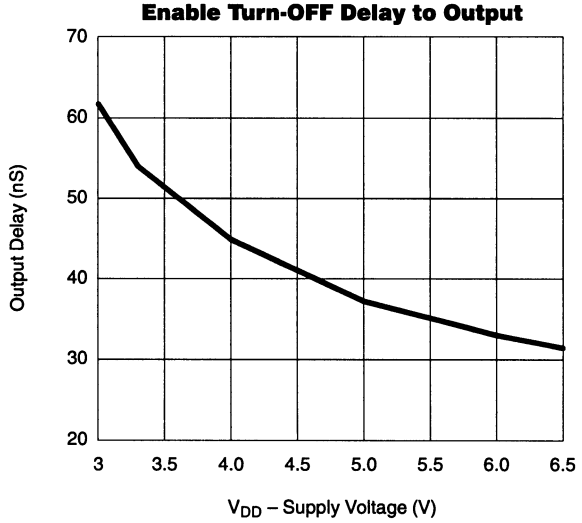


Frequency vs. R_{OSC}/C_{OSC}

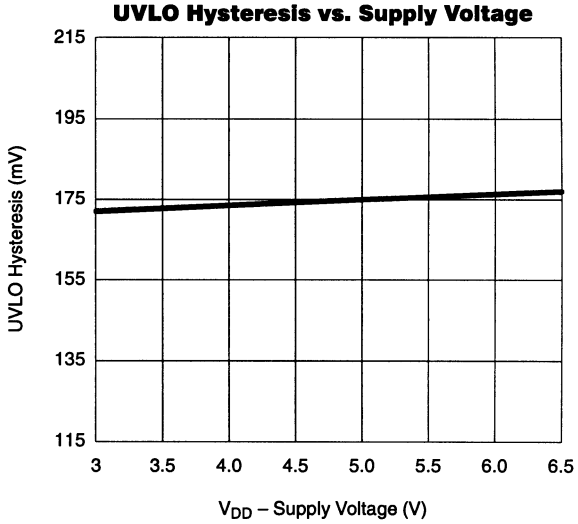


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

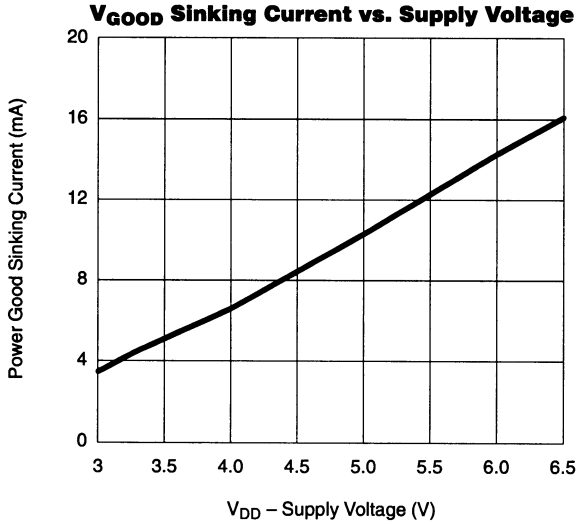
Enable Turn-OFF Delay to Output



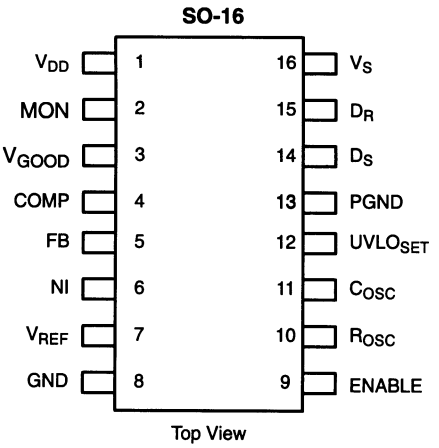
UVLO Hysteresis vs. Supply Voltage

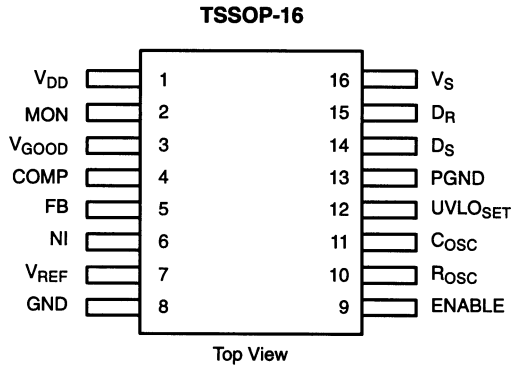


V_{GOOD} Sinking Current vs. Supply Voltage



PIN CONFIGURATIONS





ORDERING INFORMATION	
Temperature Range	**Part Number**
0° to 70°C	Si9140CY
-40° to 85°C	Si9140DY

ORDERING INFORMATION	
Temperature Range	**Part Number**
0° to 70°C	Si9140CQ
-40° to 85°C	Si9140DQ

PIN DESCRIPTION

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: MON

Non-inverting input of a comparator. Inverting input is tied internally to reference voltage. This comparator is typically used to monitor the output voltage and to flag the processor when the output voltage falls out of regulation.

Pin 3: V_{GOOD}

This is an open drain output. It will be held at ground when the voltage at MON (Pin 2) is less than the internal reference. An external pull-up resistor will pull this pin high if the MON pin (Pin 2) is higher than the V_{REF}. (Refer to Pin 2 description.)

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. An external resistor divider is connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to V_{REF} or an external reference.

Pin 7: V_{REF}

This pin supplies a 1.5-V reference.

Pin 8: GND (Ground)

Pin 9: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and D_S goes high while D_R goes low.

Pin 10: R_{OSC}

A resistor connected from this pin to ground sets the oscillator's capacitor C_{OSC}, charge and discharge current. See the oscillator section of the description of operation.

Pin 11: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency.

$$f_{OSC} \cong \frac{0.75}{R_{OSC} \times C_{OSC}} \qquad (\text{at } V_{DD} = 5.0 \text{ V})$$

Pin 12: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 165 mV.

Pin 13: P_{GND}

The negative return for the V_S supply.

Pin 14: D_S

This CMOS push-pull output pin drives the external p-channel MOSFET. This pin will be high in the standby mode. A break-before-make function between D_S and D_R is built-in.

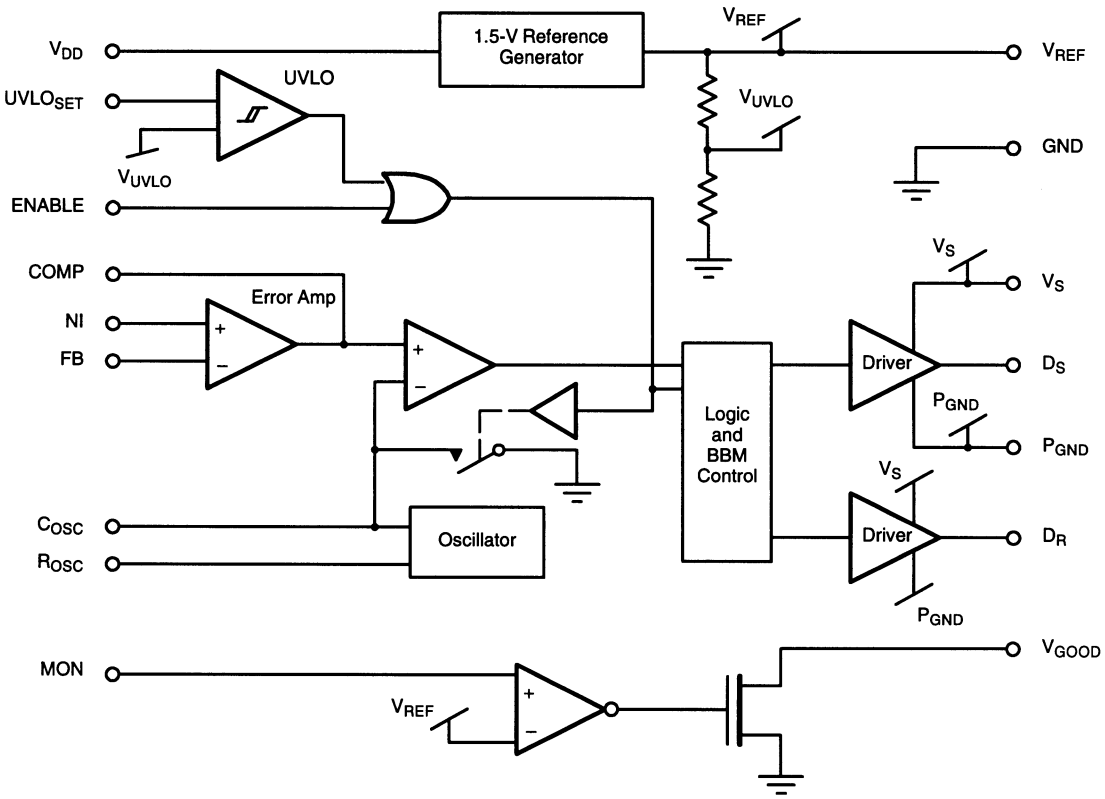
Pin 15: D_R

This CMOS push-pull output pin drives the external n-channel MOSFET. This pin will be low in the standby mode. A break-before-make function between the D_S and D_R is built-in.

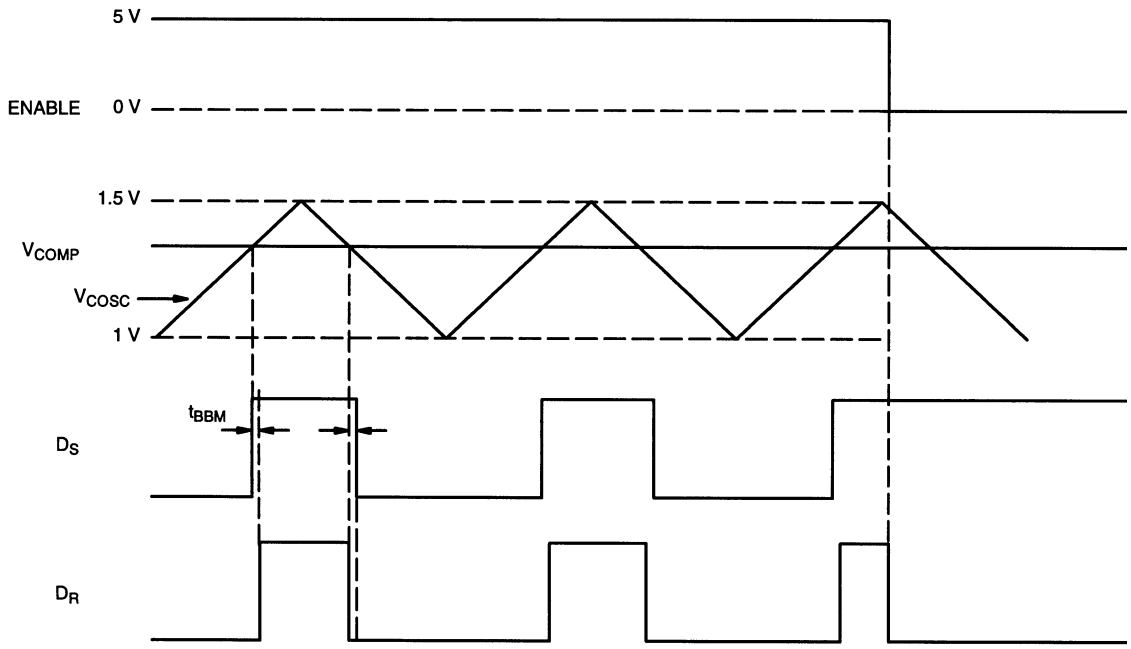
Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output drivers. A bypass capacitor is required.

FUNCTIONAL BLOCK DIAGRAM



TIMING WAVEFORMS



DESCRIPTION OF OPERATION

Schematics of the Si9140 dc-to-dc conversion solutions for high-performance PC microprocessors are shown in Figure 1 and 2 respectively. These solutions are geared to meet the extremely demanding transient regulation and power requirements of these new microprocessors at minimal cost and with a minimal parts count. The two solutions are nearly identical, except for slight variations in output voltage, load transient amplitude, and specified power. Figure 3 is a schematic diagram for a 3.3-V logic converter.

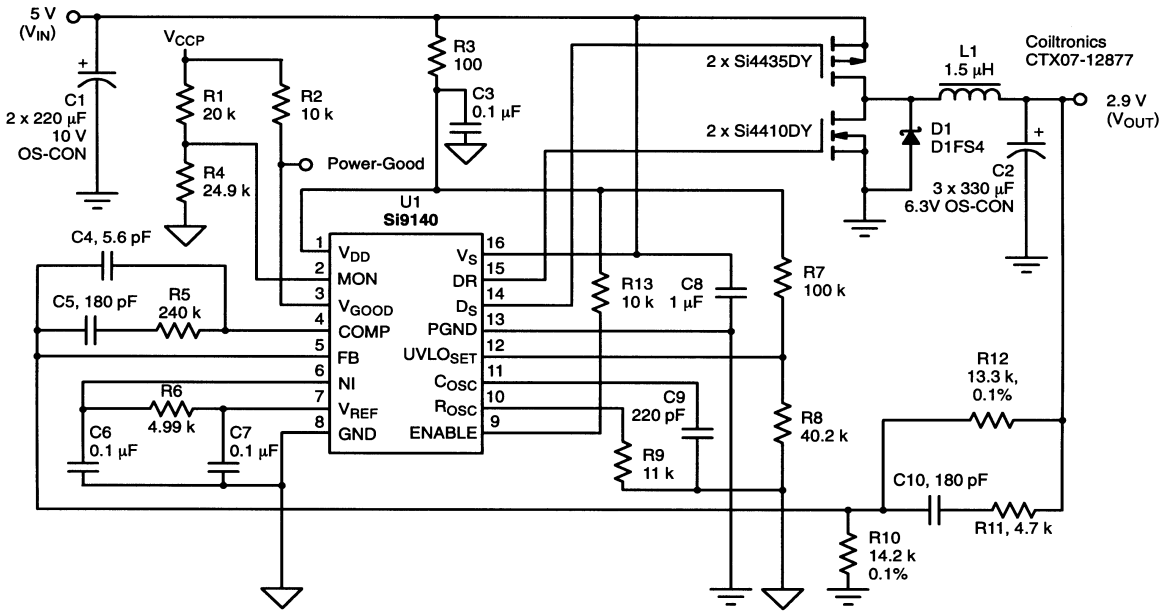


FIGURE 1. 2.9 V @ 10 A

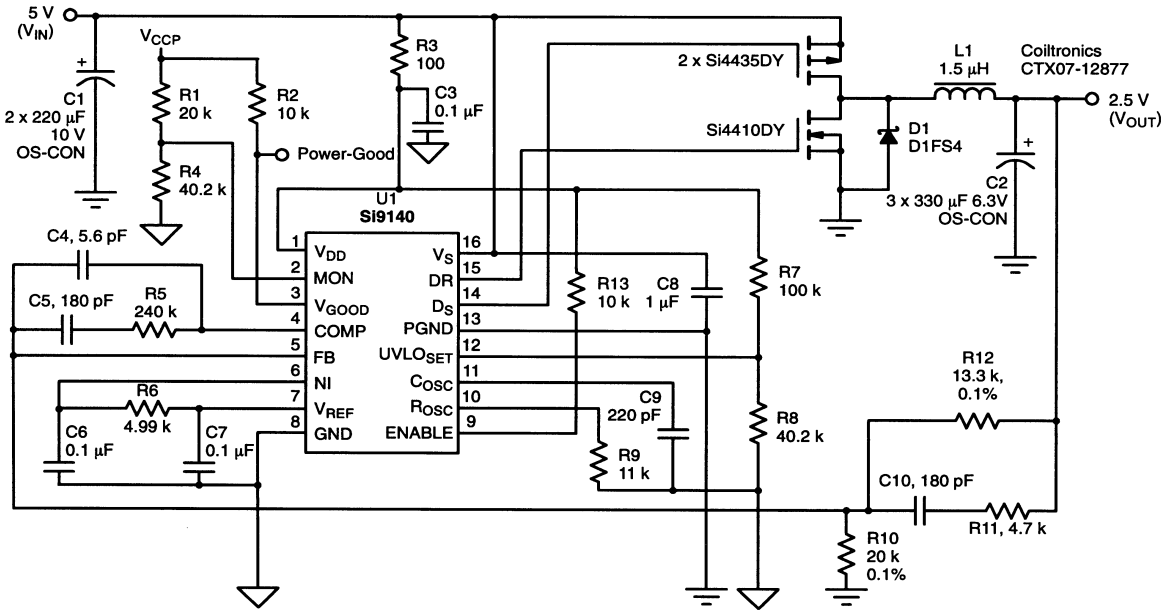


FIGURE 2. 2.5 V @ 8.5 A

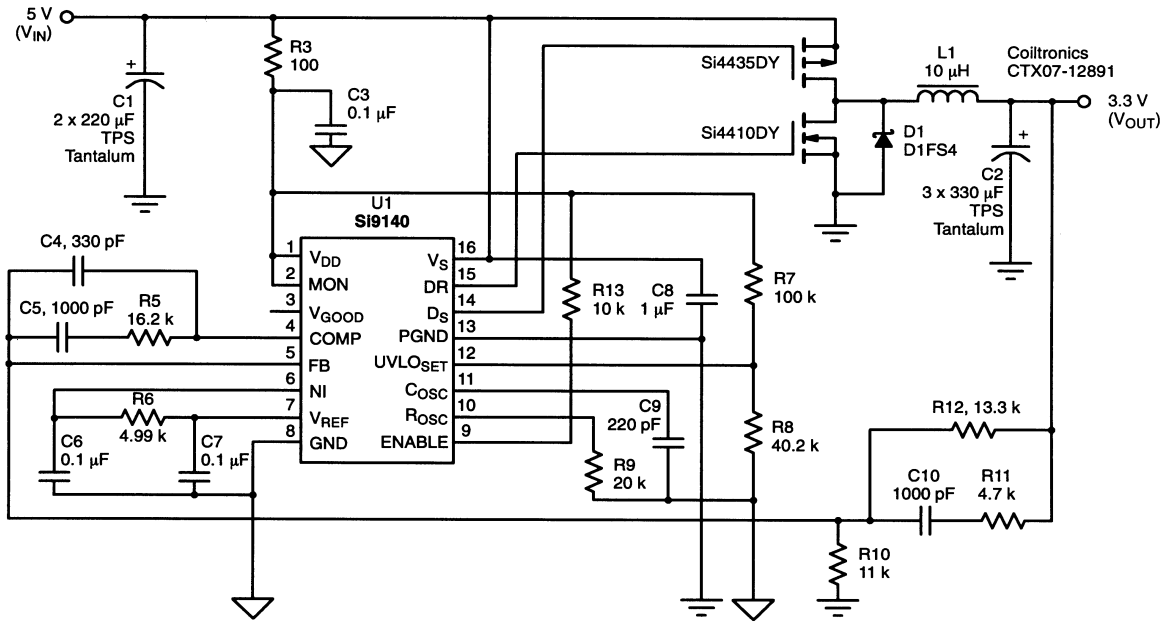


FIGURE 3. 3.3 V @ 5 A

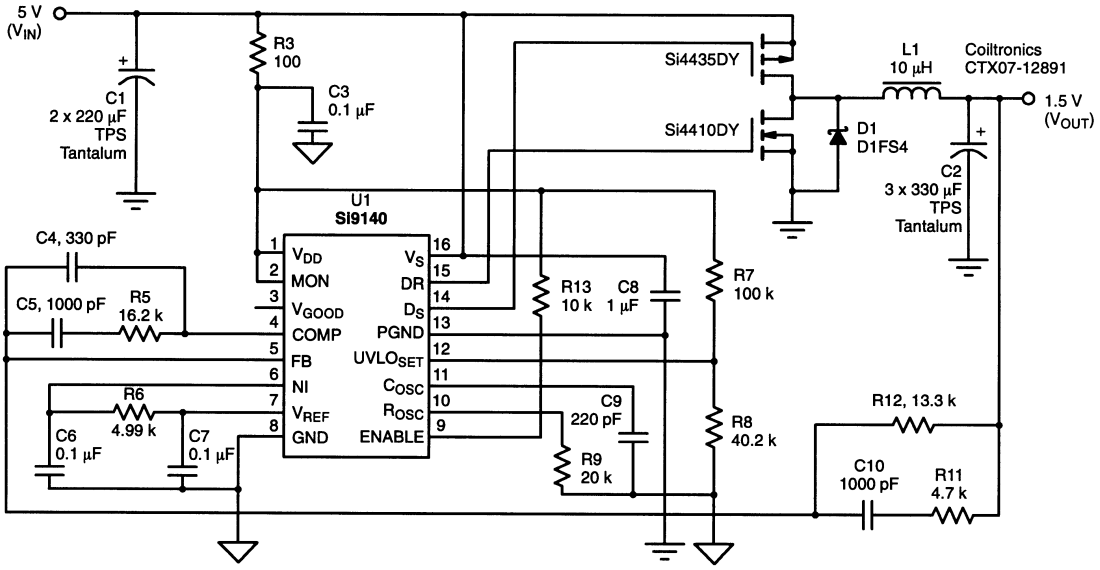


FIGURE 4. 1.5-V Converter for GTL+ Bus @ 5 A

Figure 4 is a schematic diagram of a converter which produces 1.5 V for a GTL bus.

Each of these dc-to-dc converters has four major sections:

- PWM Controller-regulates the output voltage
- Switch and Synchronous Rectification MOSFETs-delivers the power to the load
- Inductor-filters and stores the energy
- Input/Output Capacitor-filters the ripple

The functions of each circuit are explained in detail below. Design equations are provided to optimize each application circuit.

PWM CONTROLLER

There are generally two types of controllers, voltage mode or current mode. In voltage mode control, an error voltage is generated by comparing the output voltage to the reference voltage. The error voltage is then compared to an artificial ramp, and the result is the duty cycle necessary to regulate the output voltage. In current mode, an actual inductor current is used, in place of the artificial ramp, to sense the voltage across the current sense resistor.

The logic and timing sequence for voltage mode control is shown in Figure 5. The Si9140 offers voltage mode control, which is better suited for applications requiring both fast transient response and high output current.

Current mode control requires a current sense resistor to monitor the inductor current. A 10-mΩ sense resistor in a 10-A design will dissipate 1 W, decreasing efficiency by 3.5%. Such a design would require a 2-W resistor to satisfy derating criteria, besides requiring additional board space. Voltage mode control is a second-order LC system and has a faster natural transient response compared to current mode control (first-order RC system). Current mode has the advantage of providing an inherently good line regulation. But the situations where line voltage is fixed, as in the point-of-use conversion for microprocessors, this feature is wasted. Current mode control also provides automatic pulse-to-pulse current limiting. This feature requires a current sense resistor as stated above. These characteristics make voltage mode control ideal for high-end microprocessor power supplies.

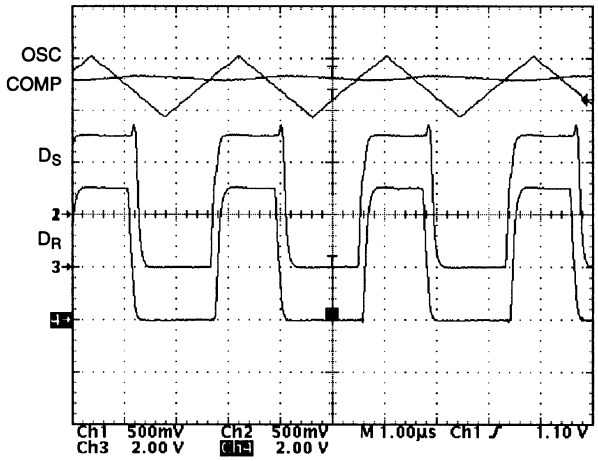


FIGURE 5. Voltage Mode Logic and Timing Diagram

The error amplifier of the PWM controller plays a major role in determining the output voltage, stability, and the transient response of the power supply. In the Si9140, the non-inverting input of the error amplifier is available for use with an external precision reference for tighter tolerance regulation. With a two-pair lead-lag compensation network, it is easy to create a stable 100-kHz closed loop converter with the Si9140 error amplifier.

The Si9140 achieves the 5-µS transient response by generating a 100-kHz closed-loop bandwidth. This is possible only by switching above 400 kHz and utilizing an error amplifier with at least a 10-MHz bandwidth. The Si9140 controller has a 25-MHz unity gain bandwidth error amplifier. The switching frequency must be at least four times greater than the desired closed-loop bandwidth to prevent oscillation. To respond to the stimuli, the error amplifier bandwidth needs to be at least 10 times larger than the desired bandwidth.

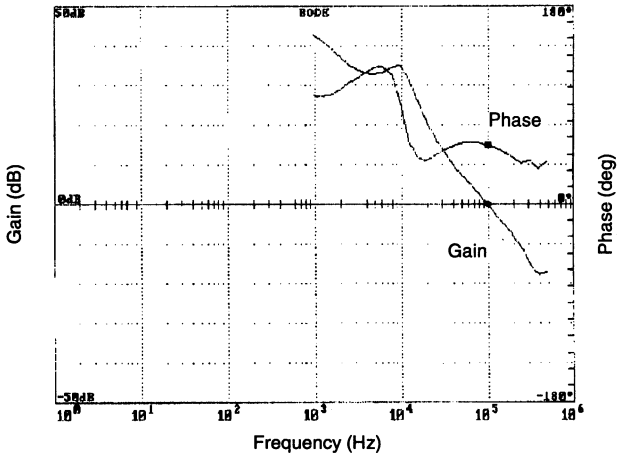


FIGURE 6. 100-kHz BW Synchronous Buck Converter

The Si9140 solution requires only three 330-µF OS-CON capacitors on the output of power supply to meet the 10-A transient requirement. Other converter solutions on the market with 20- to 50-kHz closed loop bandwidths typically require two to five times the output capacitance specified above to match the Si9140's performance.

The theoretical issues and analytical steps involved in compensating a feedback network are beyond the scope of this application note. However, to ease the converter design for today's high-performance microprocessors, typical component values for the feedback network are provided in Table 1 for various combinations of output capacitance. Figure 6 shows the Bode plot (frequency domain) of the 2.9-V converter shown schematically in Figure 1.

TABLE 1. Feedback Network Component Values

Total Output and Decoupling Capacitance	C4	C5	R5
3 x 330 µF[a] . . . . . .Os-con 6 x 100 µF[b] . . . . . .Tantalum 25 x 1 µF[b] . . . . . .Ceramic	5.6 pF	180 pF	240 k
2 x 330 µF[a] . . . . . .Os-con 4 x 100 µF[b] . . . . . .Tantalum 25 x 1 µF[b] . . . . . .Ceramic	10 pF	220 pF	200 k
3 x 330 µF[a] . . . . . .Tantalum 4 x 100 µF[b] . . . . . .Tantalum 25 x 1 µF[b] . . . . . .Ceramic	10 pF	100 pF	100 k

Notes:

a. Power supply output capacitance.

b. µprocessor decoupling capacitance.

Figure 7 is the measured transient response (time domain) for the 10-A step response. The measured transient response shows the processor voltage regulating to 70 mV, well within the 0.145-V regulation.

The Si9140's switching frequency is determined by the external R_{OSC} and C_{OSC} values, allowing designers to set the switching frequency of their choice. For applications where space is the main constraint, the switching frequency can be set as high as 2 MHz to minimize inductor and output capacitor size. In applications where efficiency is the main concern, the switching frequency can be set low to maximize battery life. The switching frequency for high-performance processors applications circuits are set for 400 kHz. The equation for switching frequency is:

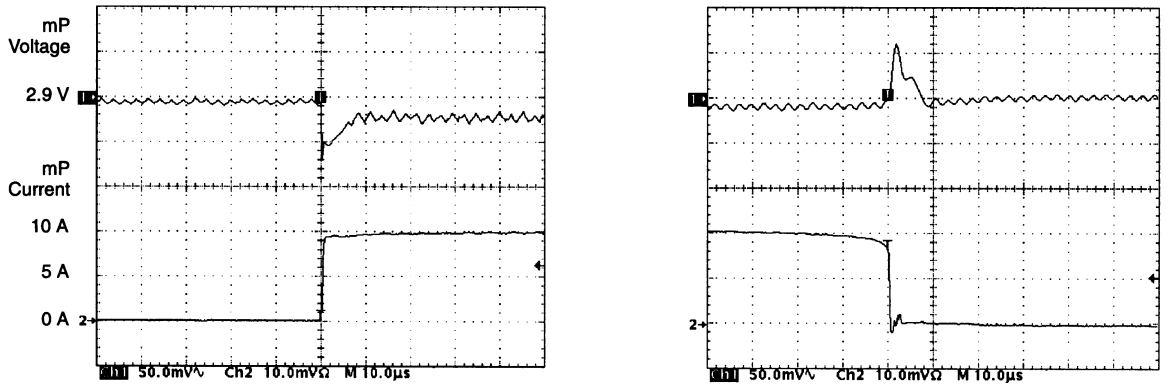
$$f_{OSC} \approx \frac{0.75}{R_{OSC} \times C_{OSC}} \qquad (\text{at } V_{DD} = 5.0 \text{ V})$$

The precision reference is set at 1.5 V ± 1.5%. The reference is capable of sourcing up to 1 mA. The combination of 1.5% reference and 3.5% transient load regulation safely complies with the ±5% regulation requirement. If additional margin is desired, an external precision reference can be used in place of the internal 1.5-V reference.

SWITCHING AND SYNCHRONOUS RECTIFICATION MOSFETS

The synchronous gate drive outputs of Si9140 PWM controller drive the high-side p-channel switch MOSFET and the low-side n-channel synchronous rectifier MOSFET. The physical difference between the non-synchronous to synchronous rectification requires an additional MOSFET across the free-wheeling diode (D1). The inductor current will reach 0 A if the peak-to-peak inductor current equals twice the output current. In synchronous rectification mode, current is allowed to flow backwards from the inductor (L1) through the synchronous MOSFET (Q3) and to the output capacitors (C2) once the current reaches 0 A. Refer to schematic on Figure 1. In non-synchronous rectification, the diode (D1) prevents the current from flowing in the reverse direction. This minor difference has a drastic affect on the performance of a power supply. By allowing the current to flow in the reverse direction, it preserves the continuous inductor current mode, maintaining the wide converter bandwidth and improving efficiency. Also, maintaining the continuous current mode during light load to full load guarantees consistent transient response throughout a wide range of load conditions.

The transition from stop clock and auto halt to active mode is a perfect example. The microprocessor current can vary from 0.5 A to 10 A or greater during these transitions. If the converter were to operate in discontinuous current mode during the stop clock and auto halt modes, the transfer function of the converter would be different compared to operation in the active mode. In discontinuous current mode, the converter bandwidth can be 10 to 15 times lower than the continuous current mode (Figure 8). Therefore, the response time will also be 10 to 15 times slower, violating the microprocessor's regulator requirements. This could result in unreliable operation of the microprocessor.



a) Transient Response from 0- to 10-A Step Load

b) Transient Response from 10- to 0-A Step Load

FIGURE 7.

For these reasons, synchronous rectification is a must in today's microprocessors power supply design. Pulse-skipping modes are undesirable in high-performance microprocessor power supplies, especially when the minimum load current is as high as 500 mA. This pulse-skipping mode disables the synchronous rectification during light load and generates a random noise spectrum which may produce EMI problems.

Siliconix' TrenchFET™ technology has resulted in 20-mΩ n-channel (Si4410DY) and 35-mΩ p-channel (Si4435DY) MOSFETs in the SO-8 surface-mount package. These LITTLE FOOT® products totally eliminate the need for an external heatsink.

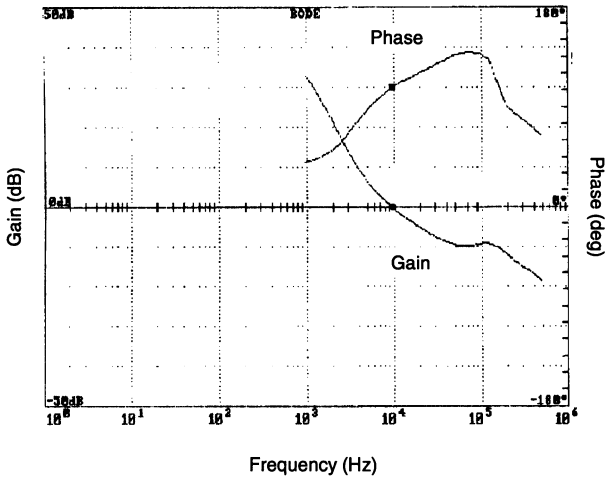


FIGURE 8. Non-Synchronous Converter BW

Worst case current of 10 A can be handled with two paralleled Si4435DY and two paralleled Si4410DY MOSFETs, which results in the efficiency levels shown in Figure 9.

Good electrical designs must provide an adequate margin for the specification, but they should not be grossly overdesigned to lower costs. LITTLE FOOT power MOSFETs allow designers to balance cost and performance considerations without sacrificing either. If the design requires only an 8.5-A continuous current, for example, one Si4410DY can be eliminated. Table 2 shows the number of MOSFETs required to handle the various output current levels of today's high-performance microprocessors. For other output power levels, the equations below should be used to calculate the power handling capability of the MOSFET.

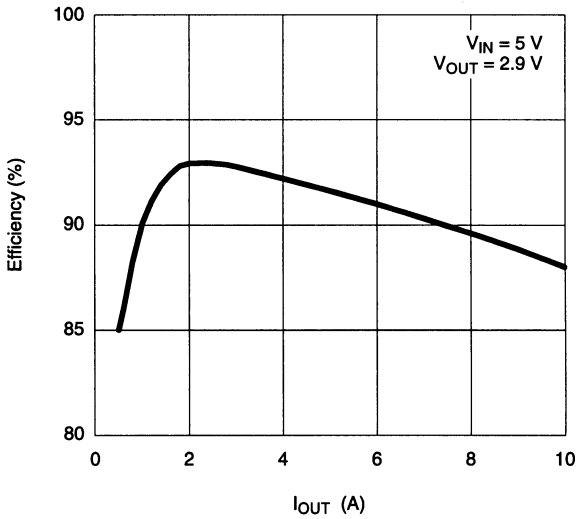


FIGURE 9. Efficiency

TABLE 2. Converter Requirements Figure 1, 2, and 3)

I_O (A) Maximum	Quantity High-side P-Channel SI4435DY	Quantity Low-side N-Channel SI4410DY	Quantity Input (C1-C3) Capacitor OS-CON 220 µF
5 A	1	1	1
8.5 A	2	1	2
10 A	2	2	2
14.5 A	3	2	3

$$P_{Dissipation\ in\ switch} = I_{RMS\ SW}{}^2 \times R_{SW} + \frac{Q_{SW} \times V_{IN} \times f_{OSC}}{2} + \frac{I_{PP} \times V_O \times \tau_C \times f_{OSC}}{2}$$

$$I_{RMS\ SW} = \sqrt{(I_{PEAK}{}^2 + I_{PP}{}^2 + I_{PEAK} \times I_{PP}) \times \frac{V_O}{3 \times V_{IN}}}$$

$$P_{Dissipation\ in\ synchronous\ rectification} = I_{RMS\ RECT}{}^2 \times R_{RECT} + \frac{Q_{RECT} \times V_{IN} \times f_{OSC}}{2}$$

$$I_{RMS\ RECT} = \sqrt{(I_{PEAK}{}^2 + I_{PP}{}^2 + I_{PEAK} \times I_{PP}) \times \frac{V_{IN} - V_O}{3 \times V_{IN}}}$$

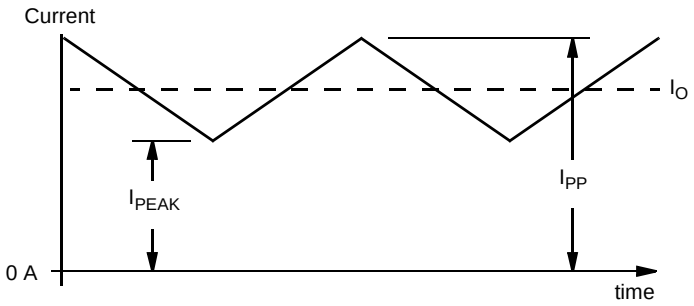
$$I_{PP} = I_{PEAK} + \Delta I$$

$$\Delta I = \frac{V_O{}^2}{L \times f_{OSC} \times V_{IN}}$$

$$I_{PEAK} = \frac{P_{IN} - (0.5 \times V_O \times \Delta I)}{V_O}$$

$$P_{IN} = \frac{V_O \times I_O}{\eta}$$

I_{RMSSW}	=	Switch rms current
R_{SW}	=	Switch on resistance
$I_{RMSRECT}$	=	Synchronous rectifier rms current
R_{RECT}	=	Synchronous rectifier on resistance
Q_{SW}	=	Total gate charge of switch
Q_{RECT}	=	Total gate charge of synchronous rectifier
V_{IN}	=	Input voltage
V_O	=	Output voltage
I_O	=	Output current
f_{OSC}	=	Switching frequency
η	=	efficiency
τ_C	=	Crossover time



INDUCTOR

The size and value of the inductor are critical in meeting overall circuit dimensional requirements and in assuring proper transient voltage regulation. The size of the core is determined by the output power, the material of the core, and the operating frequency. To handle higher output power, the core must be larger. Luckily, a higher switching frequency will lower the inductance value, decreasing the core size. However, a higher switching frequency can also mean greater core loss.

In applications where the dc flux density is high and the ac flux density swing is only 100 to 200 gauss, the core loss will be negligible compared to the wire loss. Kool Mu is the best material to use at 500 kHz to deliver 30 W in the minimum volume. Ferrite has a lower core cost and loss at this frequency, but the core size is fairly large. If the power supply is designed on the motherboard and space is not a critical issue, ferrite is a better choice.

The higher switching frequency reduces the core size by decreasing the amount of energy that must be stored between switching periods. It also accelerates the transient response to the load by decreasing the inductance value. The inductance is calculated with following equation:

$$L = \frac{V_O{}^2}{V_{IN} \times \Delta I \times f_{OSC}}$$

ΔI = desired output current ripple. Typically ΔI = 25% of maximum output current.