

## 3-A, WIDE-INPUT ADJUSTABLE SWITCHING REGULATOR

### FEATURES

- 3-A Output Current
- Wide-Input Voltage (7 V to 36 V)
- Wide-Output Voltage Adjust (2.5 V to 12.6 V)
- High Efficiency (Up to 96%)
- On/Off Inhibit
- Output Current Limit
- Overtemperature Shutdown
- Operating Temperature:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Surface Mount Package

### APPLICATIONS

- General-Purpose, Industrial Controls, HVAC Systems
- Test and Measurement, Medical Instrumentation
- AC/DC Adaptors, Vehicles, Marine, and Avionics

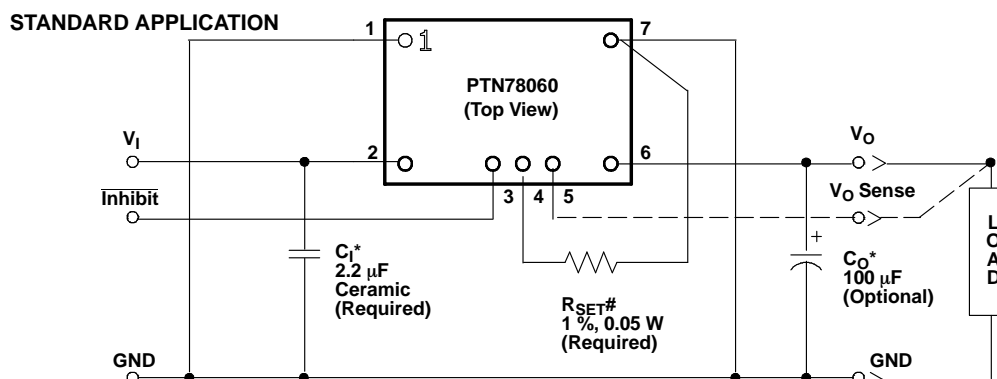


### DESCRIPTION

The PTN78060 is a series of high-efficiency, step-down integrated switching regulators (ISR), that represent the third generation in the evolution of the popular (PT)78ST200, 78ST300, (PT)78HT200, and 78HT300 series of products. In new designs, the PTN78060 series may also be considered in place of the PT6200, PT6210, and PT6300 series of single in-line pin (SIP) products. In all cases, the PTN78060 has either similar or improved electrical performance characteristics. The caseless, double-sided package has excellent thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range of 7 V to 36 V, the PTN78060 provides high-efficiency, step-down voltage conversion for loads of up to 3 A. The output voltage can be set to any value over a wide adjustment range using a single external resistor. The adjust range of the W-suffix part is 2.5 V to 12.6 V. The output voltage can be as little as 2 V lower than the input, allowing operation down to 7 V, with an output voltage of 5 V. Other features include an integral on/off inhibit. An output voltage sense ensures tight load regulation.

The PTN78060 is suited to a wide variety of general-purpose industrial applications that operate off 12-V, 24-V, or 28-V dc power.



\*See The Application Information for Capacitor Recommendation.

# $R_{SET}$  is Required to Adjust the Output Voltage Higher Than 2.5 V. See The Application Information for Values.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

PTN78060 (Basic Model)			
Output Voltage	Part Number	Description	Package Designator
2.5 V - 12.6 V	PTN78060WAH	Horizontal T/H	EUW-7
	PTN78060WAS <sup>(1)</sup>	Horizontal SMD	EUY-7

(1) Add a T suffix for tape and reel option on SMD packages.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

over operating free-air temperature range unless otherwise noted  
all voltages with respect to GND

			UNIT
T <sub>A</sub>	Operating free-air temperature	Over V <sub>I</sub> range	–40°C to 85°C
	Solder reflow temperature	Surface temperature of module body or pins	235°C
T <sub>stg</sub>	Storage temperature		–40°C to 125°C
V <sub>I</sub>	Input surge voltage, 10 ms maximum		38 V
V <sub>(inhibit)</sub>	Inhibit (pin 3) input voltage		–0.3 V to 5 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

		MIN	MAX	UNIT
V <sub>I</sub>	Input voltage	7	36	V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

**PACKAGE SPECIFICATIONS**

PTN78060x (Suffix AH and AS)			
Weight			3.9 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500 Gs <sup>(1)</sup>
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH)	20 Gs <sup>(1)</sup>
		Horizontal SMD (suffix AS)	20 Gs <sup>(1)</sup>

(1) Qualification limit.

## ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature,  $V_I = 20\text{ V}$ ,  $V_O = 5\text{ V}$ ,  $I_O = I_O(\text{max})$ ,  $C_I = 2.2\text{ }\mu\text{F}$ ,  $C_O = 100\text{ }\mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_O$	Output current	$T_A = 85^\circ\text{C}$ , natural convection airflow	0		3	A
$V_I$	Input voltage range	Over $I_O$ range	7 <sup>(1)</sup>		36 <sup>(2)</sup>	V
$V_O$	Set-point voltage tolerance	$T_A = 25^\circ\text{C}$			$\pm 2\%$ <sup>(3)</sup>	
	Temperature variation	$-40^\circ\text{C}$ to $+85^\circ\text{C}$		$\pm 0.5\%$		
	Line regulation	Over $V_I$ range		$\pm 10$		mV
	Load regulation	Over $I_O$ range		$\pm 10$		mV
	Total output voltage variation	Includes set point, line, load $-40 < T_A < 85^\circ\text{C}$			$\pm 3\%$ <sup>(3)</sup>	
$V_O(\text{adj})$	Output voltage adjust range	$V_I < 12\text{ V}$	2.5		$V_I - 2$	V
		$12\text{ V} \leq V_I \leq 15.1\text{ V}$	2.5		$V_I - 2.5$	
		$15.1\text{ V} < V_I \leq 25\text{ V}$	2.5		12.6	
		$V_I > 25\text{ V}$	$0.1 \times V_I$		12.6	
$\eta$	Efficiency	$V_I = 24\text{ V}$ , $I_O = 3\text{ A}$				
		$R_{\text{SET}} = 732\text{ }\Omega$ , $V_O = 12\text{ V}$		94%		
		$R_{\text{SET}} = 21\text{ k}\Omega$ , $V_O = 5\text{ V}$		86%		
		$R_{\text{SET}} = 78.7\text{ k}\Omega$ , $V_O = 3.3\text{ V}$		82%		
	Output voltage ripple	20-MHz bandwidth		$1\% V_O$		$V_{(\text{PP})}$
$I_{O(\text{LIM})}$	Current limit threshold	$\Delta V_O = -50\text{ mV}$		5.5		A
	Transient response	1-A/ $\mu\text{s}$ load step from 50% to 100% $I_{O(\text{max})}$				
		Recovery time		100		$\mu\text{s}$
		$V_O$ over/undershoot		5		$\%V_O$
	Inhibit control (pin 3)	Input high voltage ( $V_{\text{IH}}$ )	1		Open <sup>(4)</sup>	V
		Input low voltage ( $V_{\text{IL}}$ )	-0.1		0.3	
		Input low current ( $I_{\text{IL}}$ )		-0.25		mA
$I_{\text{I(stby)}}$	Input standby current	Pin 3 connected to GND		17		mA
$F_S$	Switching frequency	Over $V_I$ and $I_O$ ranges	440	550	660	kHz
$C_I$	External input capacitance		2.2 <sup>(5)</sup>			$\mu\text{F}$
$C_O$	External output capacitance	ceramic or nonceramic	100 <sup>(6)</sup>			$\mu\text{F}$
		ceramic			200	
		nonceramic			2,000	
		Equivalent series resistance (nonceramic)	17 <sup>(7)</sup>			m $\Omega$
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$ , ground benign	8.9			$10^6\text{ Hr}$

- (1) For output voltages less than 10 V, the minimum input voltage is 7 V or  $(V_O + 2)\text{ V}$ , whichever is greater. For output voltages of 10 V and higher, the minimum input voltage is  $(V_O + 2.5)\text{ V}$ . See the application information for further guidance.
- (2) For output voltages less than 3.6 V, the maximum input voltage is  $10 \times V_O$ . See the application information for further guidance.
- (3) The set-point voltage tolerance is affected by the tolerance and stability of  $R_{\text{SET}}$ . The stated limit is unconditionally met if  $R_{\text{SET}}$  has a tolerance of 1% with 100 ppm/ $^\circ\text{C}$  or better temperature stability.
- (4) This control pin has an internal pullup, and if left open-circuit the module operates when input power is applied. The open-circuit voltage is typically 1.5 V. A small low-leakage ( $< 100\text{ nA}$ ) MOSFET is recommended for control. See the application information for further guidance.
- (5) An external 2.2- $\mu\text{F}$  ceramic capacitor is required across the input ( $V_I$  and GND) for proper operation. Locate the capacitor close to the module.
- (6) 100  $\mu\text{F}$  of output capacitance is required for proper operation. See the application information for further guidance.
- (7) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 m $\Omega$  as the minimum when using max-ESR values to calculate.

## PIN ASSIGNMENT

### TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1, 7		This is the common ground connection for the $V_I$ and $V_O$ power connections. It is also the 0-VDC reference for the <i>Inhibit</i> and $V_O$ <i>Adjust</i> control inputs.
$V_I$	2	I	The positive input voltage power node to the module, which is referenced to common GND.
Inhibit	3	I	The Inhibit pin is an open-collector/drain active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied.
$V_O$ Adjust	4	I	A 1% resistor must be connected between this pin and GND (pin 7) to set the output voltage of the module higher than 2.5 V. If left open-circuit, the output voltage defaults to this value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 2.5 V to 12.6 V. The standard resistor value for a number of common output voltages is provided in the application information.
$V_O$ Sense	5	I	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimum voltage accuracy, $V_O$ <i>Sense</i> should be connected to $V_O$ . If the sense feature is not used, this pin may be left disconnected.
$V_O$	6	O	The regulated positive power output with respect to the GND node.

# TYPICAL CHARACTERISTICS (7-V INPUT)<sup>(1)(2)</sup>

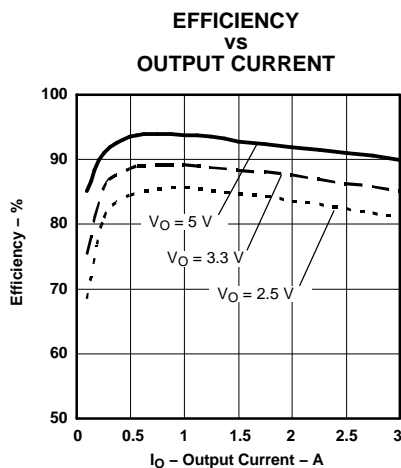


Figure 1.

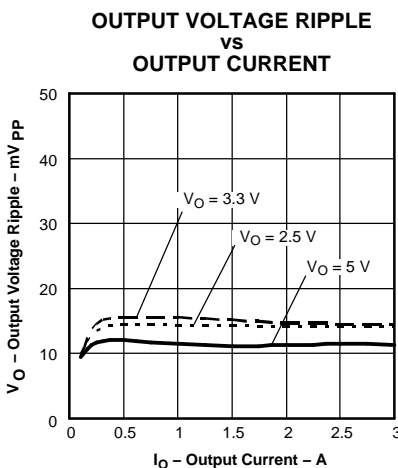


Figure 2.

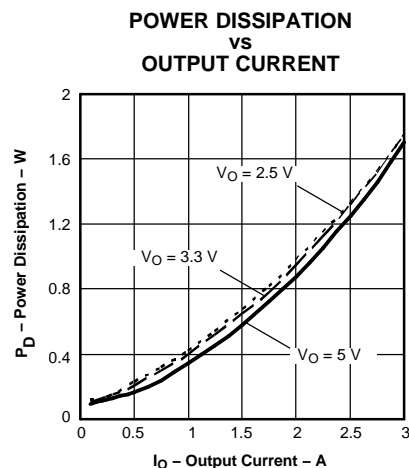


Figure 3.

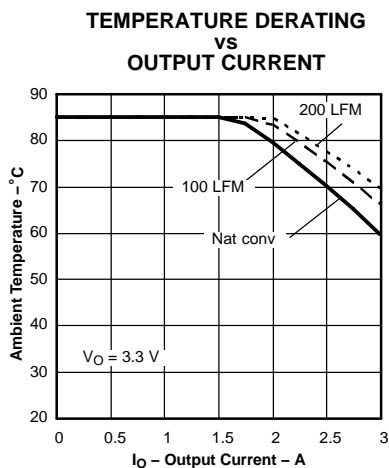


Figure 4.

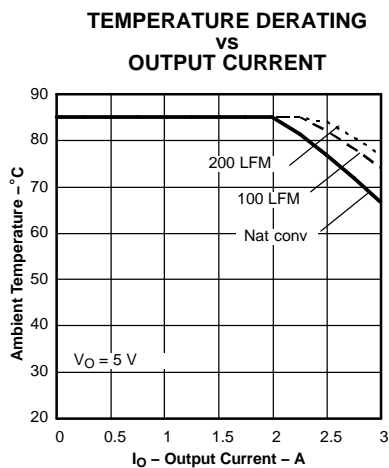


Figure 5.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 4.

# TYPICAL CHARACTERISTICS (15-V INPUT)<sup>(3)(4)</sup>

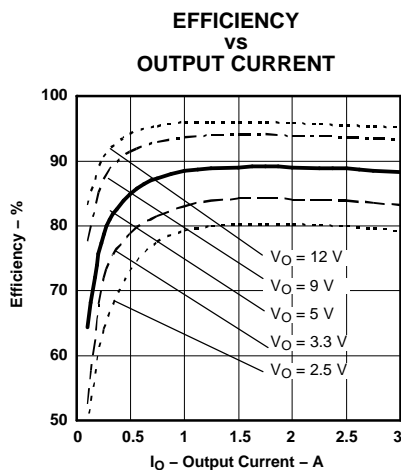


Figure 6.

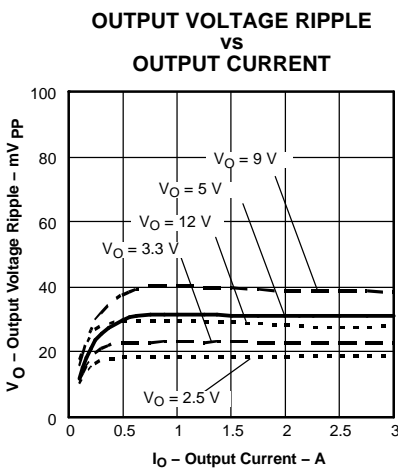


Figure 7.

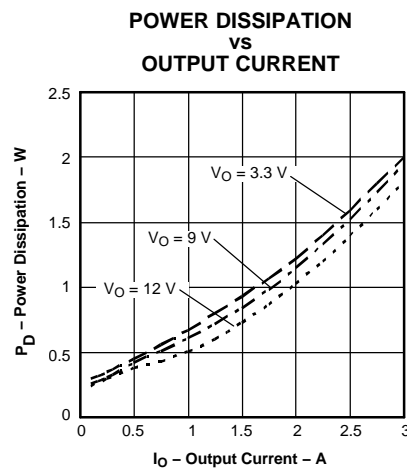


Figure 8.

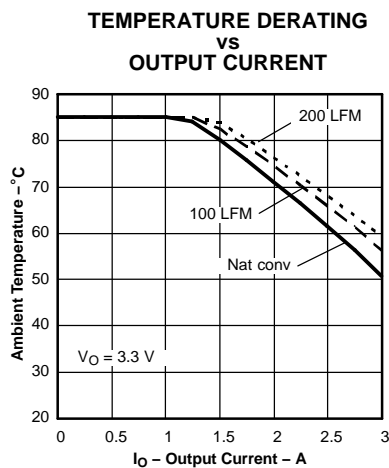


Figure 9.

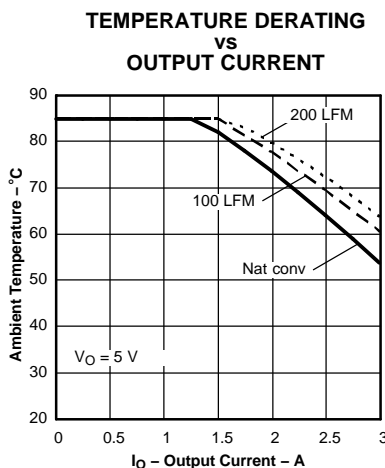


Figure 10.

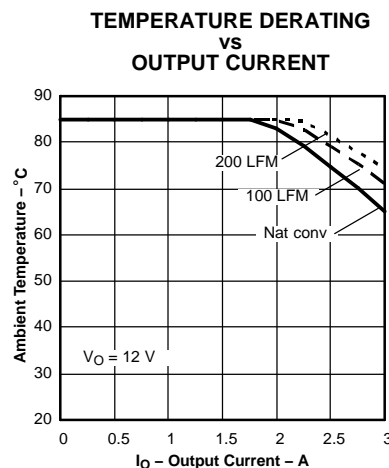
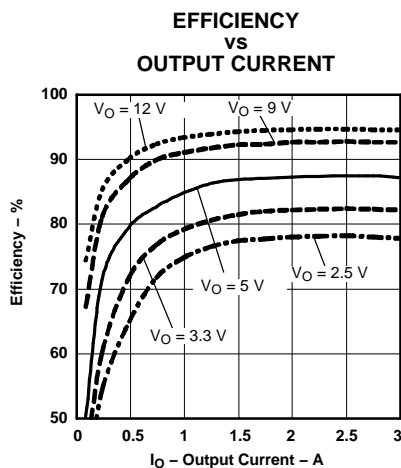


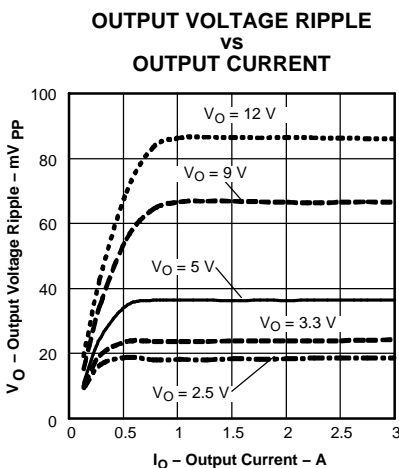
Figure 11.

- (3) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.
- (4) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 9 and Figure 10.

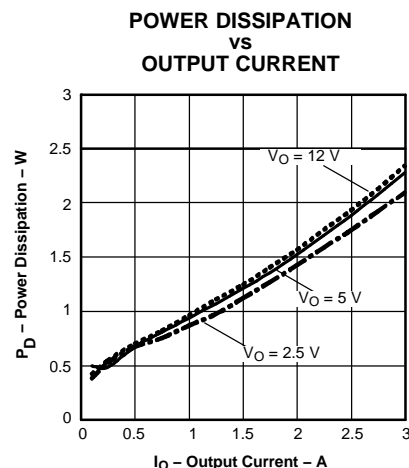
# **TYPICAL CHARACTERISTICS (24-V INPUT)<sup>(5)(6)</sup>**



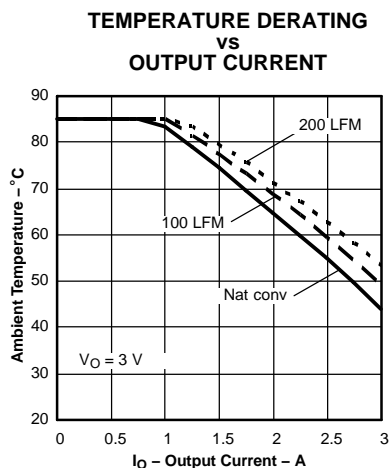
**Figure 12.**



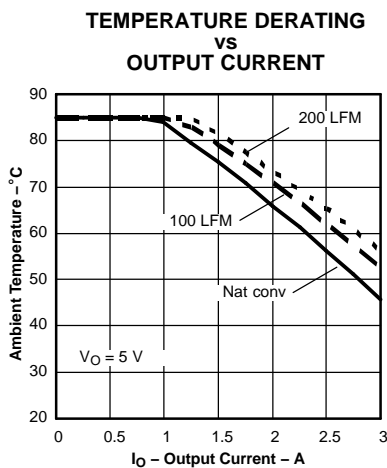
**Figure 13.**



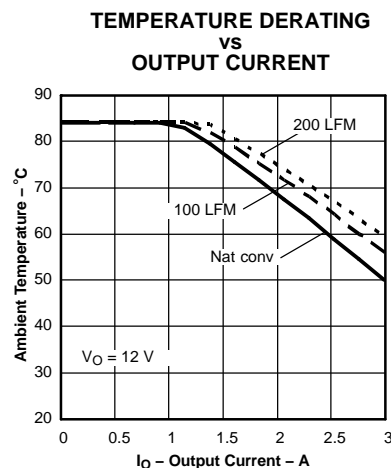
**Figure 14.**



**Figure 15.**



**Figure 16.**



**Figure 17.**

- (5) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 12, Figure 13, and Figure 14.
- (6) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 15, Figure 16, and Figure 17.

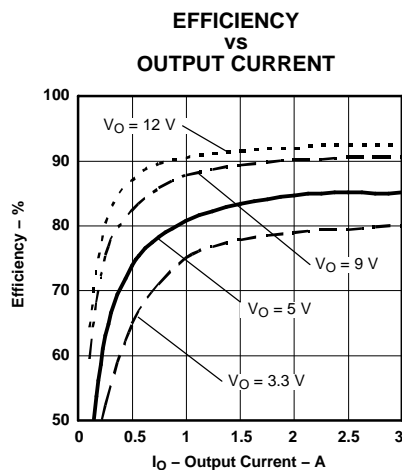
TYPICAL CHARACTERISTICS (32-V INPUT)<sup>(7)(8)</sup>

Figure 18.

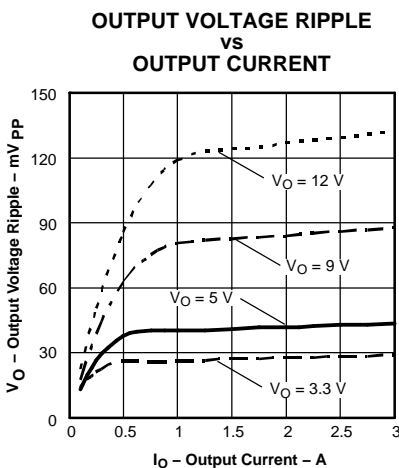


Figure 19.

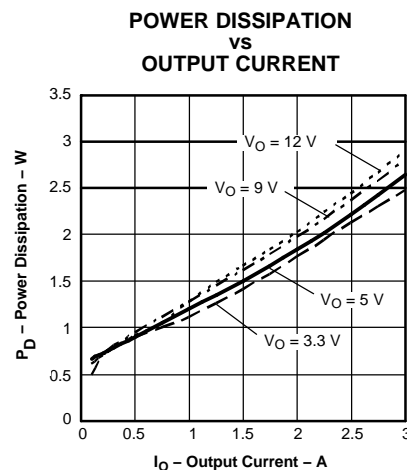


Figure 20.

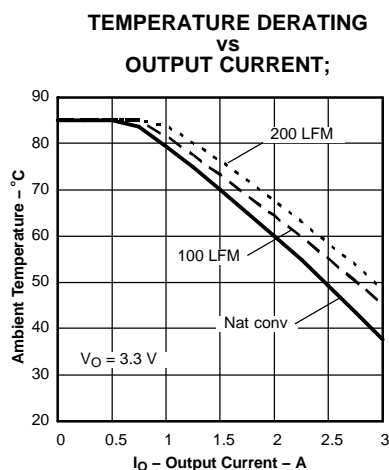


Figure 21.

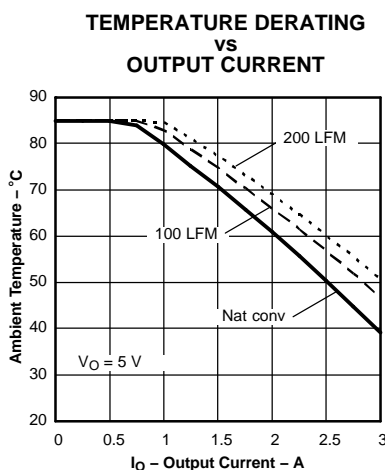


Figure 22.

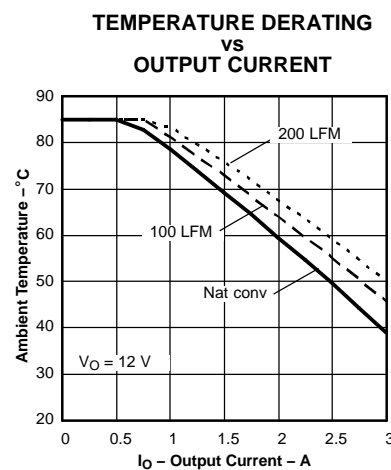


Figure 23.

- (7) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 18, Figure 19, and Figure 20.
- (8) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 21, Figure 22, and Figure 23.



## APPLICATION INFORMATION

### Adjusting the Output Voltage of the PTN78060 Wide-Output Adjust Power Modules

#### General

A resistor must be connected directly between the  $V_O$  *Adjust* control (pin 4) and the output *GND* (pin 7) to set the output voltage higher than 2.5 V. The adjustment range is from 2.5 V to 12.6 V. If pin 4 is left open, the output voltage defaults to the lowest value, 2.5 V.

Table 1 gives the standard resistor value for a number of common voltages, and with the actual output voltage that the value produces. For other output voltages, the resistor value can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 24 shows the placement of the required resistor.

$$R_{\text{set}} = 54.9 \text{ k}\Omega \times \frac{1.25 \text{ V}}{V_O - 2.5 \text{ V}} - 6.49 \text{ k}\Omega \quad (1)$$

#### Input Voltage Considerations

The PTN78060 is a step-down switching regulator. In order that the output remains in regulation, the input voltage must exceed the output by a minimum differential voltage.

Another consideration is the pulse width modulation (PWM) range of the regulator's internal control circuit. For stable operation, its operating duty cycle should not be lower than some minimum percentage. This defines the maximum advisable ratio between the regulator's input and output voltage magnitudes.

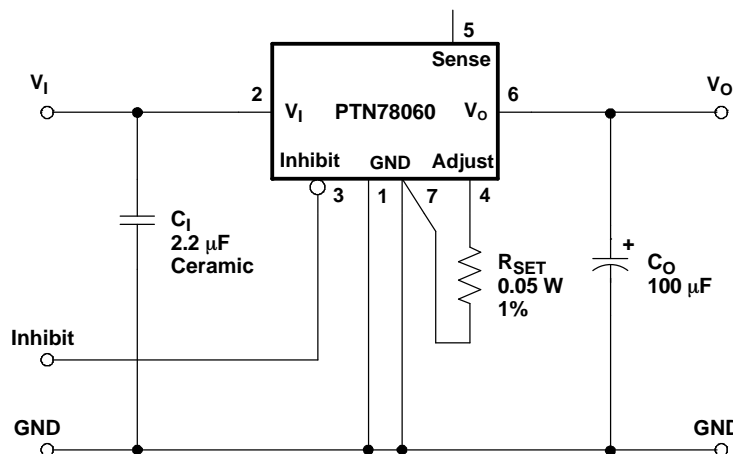
For satisfactory performance, the operating input voltage range must adhere to the following requirements.

1. For output voltages lower than 10 V, the minimum input voltage is  $(V_O + 2 \text{ V})$  or 7 V, whichever is higher.
2. For output voltages equal to 10 V and higher, the minimum input voltage is  $(V_O + 2.5 \text{ V})$ .
3. The maximum input voltage is  $(10 \times V_O)$  or 36 V, whichever is less.

As an example, Table 1 gives the operating input voltage range for the common output bus voltages. In addition, the Electrical Characteristics define the available output voltage adjust range for various input voltages.

**Table 1. Standard Values of  $R_{\text{set}}$  for Common Output Voltages**

$V_O$ (Required)	$R_{\text{SET}}$ (Standard Value)	$V_O$ (Actual)	Operating $V_I$ Range
2.5 V	Open	2.5 V	7 V to 25 V
3.3 V	78.7 k $\Omega$	3.306 V	7 V to 33 V
5 V	21 k $\Omega$	4.996 V	7 V to 36 V
12 V	732 $\Omega$	12.002 V	14.5 V to 36 V



- (1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
- (2) Never connect capacitors from  $V_O$  Adjust to either GND or  $V_O$ . Any capacitance added to the  $V_O$  Adjust pin affects the stability of the regulator.

Figure 24.  $V_O$  Adjust Resistor Placement

Table 2. Output Voltage Set-Point Resistor Values

$V_O$ Required	$R_{SET}$	$V_O$ Required	$R_{SET}$	$V_O$ Required	$R_{SET}$	$V_O$ Required	$R_{SET}$
2.50 V	Open	3.7 V	50.7 k $\Omega$	6.1 V	12.6 k $\Omega$	9.0 V	4.07 k $\Omega$
2.55 V	1.37 M $\Omega$	3.8 V	46.3 k $\Omega$	6.2 V	12.1 k $\Omega$	9.2 V	3.75 k $\Omega$
2.60 V	680 k $\Omega$	3.9 V	42.5 k $\Omega$	6.3 V	11.6 k $\Omega$	9.4 V	3.46 k $\Omega$
2.65 V	451 k $\Omega$	4.0 V	39.3 k $\Omega$	6.4 V	11.1 k $\Omega$	9.6 V	3.18 k $\Omega$
2.70 V	337 k $\Omega$	4.1 V	36.4 k $\Omega$	6.5 V	10.7 k $\Omega$	9.8 V	2.91 k $\Omega$
2.75 V	268 k $\Omega$	4.2 V	33.9 k $\Omega$	6.6 V	10.2 k $\Omega$	10.0 V	2.66 k $\Omega$
2.80 V	222 k $\Omega$	4.3 V	31.6 k $\Omega$	6.7 V	9.85 k $\Omega$	10.2 V	2.42 k $\Omega$
2.85 V	190 k $\Omega$	4.4 V	29.6 k $\Omega$	6.8 V	9.47 k $\Omega$	10.4 V	2.20 k $\Omega$
2.90 V	165 k $\Omega$	4.5 V	27.8 k $\Omega$	6.9 V	9.11 k $\Omega$	10.6 V	1.98 k $\Omega$
2.95 V	146 k $\Omega$	4.6 V	26.2 k $\Omega$	7.0 V	8.76 k $\Omega$	10.8 V	1.78 k $\Omega$
3.00 V	131 k $\Omega$	4.7 V	24.7 k $\Omega$	7.1 V	8.43 k $\Omega$	11.0 V	1.58 k $\Omega$
3.05 V	118 k $\Omega$	4.8 V	23.3 k $\Omega$	7.2 V	8.11 k $\Omega$	11.2 V	1.40 k $\Omega$
3.10 V	108 k $\Omega$	4.9 V	22.1 k $\Omega$	7.3 V	7.81 k $\Omega$	11.4 V	1.22 k $\Omega$
3.15 V	99.1 k $\Omega$	5.0 V	21.0 k $\Omega$	7.4 V	7.52 k $\Omega$	11.6 V	1.05 k $\Omega$
3.20 V	91.5 k $\Omega$	5.1 V	19.9 k $\Omega$	7.5 V	7.24 k $\Omega$	11.8 V	889 $\Omega$
3.25 V	85.0 k $\Omega$	5.2 V	18.9 k $\Omega$	7.6 V	6.97 k $\Omega$	12.0 V	734 $\Omega$
3.30 V	79.3 k $\Omega$	5.3 V	18.0 k $\Omega$	7.7 V	6.71 k $\Omega$	12.2 V	585 $\Omega$
3.35 V	74.2 k $\Omega$	5.4 V	17.2 k $\Omega$	7.8 V	6.46 k $\Omega$	12.4 V	442 $\Omega$
3.40 V	69.8 k $\Omega$	5.5 V	16.4 k $\Omega$	7.9 V	6.22 k $\Omega$	12.6 V	305 $\Omega$
3.45 V	65.7 k $\Omega$	5.6 V	15.6 k $\Omega$	8.0 V	5.99 k $\Omega$		
3.50 V	62.1 k $\Omega$	5.7 V	15.0 k $\Omega$	8.2 V	5.55 k $\Omega$		
3.55 V	58.9 k $\Omega$	5.8 V	14.3 k $\Omega$	8.4 V	5.14 k $\Omega$		
3.60 V	55.9 k $\Omega$	5.9 V	13.7 k $\Omega$	8.6 V	4.76 k $\Omega$		
3.65 V	53.2 k $\Omega$	6.0 V	13.1 k $\Omega$	8.8 V	4.40 k $\Omega$		

## **CAPACITOR RECOMMENDATIONS for the PTN78060 WIDE-OUTPUT ADJUST POWER MODULES**

### **Input Capacitor**

The minimum requirement for the input is 2.2  $\mu\text{F}$  of ceramic capacitance, in either an X5R or X7R temperature characteristic. Ceramic capacitors should be located within 0.5 inches (1.27 cm) of the regulator's input pins. Electrolytic capacitors can be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for any nonceramic capacitance must be at least 500 mA rms for  $V_O \leq 5.5$  V. For  $V_O > 5.5$  V, the minimum ripple current rating is 750 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input. This ripple current requirement can be reduced by placing more ceramic capacitors at the input, in addition to the minimum required 2.2  $\mu\text{F}$ .

Tantalum capacitors are not recommended for use at the input bus, as none were found to meet the minimum voltage rating of  $2 \times$  (maximum dc voltage + ac ripple). The  $2\times$  rating is standard practice for regular tantalum capacitors to ensure reliability. Polymer-tantalum capacitors are more reliable, and are available with a maximum rating of typically 20 V. These can be used with input voltages up to 16 V.

### **Output Capacitor**

The minimum capacitance required to ensure stability is a 100- $\mu\text{F}$  capacitor. Either ceramic or electrolytic-type capacitors can be used. The minimum ripple current rating for the nonceramic capacitance must be at least 150 mA rms. The stability of the module and voltage tolerances will be compromised if the capacitor is not placed near the output bus pins. A high-quality computer-grade electrolytic capacitor should be adequate. A ceramic capacitor can also be located within 0.5 inches (1.27 cm) of the output pin.

For applications with load transients (sudden changes in load current), the regulator response improves with additional capacitance. Additional electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 m $\Omega$  (17 m $\Omega$  using the manufacturer's maximum ESR for a single capacitor). A list of capacitors and vendors are identified in Table 3, the recommended capacitor table.

### **Ceramic Capacitors**

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further reduce the reflected input ripple current, or improve the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR, and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 200  $\mu\text{F}$ . Also, to prevent the formation of local resonances, do not place more than three identical ceramic capacitors with values of 10  $\mu\text{F}$  or greater in parallel.

### **Tantalum Capacitors**

Tantalum-type capacitors may be used at the output and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

## Capacitor Table

The capacitor table, Table 3, identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

## Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/μs. The typical voltage deviation for this load transient is given in the data sheet specification table using the required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation of any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

**Table 3. Recommended Input/Output Capacitors**

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (μF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (I <sub>RMS</sub> ) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Panasonic WA (SMD)	20	150	0.026	32500	10 × 10,2	1 <sup>(1)</sup>	≤ 2	EEFWA1D151P (V <sub>I</sub> < 16 V)
FC( Radial)	50	180	0.119	850	10 × 16	1	1	EEUFC1H181
FC (SMD)	35	100	0.015	670	10 × 10,2	1 <sup>(1)</sup>	1	EEVFC1V101P (V <sub>O</sub> ≤ 5.5 V)
United Chemi-Con PXA (SMD)	16	180	0.016	4360	8 × 12	1 <sup>(1)</sup>	≤ 1	PXA16VC180MF60 (V <sub>I</sub> < 14 V)
FS	20	150	0.024	3200	8 × 10,5	1 <sup>(1)</sup>	≤ 2	10FS100M (V <sub>I</sub> < 16 V)
LXZ	35	220	0.090	760	10 × 12,5	1 <sup>(1)</sup>	1	LXZ35VB221M10X12LL (V <sub>I</sub> < 32 V)
MVY(SMD)	50	100	0.300	500	10 × 10	1	1	MVY50VC101M10X10TP (V <sub>O</sub> ≤ 5.5 V)
Nichicon UWG (SMD)	50	100	0.300	500	10 × 10	1	1	UWG1H101MNR1GS (V <sub>O</sub> ≤ 5.5 V)
F550 (Tantalum)	10	100	0.055	2000	7,7 × 4,3	N/R <sup>(1)</sup>	≤ 3 <sup>(2)</sup>	F551A107MN (V <sub>O</sub> ≤ 5 V)
HD	50	120	0.072	979	10 × 12,5	1	1	UHD1H151MHR
Sanyo Os-Con SVP (SMD)	20	100	0.024	2500	8 × 12	1 <sup>(1)</sup>	≤ 2	20SVP100M (V <sub>I</sub> ≤ 16 V)
SP	16	100	0.032	2890	10 × 5	1 <sup>(1)</sup>	≤ 2	16SP100M (V <sub>I</sub> ≤ 14 V)
AVX Tantalum TPS (SMD)	20	100	0.085	1543	7,3 L × 4,3 W × 4,1 H	N/R <sup>(3)</sup>	≤ 3	TPSV107M020R0085 (V <sub>O</sub> ≤ 10 V)
	20	100	0.200	> 817		N/R <sup>(3)</sup>	≤ 3	TPSE107M020R0200 (V <sub>O</sub> ≤ 10 V)
Murata X5R Ceramic	6.3	100	0.002	>1000	1210 case	N/R <sup>(1)</sup>	≤ 2	GRM32ER60J107M (V <sub>O</sub> ≤ 5.5 V)
TDK X5R Ceramic	6.3	100	0.002	>1000	3225	N/R <sup>(1)</sup>	≤ 2	C3225X5R0J107MT (V <sub>O</sub> ≤ 5.5 V)
Murata X5R Ceramic	16	47	0.002	>1000	1210 case	1 <sup>(1)</sup>	≤ 4	GRM32ER61C476M (V <sub>O</sub> ~ V <sub>I</sub> ≤ 13.5 V)

- (1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
- (2) The maximum voltage rating of the capacitor must be selected for the desired set-point voltage (V<sub>O</sub>). To operate at a higher output voltage select a capacitor with a higher voltage rating.
- (3) Not recommended (N/R). The voltage rating does not meet the minimum operating limits in most applications.

**Table 3. Recommended Input/Output Capacitors (continued)**

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE ( $\mu$ F)	EQUIVALENT SERIES RESISTANCE (ESR) ( $\Omega$ )	85°C MAXIMUM RIPPLE CURRENT (I <sub>RMS</sub> ) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Kemet X5R Ceramic	6.3	47	0.002	>1000	1210 case	N/R <sup>(1)</sup>	≤ 4	C1210C476K9PAC (V <sub>O</sub> ≤ 5.5 V)
TDK X5R Ceramic	6.3	47	0.002	>1000	3225	N/R <sup>(1)</sup>	≤ 4	C3225X5R0J476MT (V <sub>O</sub> ≤ 5.5 V)
Murata X5R Ceramic	6.3	47	0.002	>1000	3225	N/R <sup>(1)</sup>	≤ 4	GRM422X5R476M6.3 (V <sub>O</sub> ≤ 5.5 V)
TDK X7R Ceramic	25	2.2	0.002	>1000	SMD	≥ 1 <sup>(4)</sup>	1	C3225X7R0J225KT/MT (V <sub>O</sub> ≤ 20 V)
Murata X7R Ceramic	25	2.2	0.002	>1000	1210 case	≥ 1 <sup>(4)</sup>	1	GRM32RR71J225K (V <sub>O</sub> ≤ 20 V)
Kemet X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 1 <sup>(4)</sup>	1	C1210C225K3RAC (V <sub>O</sub> ≤ 20 V)
AVX X7R Ceramic	25	2.2	0.002	>1000		≥ 1 <sup>(4)</sup>	1	C1210C225KAT2A (V <sub>O</sub> ≤ 20 V)
Kemet X7R Ceramic	50	1.0	0.002	>1000	SMD	≥ 2 <sup>(5)</sup>	1	C1210C105K5RAC
Murata X7R Ceramic	50	4.7	0.002	>1000		≥ 1	1	GRM32ER71H475KA88L
TDK X7R Ceramic	50	2.2	0.002	>1000		≥ 1	1	C3225X7R1H225KT
Murata X7R Ceramic	50	1.0	0.002	>1000	1210 case	≥ 2 <sup>(5)</sup>	1	GRM32RR71H105KA01L
TDK X7R Ceramic	50	1.0	0.002	>1000	3225	≥ 2 <sup>(5)</sup>	1	C3225X7R1H105KT
Kemet Radial Through-hole	50	1.0	0.002	>1000	5,08 × 7,62 × 9,14 H	≥ 2 <sup>(5)</sup>	1	C330C105K5R5CA
Murata Radial Through-hole	50	2.2	0.004	>1000	10 H × 10 W × 4 D	≥ 1	1	RPER71H2R2KK6F03

(4) The maximum rating of the ceramic capacitor limits the regulator's operating input voltage to 20 V. Select an alternative ceramic component to operate at a higher input voltage.

(5) A total capacitance of 2  $\mu$ F is an acceptable replacement value for a single 2.2- $\mu$ F ceramic capacitor

## Power-Up Characteristics

When configured per the standard application, the PTN78060 power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay (typically 5–10 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 25 shows the power-up waveforms when operating from a 12-V input and with the output voltage adjusted to 5 V. The waveforms were measured with a 2.8-A resistive load.

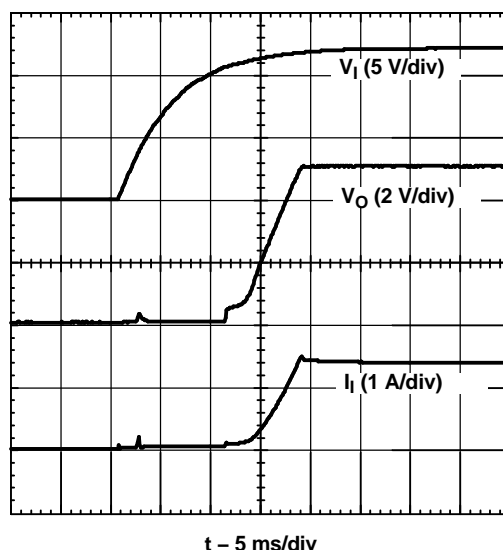


Figure 25. Power-Up Waveforms

## Current Limit Protection

The module is protected against load faults with a continuous current limit characteristic. Under a load-fault condition, the output current increases to the current limit threshold. Attempting to draw current that exceeds the current limit threshold causes the module to progressively reduce its output voltage. Current is continuously supplied to the fault until the fault is removed. Once it is removed, the output voltage promptly recovers. When limiting output current, the regulator experiences higher power dissipation, which increases its temperature. If the temperature increase is excessive, the module overtemperature protection begins to periodically turn the output voltage off.

## Overtemperature Protection

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current limit condition. If the internal temperature rises excessively, the module turns itself off, reducing the output voltage to zero. The module exercises a soft-start power up when the sensed temperature has decreased by about 10°C below the trip point.

**NOTE:** Overtemperature protection is a last resort mechanism to prevent damage to the module. It should not be relied on as permanent protection against thermal stress. Always operate the module within its temperature derated limits, for the worst case operating conditions of output current, ambient temperature, and airflow. Operating the module above these limits, albeit below the thermal shutdown temperature, reduces the long-term reliability of the module.

## Output Voltage Sense

An external voltage sense improves the load regulation performance of the module by enabling it to compensate for any IR-voltage drop between the module and the load circuit. This voltage drop is caused by the flow of current through the resistance in the printed-circuit board connections.

To use the output voltage sense feature, simply connect the  $V_O$  Sense input (pin 5) to  $V_O$ , close to the device that draws the most supply current. If an external voltage sense is not desired, the  $V_O$  Sense input may be left open circuit. An internal resistor ( $15\ \Omega$  or less), connected between this input and  $V_O$ , ensures that the output remains in regulation.

With  $V_O$  Sense connected, the difference between the voltage measure directly between the  $V_O$  and  $GND$ , and that measured from  $V_O$  Sense to  $GND$ , represents the amount of IR-voltage drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

**Note:** The external voltage sense is not designed to compensate for the forward drop of nonlinear or frequency-dependent components that may be placed in series with the regulator's output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the external sense connection, they are effectively placed inside the regulation control loop. This can adversely affect the stability of the module.

## Output On/Off Inhibit

The inhibit feature can be used wherever there is a requirement for the output voltage to be turned off. The power module functions normally when the Inhibit control (pin 3) is left open-circuit, providing a regulated output whenever a valid source voltage is connected to  $V_I$  with respect to  $GND$ . Figure 26 shows the circuit used to demonstrate the inhibit function. Note the discrete transistor (Q1). Turning Q1 on applies a low voltage to the *Inhibit* control pin and turns the module off. The output voltage decays as the load circuit discharges the capacitance. The current drawn at the input is reduced to typically 17 mA. If Q1 is then turned off, the module executes a soft-start power up. A regulated output voltage is produced within 20 ms. Figure 27 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the fall in the waveform, Q1 Vgs. The waveforms were measured with a 2.8-A resistive load.

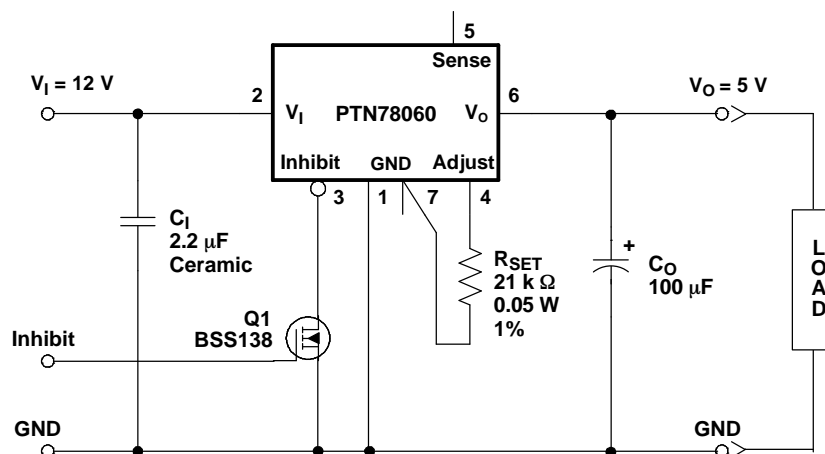
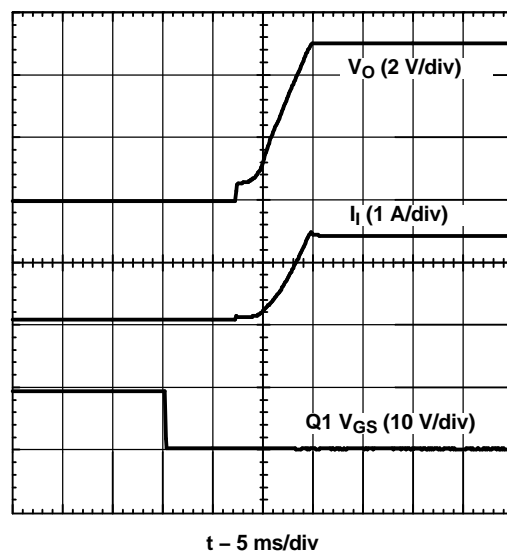


Figure 26. On/Off Inhibit Control Circuit

**Figure 27. Power-Up Response From Inhibit Control**



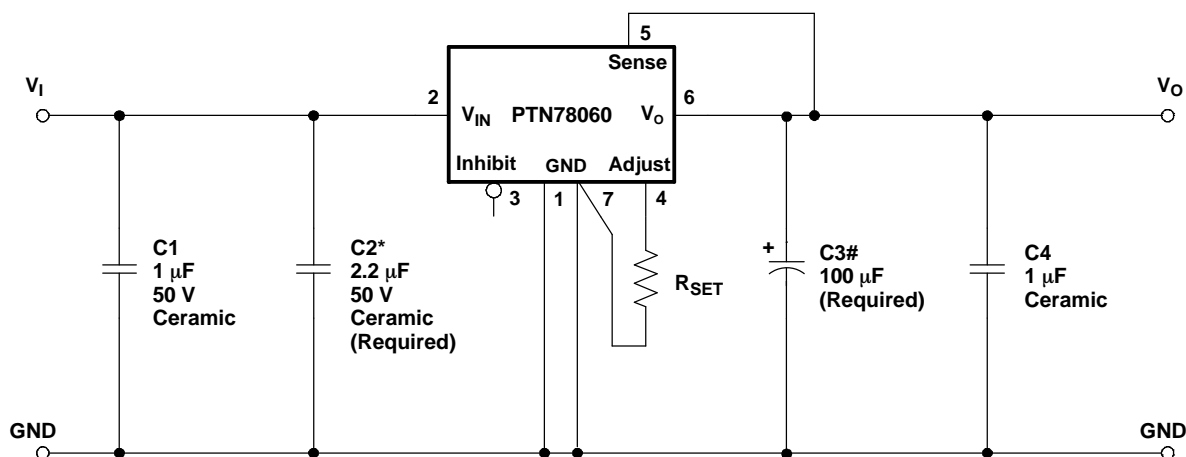
## Optional Input/Output Filters

Power modules include internal input and output ceramic capacitors in all of their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

### Input/Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more 1- $\mu$ F ceramic capacitors, such as C4 shown in Figure 28. Ceramic capacitors should be placed close to the output power terminals. A single 1- $\mu$ F capacitor reduces the output ripple/noise by 10% to 30% for modules with a rated output current of less than 3 A. (Note: C3 is recommended to improve the regulators transient response, and does not reduce output ripple and noise.)

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of C1, minimum 1- $\mu$ F ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by up to 20%.



\* See specifications for required value and type.

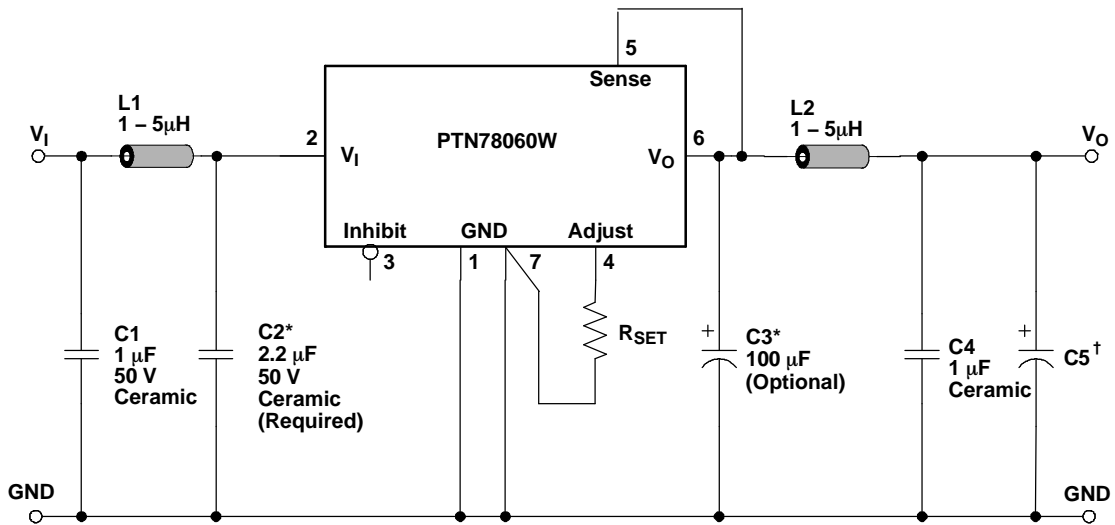
# See Application Information for suggested value and type.

**Figure 28. Adding High-Frequency Bypass Capacitors To The Input and Output**

### $\pi$ Filters

If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A  $\pi$  (pi) filter, employing a ferrite bead (Fair-Rite Pt. No. 2673000701 or equivalent) in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 29 and Figure 30). In order for the inductor to be effective ceramic capacitors are also required. (Note: see Capacitor Recommendations for additional information on vendors and component suggestions).

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency (650 kHz - 1 MHz). The placement of this filter is critical. It must be located as close as possible to the input or output pins to be effective. The ferrite bead is small (12,5 mm  $\times$  3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite also manufactures a surface-mount bead (Pt. No. 2773021447). It is rated to 5 A, and can be used on the output bus. As an alternative, suitably rated 1- $\mu$ H to 5- $\mu$ H wound inductors can be used in place of the ferrite inductor bead.

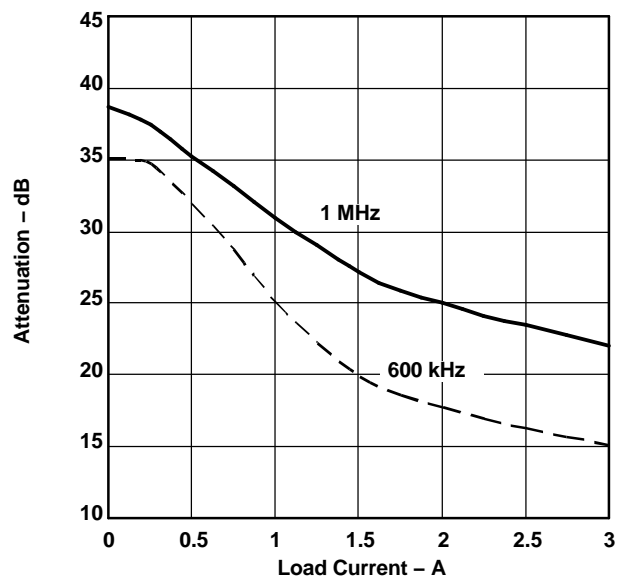


\* See specifications for required value and type.

# See Application Information for suggested value and type.

† Recommended whenever  $I_O$  is greater than 2 A.

**Figure 29. Adding  $\pi$  Filters ( $I_O \leq 3$  A)**



**Figure 30.  $\pi$ -Filter Attenuation vs. Load Current**

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