
Document Title

256Kx36 & 512Kx18-Bit Synchronous Burst SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	April. 10 . 1998	Preliminary
0.1	Change DC Characteristics. ISB value from 60mA to 90mA at -8 ISB value from 50mA to 80mA at -9 ISB value from 40mA to 70mA at -10 ISB1 value from 10mA to 30mA ISB2 value from 10mA to 30mA	Aug. 31. 1998	Preliminary
0.2	1. Changed tcd from 8.0ns to 8.5ns at -8 2. Changed tcyc from 13.0ns to 12.0ns at -10 3. Changed DC condition at Icc and parameters Icc ; from 300mA to 350mA at -8, from 260mA to 300mA at -9, from 220mA to 260mA at -10, ISB ; from 90mA to 130mA at -8, from 80mA to 120mA at -9, from 70mA to 110mA at -10,	Sep. 09. 1998	Preliminary
0.3	1. Add 119BGA(7x17 Ball Grid Array Package) . 2. Add x32 organization.	Oct. 15. 1998	Preliminary
0.4	Add VDDQ Supply voltage(2.5V)	Dec. 10. 1998	Preliminary
0.5	Changed Vol Max value from 0.2V to 0.4V at 2.5V I/O.	Dec. 23. 1998	Preliminary
1.0	1. Final Spec Release. 2. Remove x32 organization.	Jan. 29. 1999	Final
2.0	1. Remove VDDQ supply voltage(2.5V)	Feb. 25. 1999	Final
3.0	1. Changed Icc from 350mA to 330mA at -8. 2. Add bin -7. (tCD 7.5ns).	Mar. 30. 1999	Final
4.0	1. Add VDDQ supply voltage(2.5V)	May. 13. 1999	Final
5.0	1. Changed tCYC from 12ns to 10ns at -9.	Nov. 19. 1999	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

256Kx36 & 512Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package)

FAST ACCESS TIMES

PARAMETER	Symbol	-75	-85	-90	-10	Unit
Cycle Time	tcyc	8.5	10	10	12	ns
Clock Access Time	tcd	7.5	8.5	9.0	10.0	ns
Output Enable Access Time	toe	3.5	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B803625M and K7B801825M are 9,437,184-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 256K(512K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, $\overline{ZZ}$. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

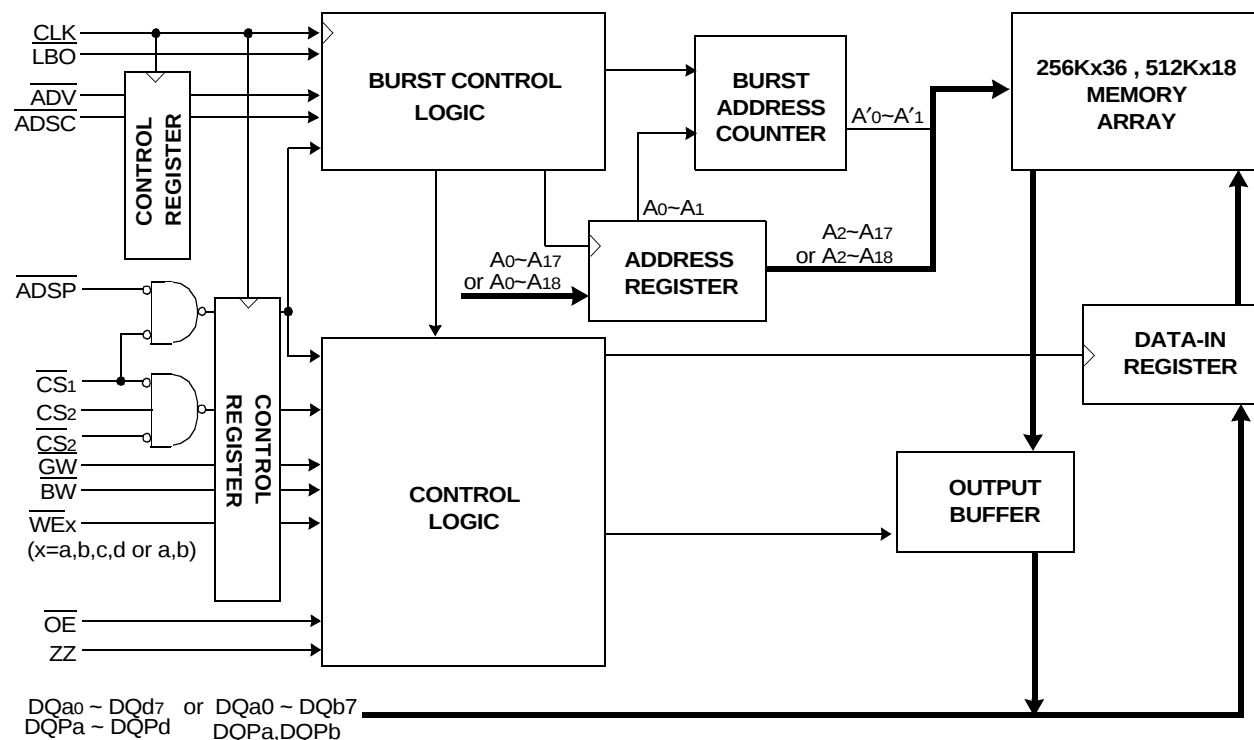
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

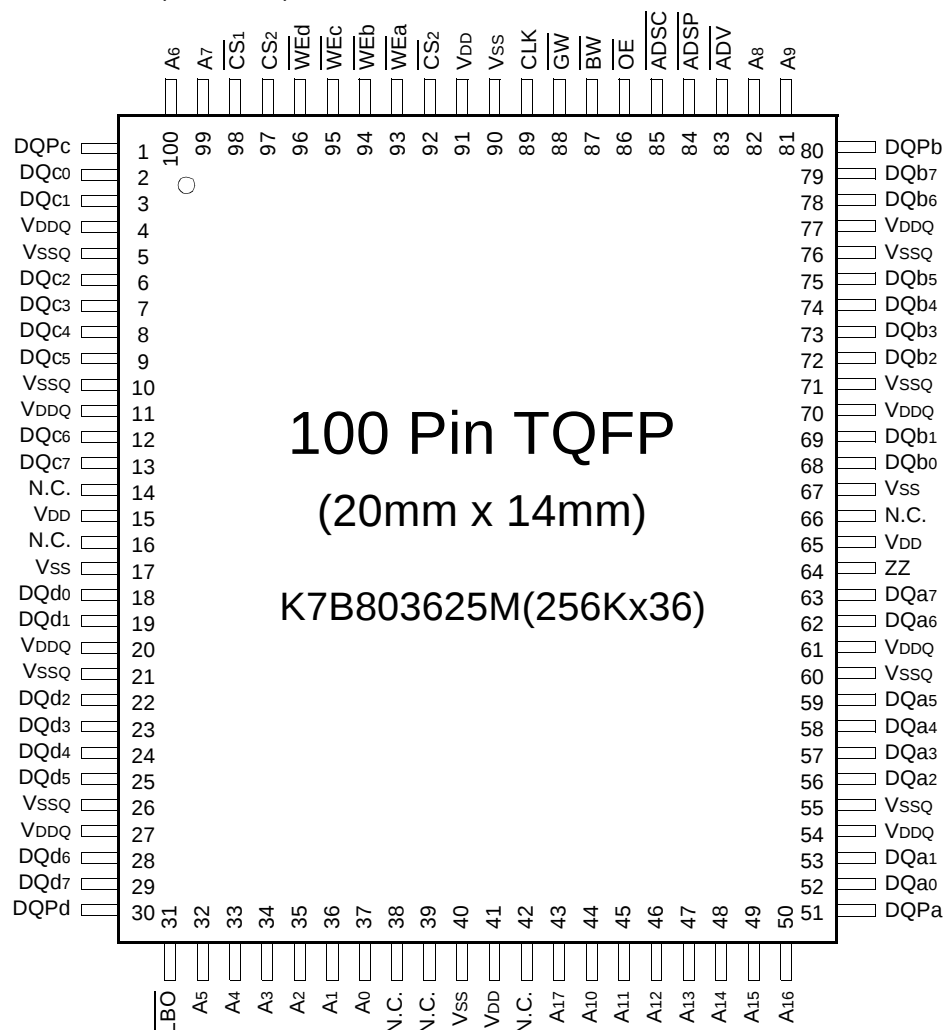
$\overline{ZZ}$ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B803625M and K7B801825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP and 119BGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

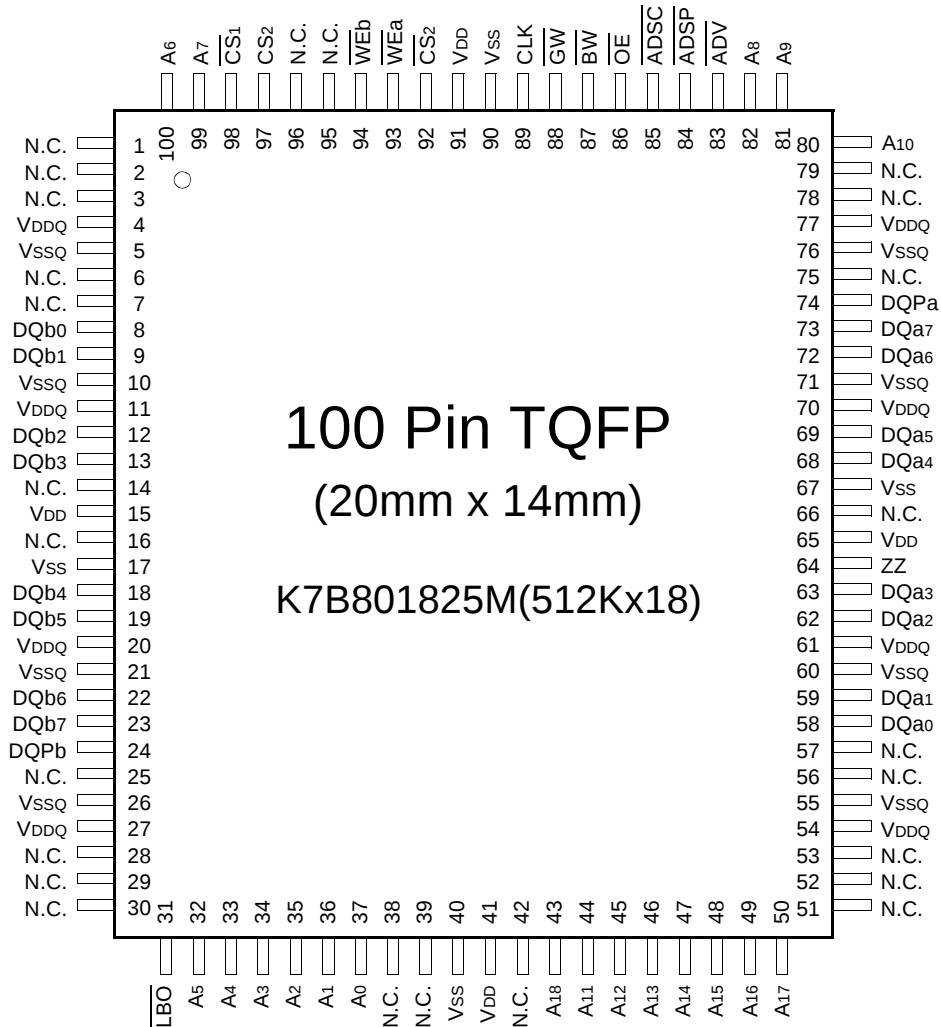


PIN

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,66
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSP	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	92	VSSQ	Output Ground	5,10,21,26,55,60,71,76
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,43 44,45,46,47,48,49,50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,39,42,51,52,53,56, 57,66,75,78,79,95,96
ADV	Burst Address Advance	83	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
ADSP	Address Status Processor	84	DQb0 ~ b7		8,9,12,13,18,19,22,23
ADSC	Address Status Controller	85	DQPa, Pb		74,24
CLK	Clock	89	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS1	Chip Select	98	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	97			
CS2	Chip Select	92			
WE _x	Byte Write Inputs	93,94			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
2. The pin 42 is reserved for address bit for the 16Mb .

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B803625M(256Kx36)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	$\overline{\text{ADSP}}$	A	A	V _{DDQ}
B	NC	CS ₂	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _c	DQP _c	V _{SS}	NC	V _{SS}	DQP _b	DQ _b
E	DQ _c	DQ _c	V _{SS}	$\overline{\text{CS}}_1$	V _{SS}	DQ _b	DQ _b
F	V _{DDQ}	DQ _c	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQ _b	V _{DDQ}
G	DQ _c	DQ _c	$\overline{\text{WE}}_c$	$\overline{\text{ADV}}$	$\overline{\text{WE}}_b$	DQ _b	DQ _b
H	DQ _c	DQ _c	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQ _b	DQ _b
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQ _d	DQ _d	V _{SS}	CLK	V _{SS}	DQ _a	DQ _a
L	DQ _d	DQ _d	$\overline{\text{WE}}_d$	NC	$\overline{\text{WE}}_a$	DQ _a	DQ _a
M	V _{DDQ}	DQ _d	V _{SS}	$\overline{\text{BW}}$	V _{SS}	DQ _a	V _{DDQ}
N	DQ _d	DQ _d	V _{SS}	A ₁ *	V _{SS}	DQ _a	DQ _a
P	DQ _d	DQP _d	V _{SS}	A ₀ *	V _{SS}	DQP _a	DQ _a
R	NC	A	$\overline{\text{LBO}}$	V _{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply(+3.3V)
A ₀ , A ₁	Burst Count Address	V _{SS}	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQ _a	Data Inputs/Outputs
CLK	Clock	DQ _b	Data Inputs/Outputs
CS ₁	Chip Select	DQ _c	Data Inputs/Outputs
CS ₂	Chip Select	DQ _d	Data Inputs/Outputs
WE _x	Byte Write Inputs	DQP _a ~Pd	Data Inputs/Outpus
(x=a,b,c,d)			
$\overline{\text{OE}}$	Output Enable	V _{DDQ}	Output Power Supply
$\overline{\text{GW}}$	Global Write Enable		(2.5V or 3.3V)
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
LBO	Burst Mode Control		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B801825M(512Kx18)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	$\overline{\text{ADSP}}$	A	A	V _{DDQ}
B	NC	CS ₂	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _b	NC	V _{SS}	NC	V _{SS}	DQ _{Pa}	NC
E	NC	DQ _b	V _{SS}	$\overline{\text{CS}}_1$	V _{SS}	NC	DQ _a
F	V _{DDQ}	NC	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQ _a	V _{DDQ}
G	NC	DQ _b	$\overline{\text{WE}}_b$	$\overline{\text{ADV}}$	V _{SS}	NC	DQ _a
H	DQ _b	NC	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQ _a	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQ _b	V _{SS}	CLK	V _{SS}	NC	DQ _a
L	DQ _b	NC	V _{SS}	NC	$\overline{\text{WE}}_a$	DQ _a	NC
M	V _{DDQ}	DQ _b	V _{SS}	$\overline{\text{BW}}$	V _{SS}	NC	V _{DDQ}
N	DQ _b	NC	V _{SS}	A ₁ *	V _{SS}	DQ _a	NC
P	NC	DQ _{Pb}	V _{SS}	A ₀ *	V _{SS}	NC	DQ _a
R	NC	A	$\overline{\text{LBO}}$	V _{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	V _{SS}	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQ _a	Data Inputs/Outputs
CLK	Clock	DQ _b	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	DQ _{Pa~Pb}	Data Inputs/Outputs
CS ₂	Chip Select		
$\overline{\text{WE}}_x$	Byte Write Inputs	V _{DDQ}	Output Power Supply
(x=a,b)			(2.5V or 3.3V)
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable		
$\overline{\text{BW}}$	Byte Write Enable		
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		

FUNCTION DESCRIPTION

The K7B803625M and K7B801825M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When $\overline{ZZ}$ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling $\overline{GW}$ (independent of $\overline{BW}$ and $\overline{WEx}$), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B803625M, a 256Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQ Pb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQ Pc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQ Pd.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{\text{OE}}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with OE, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.3 to 4.6	V
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.5	V
Power Dissipation	PD	1.4	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE* (TA=25°C, f=1MHz)

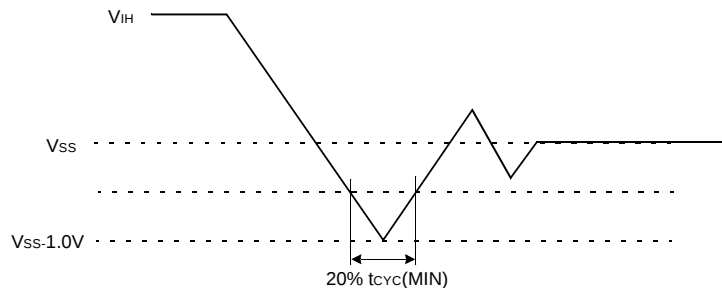
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	6	pF
Output Capacitance	COUT	VOU=0V	-	8	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	$V_{DD}=Max$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled, $V_{out}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	I_{CC}	Device Selected, $I_{OUT}=0mA$, $ZZ \leq V_{IL}$, Cycle Time $\geq t_{CYC}$ Min	-75	-	350	mA 1,2
			-85	-	330	
			-90	-	300	
			-10	-	260	
Standby Current	I_{SB}	Device deselected, $I_{OUT}=0mA$, $ZZ \leq V_{IL}$, $f=Max$, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-75	-	140	mA
			-85	-	130	
			-90	-	120	
			-10	-	120	
	I_{SB1}	Device deselected, $I_{OUT}=0mA$, $ZZ \leq 0.2V$, $f=0$, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	30	mA	
	I_{SB2}	Device deselected, $I_{OUT}=0mA$, $ZZ \geq V_{DD}-0.2V$, $f=Max$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	30	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	$I_{OL}=8.0mA$	-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	$I_{OH}=-4.0mA$	2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	$I_{OL}=1.0mA$	-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	$I_{OH}=-1.0mA$	2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}		2.0	$V_{DD}+0.5^{**}$	V	3
Input Low Voltage(2.5V I/O)	V_{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}		1.7	$V_{DD}+0.5^{**}$	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

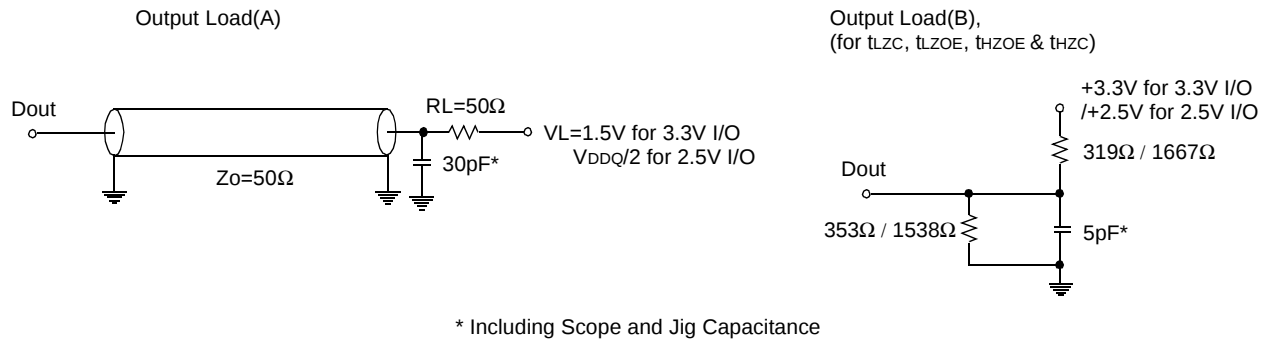


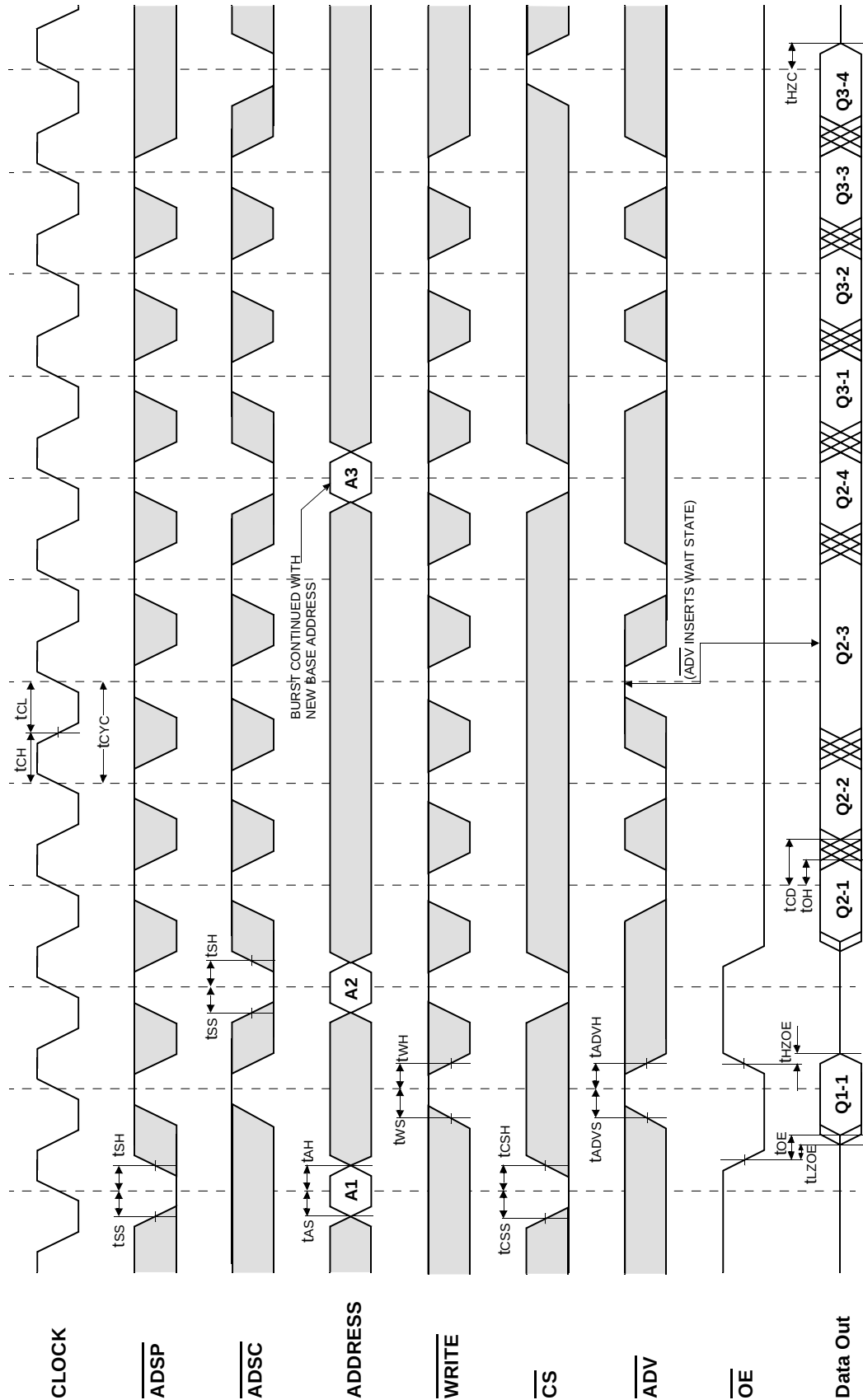
Fig. 1

AC TIMING CHARACTERISTICS(VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

PARAMETER	SYMBOL	-75		-85		-90		-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	8.5	-	10	-	10	-	12	-	ns
Clock Access Time	tCD	-	7.5	-	8.5	-	9.0	-	10	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	tLZC	2.5	-	2.5	-	2.5	-	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	-	3.5	-	4.0	ns
Clock High to Output High-Z	tHZC	-	4.0	-	5.0	-	5.0	-	6.0	ns
Clock High Pulse Width	tCH	2.5	-	3.0	-	3.0	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	3.0	-	3.0	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tpDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tpUS	2	-	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.

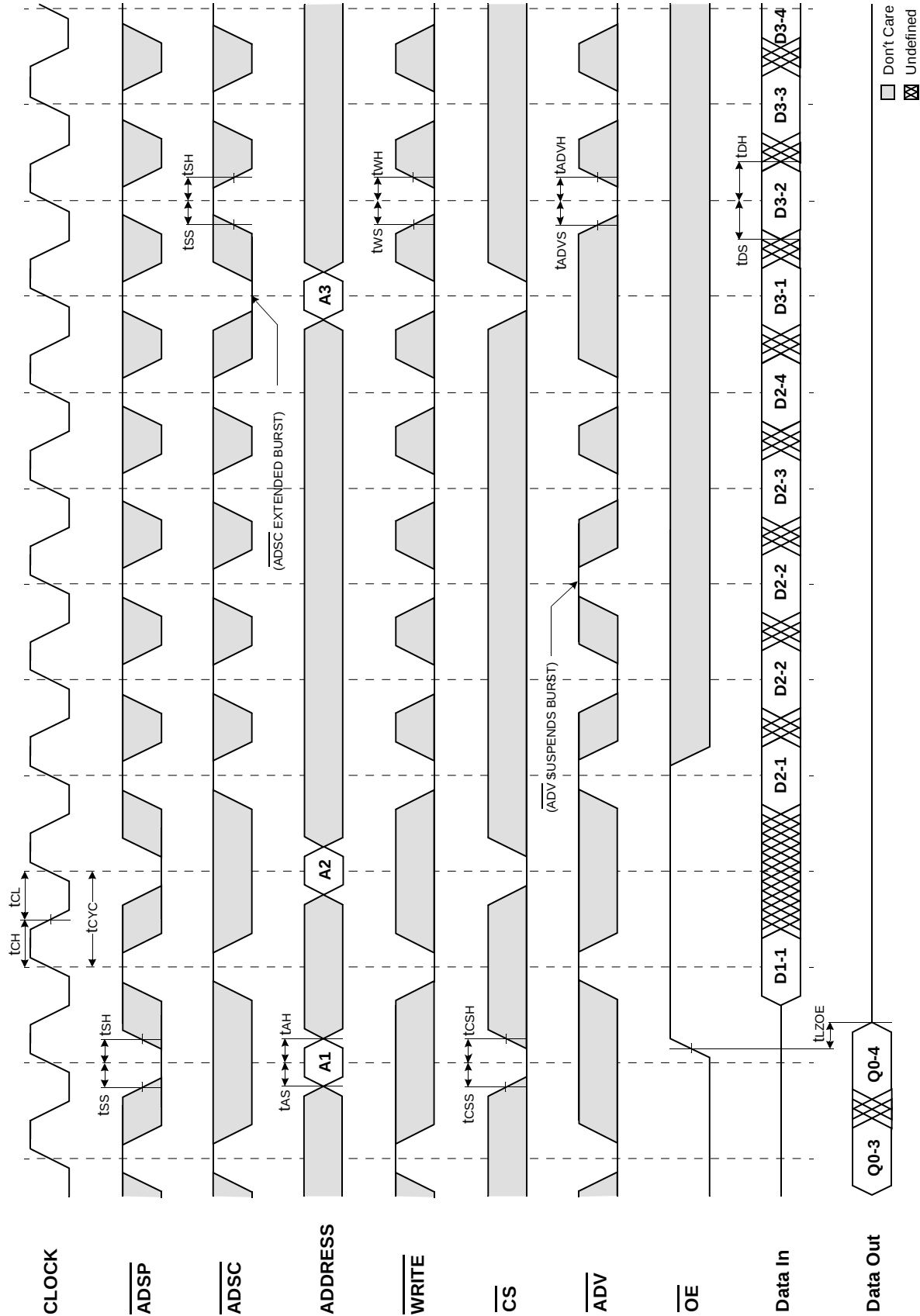
TIMING WAVEFORM OF READ CYCLE



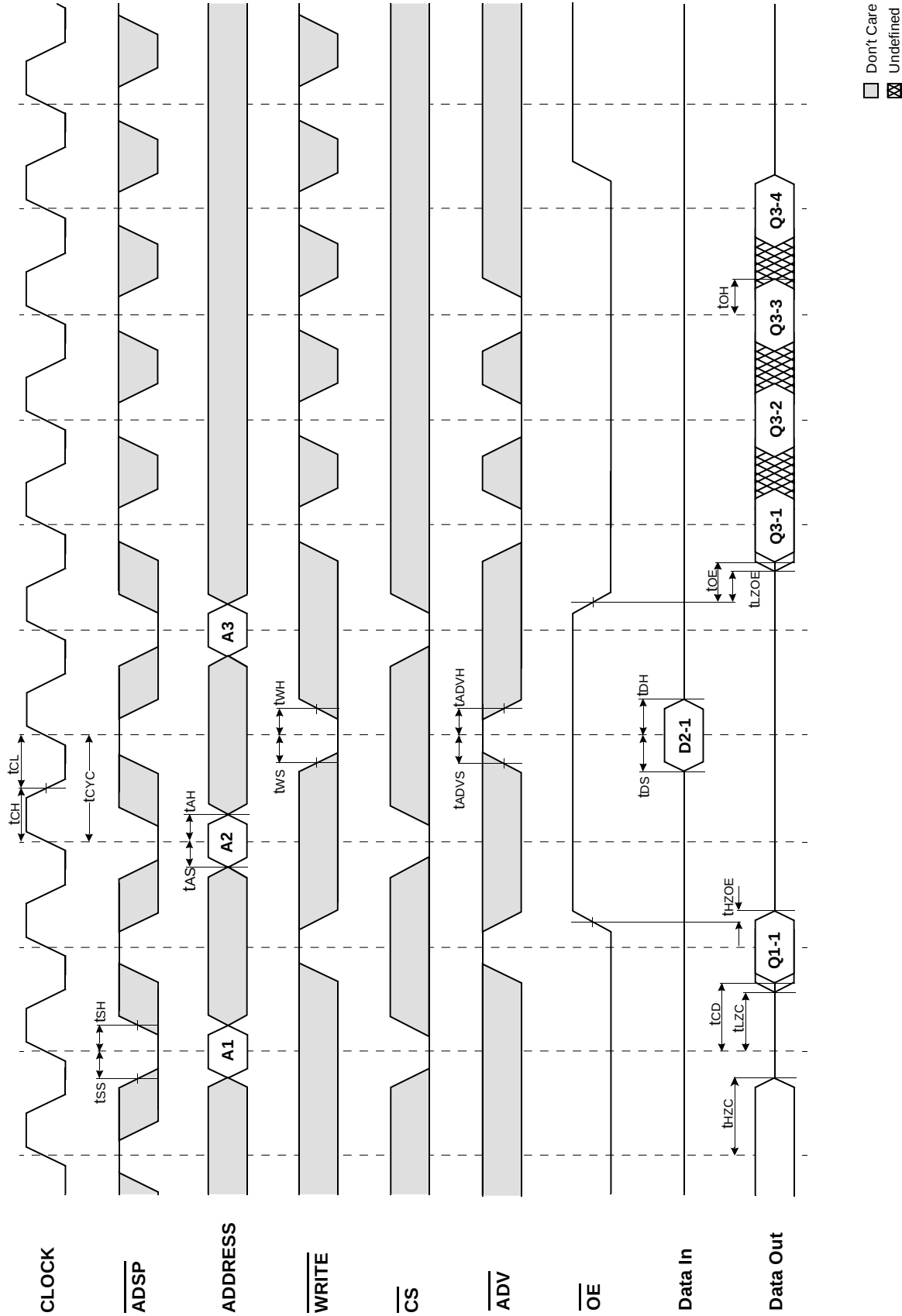
NOTES : $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE} = L$
 $\overline{CS} = L$ means $\overline{CS}_1 = L$, $\overline{CS}_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $\overline{CS}_2 = L$

□ Don't Care
⊗ Undefined

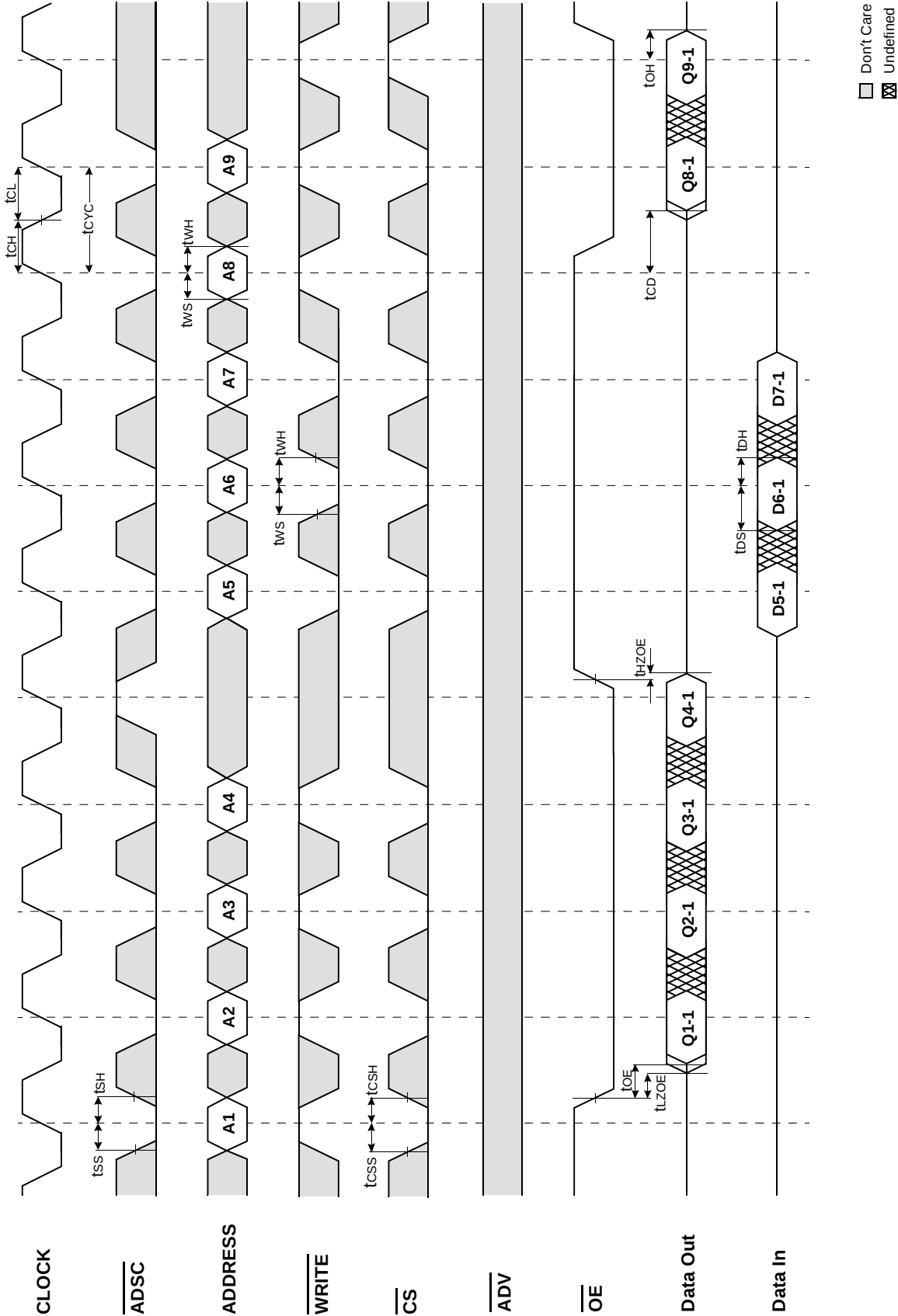
TIMING WAVEFORM OF WRTE CYCLE



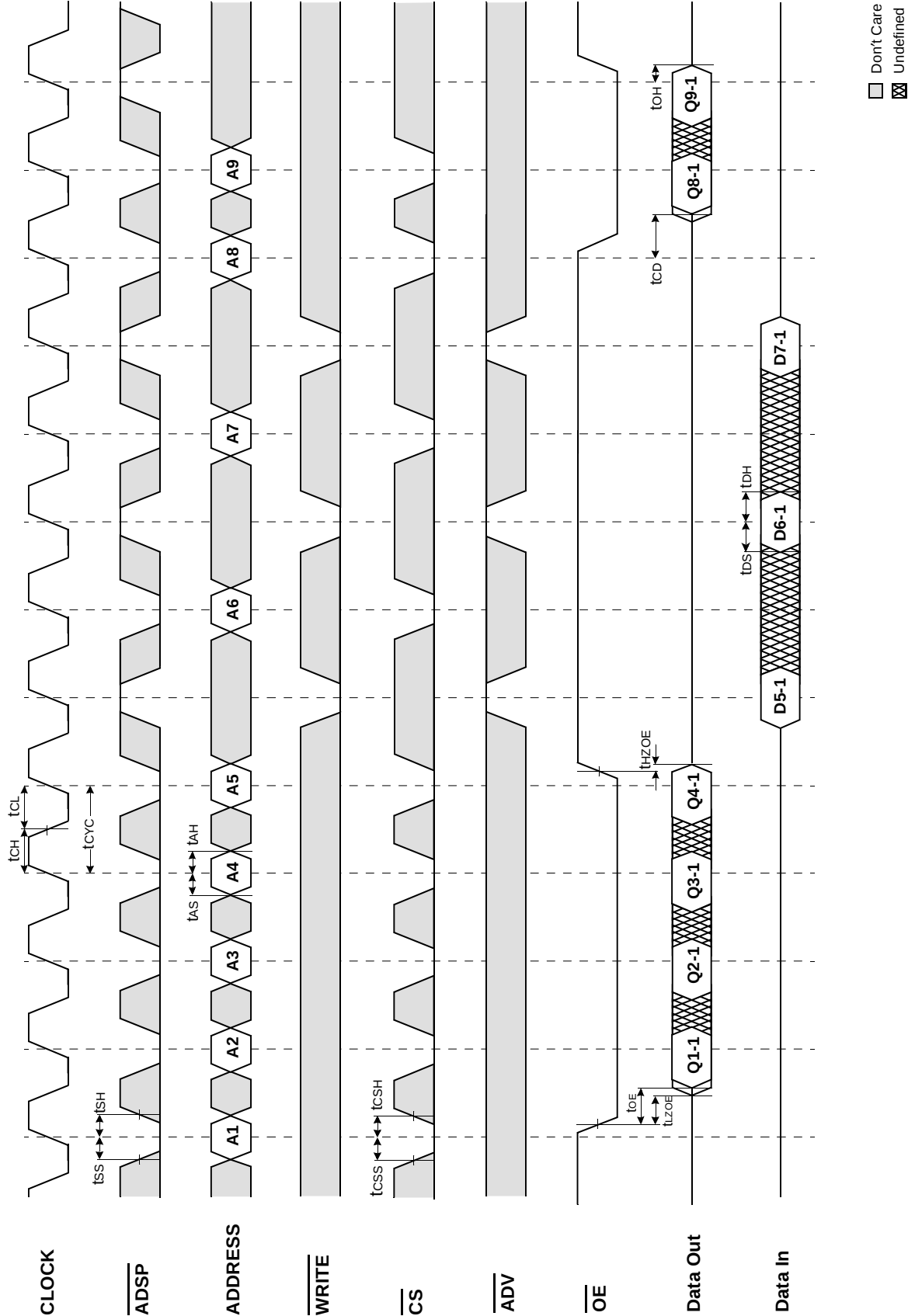
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



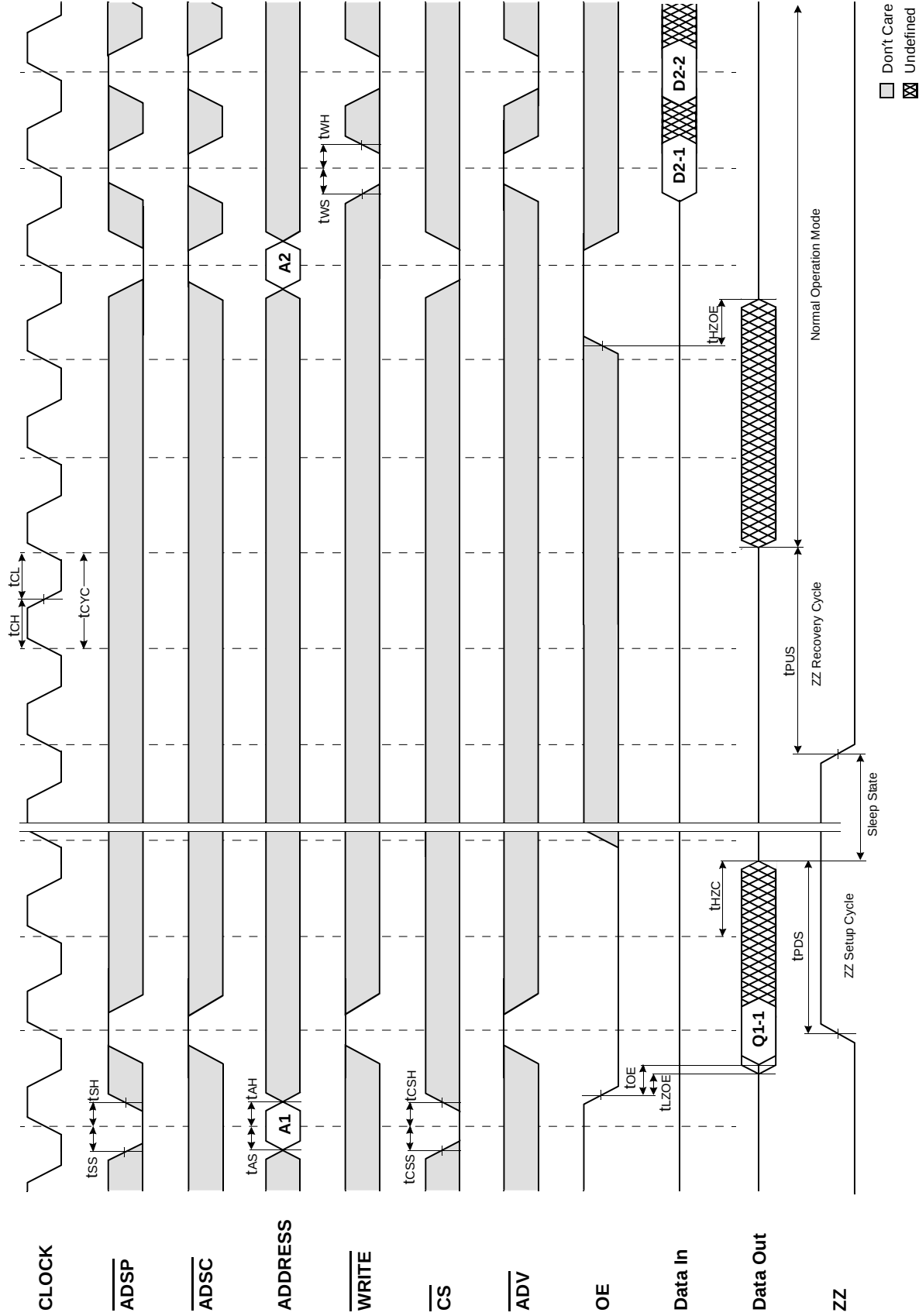
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



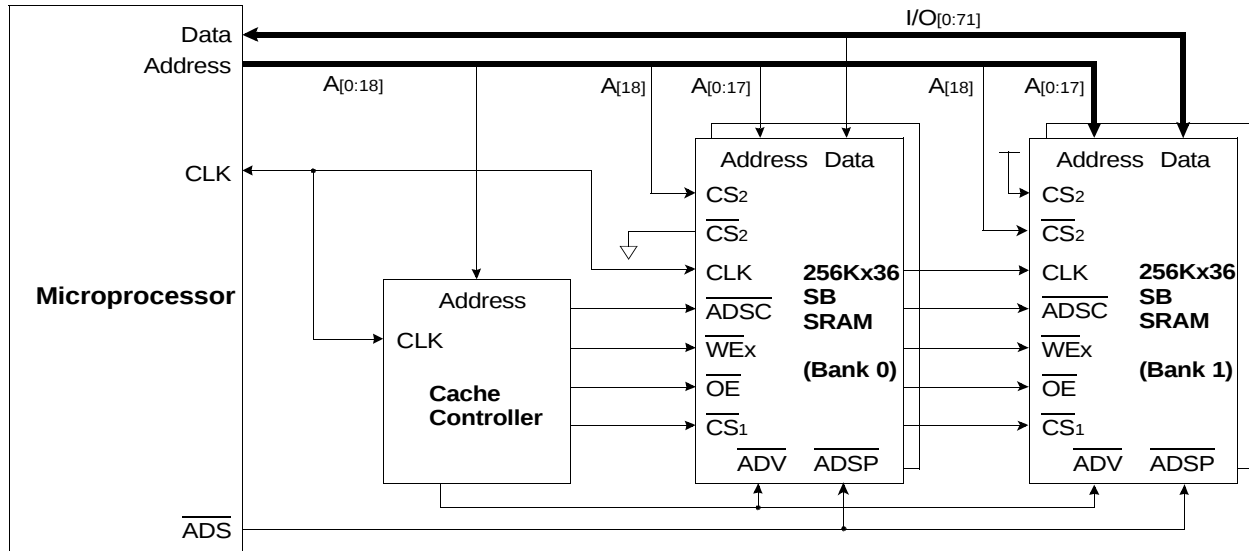
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

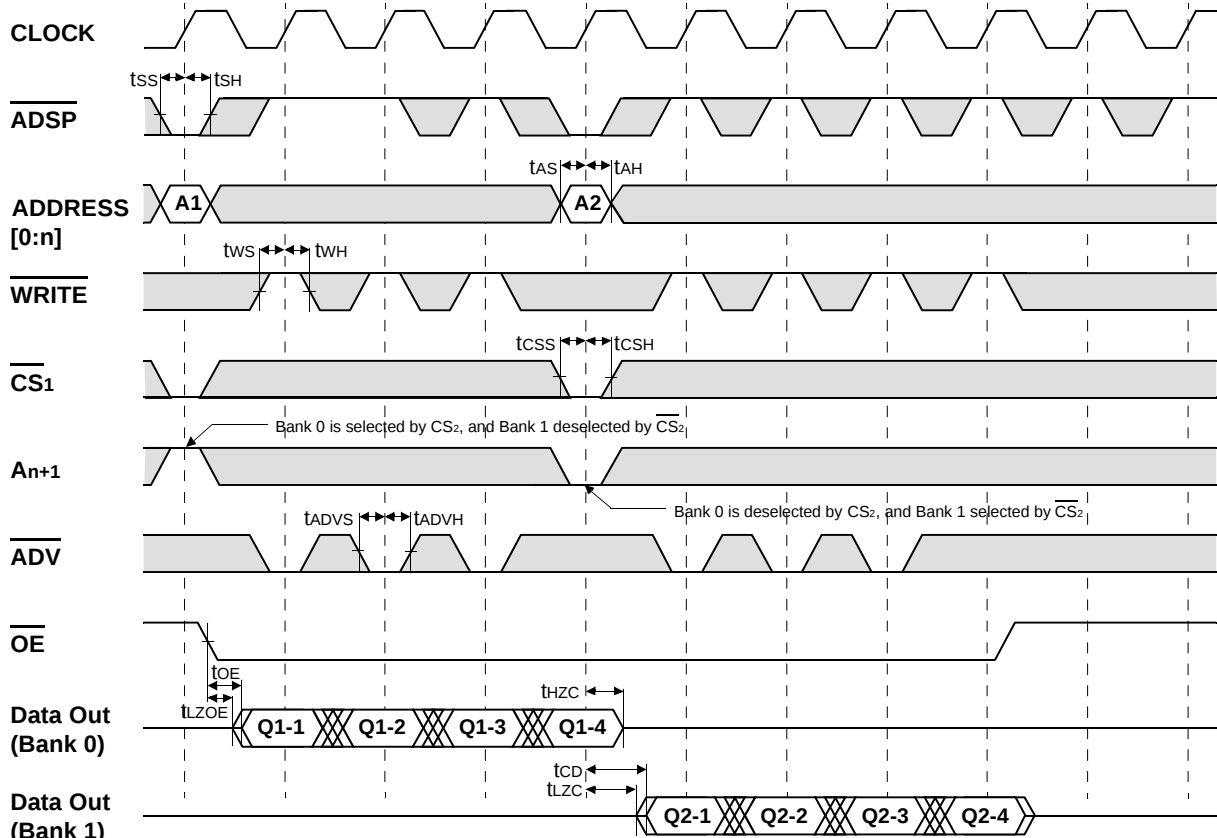
DEPTH EXPANSION

The Samsung 256Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



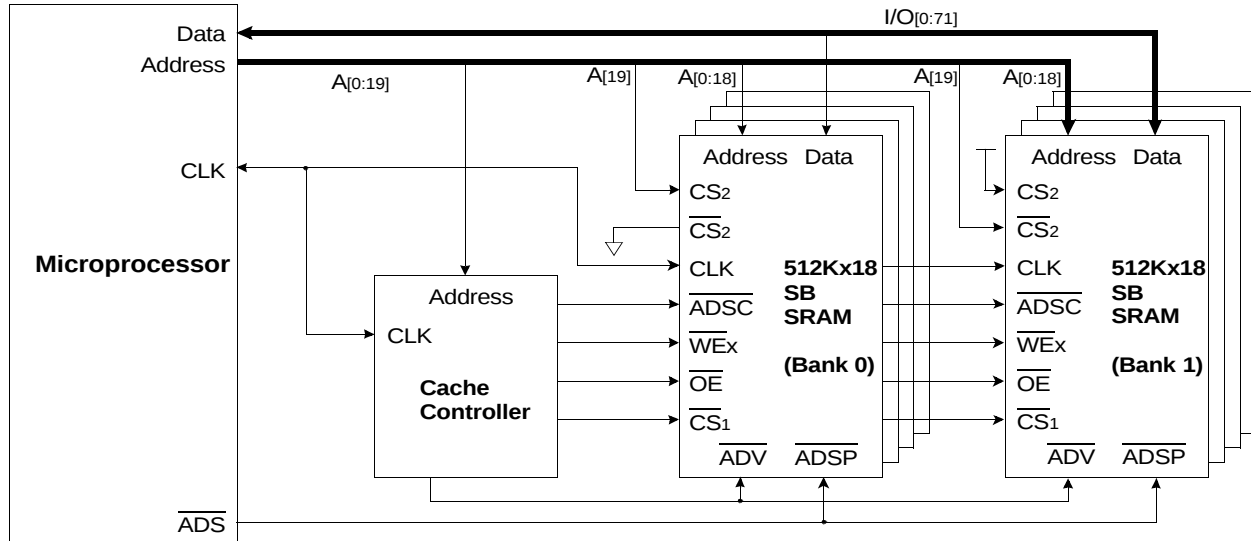
*Notes : n = 14 32K depth, 15 64K depth
16 128K depth, 17 256K depth
18 512K depth

□ Don't Care ▣ Undefined

APPLICATION INFORMATION

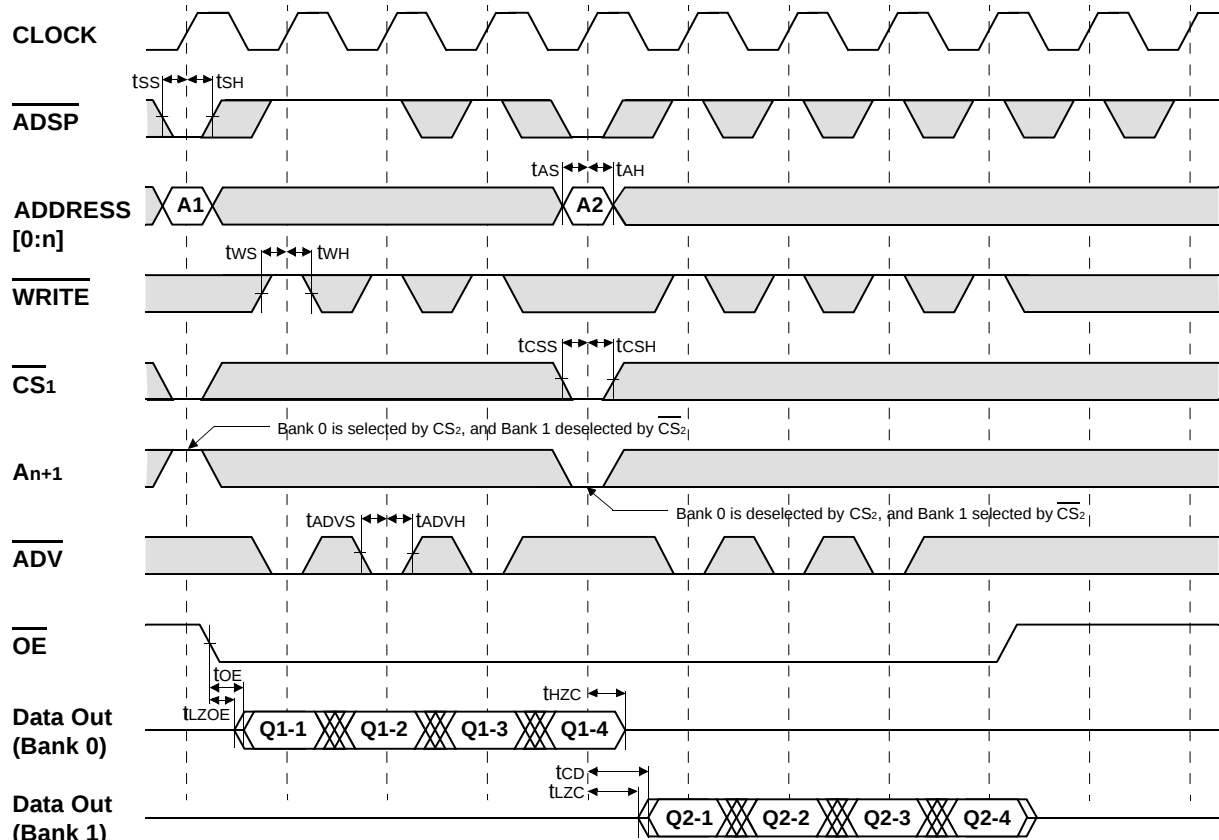
DEPTH EXPANSION

The Samsung 512Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

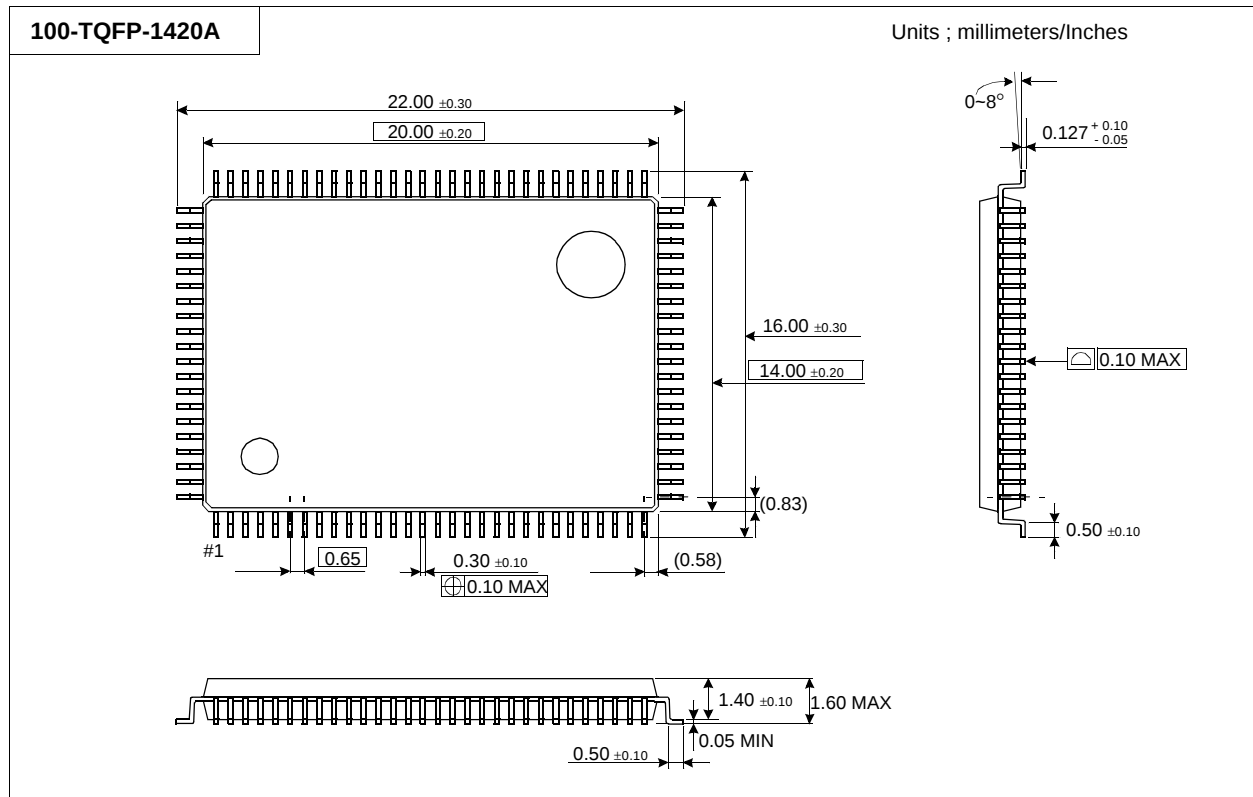
(ADSP CONTROLLED, ADSC=HIGH)



*Notes : n = 14 32K depth, 15 64K depth
16 128K depth, 17 256K depth
18 512K depth, 19 1M depth

□ Don't Care ▣ Undefined

PACKAGE DIMENSIONS



119BGA PACKAGE DIMENSIONS

