19-2105; Rev 0; 7/01

+3.3V, 2.5Gbps Low-Power Transimpedance Amplifier

MAX3271

General Description

The MAX3271 transimpedance amplifier provides a compact low-power solution for 2.5Gbps communications. It features 495nA input-referred noise, 2GHz bandwidth, and 2mA AC input overload.

The MAX3271 is a compact 30mil x 50mil die and requires no external compensation capacitor. It operates from a single +3.3V supply and consumes 83mW. A space-saving filter connection is provided for positive bias to the photodiode through a 750Ω resistor to V_{CC}. These features allow easy assembly into a TO-46 or TO-56 header with a photodiode.

The MAX3271 has a typical optical dynamic range of -21dBm to +3dBm in a shortwave configuration or -24dBm to 0dBm in a longwave configuration. The MAX3271 and MAX3272* provide a two-chip solution for Gigabit Ethernet and Fibre Channel receiver applications.

Applications

Gigabit Ethernet Optical Receivers

Fibre Channel Optical Receivers

System Interconnects

2.5Gbps Optical Receivers

SONET/SDH Receivers

Features

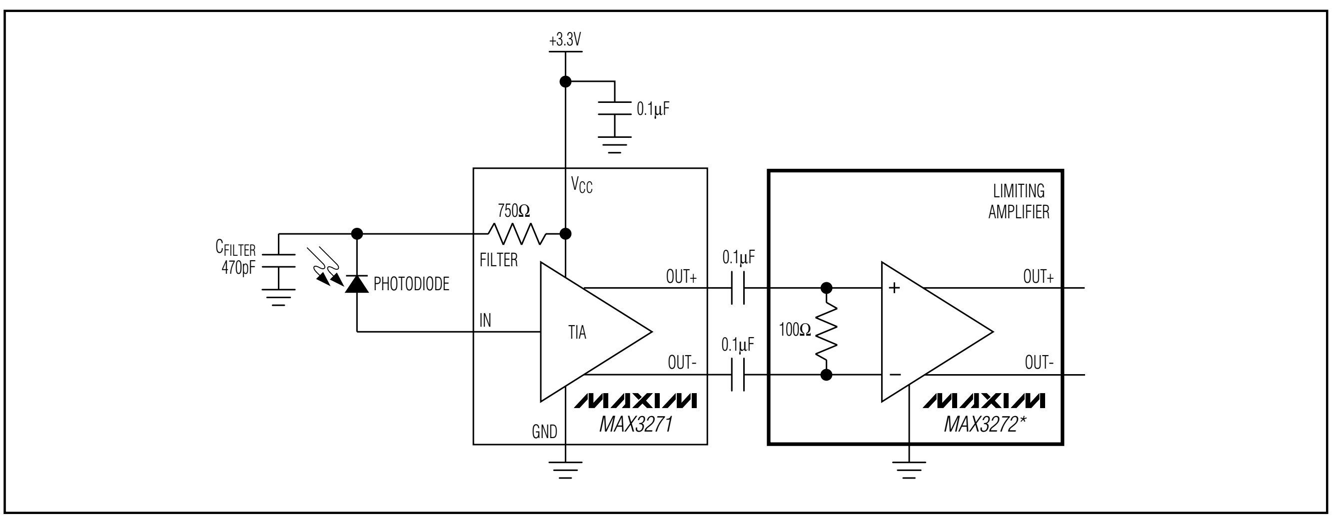
- ♦ **Single +3.3V Power Supply**
- ♦ **83mW Power Consumption**
- ♦ **495nA Input-Referred-Noise**
- ♦ **2GHz Bandwidth**
- ♦ **2mA AC Input Overload**
- ♦ **30mil x 50mil Die Size**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3271E/D	-40°C to +85°C	Dice**
MAX3271E/W	-40°C to +85°C	Wafer**

***Dice/wafers are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_A = +25°C.*

Typical Application Circuit



**Future product*

+3.3V, 2.5Gbps Low-Power Transimpedance Amplifier

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) ....-0.5V to +6.0V
Input Current (IN)..-4mA to +4mA
FILTER Current ....-12mA to +12mA
Voltage at OUT+, OUT- ....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Operating Junction
Temperature Range (T_J) ....-55°C to +150°C
Storage Ambient Temperature Range (T_{stg}) ....-55°C to +150°C
Die Attach Temperature ....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, source capacitance = 0.85pF, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

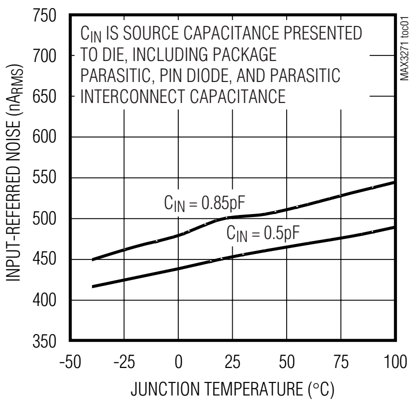
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Voltage				0.66	0.83	1.1	V
Power-Supply Current	I_{CC}				25	35	mA
Transimpedance		40µAp-p input, differential out		2.1	2.8	3.4	kΩ
Small-Signal Bandwidth	BW	(Note 3)		1.5	2		GHz
Output Impedance		Single-ended		42	50	58	Ω
Maximum Differential Output Swing		Input = 1mAp-p		185	300	430	mVp-p
Filter Resistor					750		Ω
AC Input Overload		(Note 3)		2.0			mAp-p
DC Input Overload		(Note 3)		1.0			mA
Input-Referred Noise	I_N	(Note 3)			495	655	nA_{RMS}
Input-Referred Noise Density		(Note 4)			11		$pA/\sqrt{Hz}$
Low-Frequency Cutoff		-3dB, input ≤ 20µA DC			50		kHz
Transimpedance Linear Range		0.95 ≤ linearity ≤ 1.05 (Note 3)		40			µAp-p
Deterministic Jitter	DJ	(Notes 3, 5)	10µAp-p input		18	40	psp-p
			20µAp-p ≤ input ≤ 2mAp-p		12	30	
Power-Supply Noise Rejection	PSNR	ΔV_{CC} = 100mVp-p, f < 2MHz (Note 6)			36		dB

Note 1: Production test at room ambient temperature only. Die parameters are guaranteed by design and characterization at -40°C and +85°C.
Note 2: Source capacitance represents the total capacitance at the IN pad during characterization of the noise and bandwidth parameters.
Note 3: Guaranteed by design and characterization.
Note 4: Input-referred noise density is $I_N/\sqrt{BW}$. No external filters are used for the noise measurements.
Note 5: Deterministic jitter is measured with a K28.5 pattern (0011 1110 1011 0000 0101).
Note 6: Power-supply noise rejection PSNR = $-20\log(\Delta V_{OUT}/\Delta V_{CC})$, where ΔV_{OUT} is the differential output voltage and ΔV_{CC} is the noise on V_{CC}.

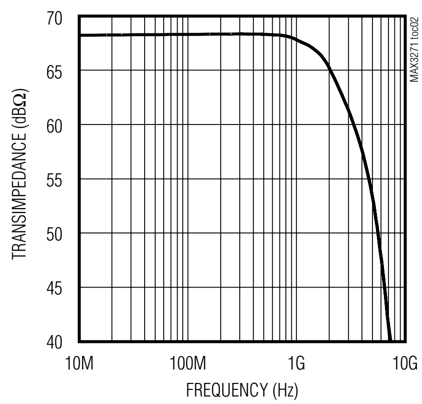
Typical Operating Characteristics

(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)

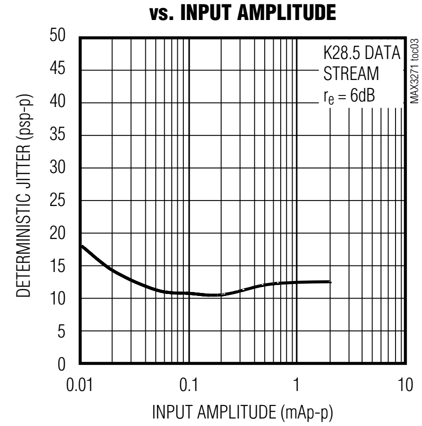
INPUT-REFERRED NOISE vs. TEMPERATURE



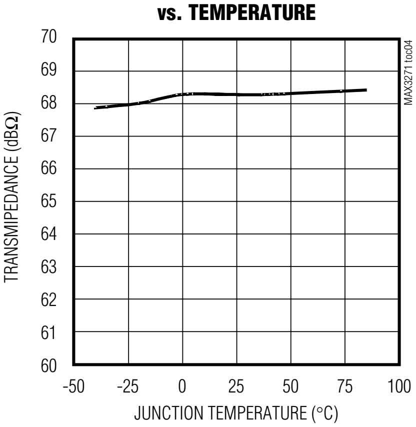
FREQUENCY RESPONSE



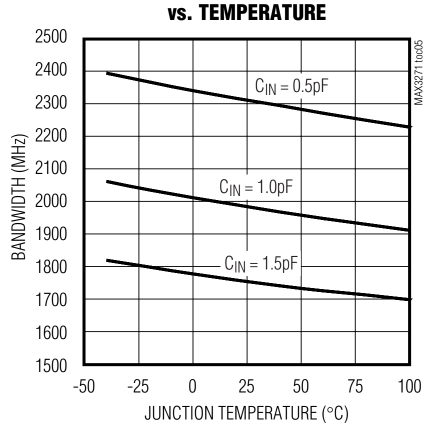
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



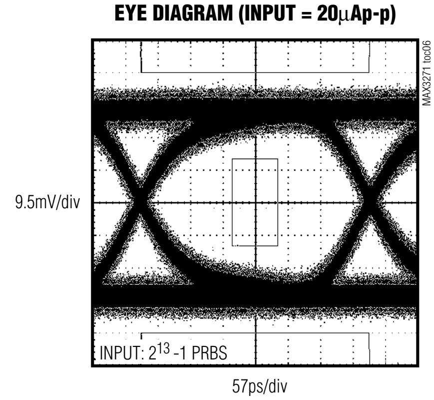
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



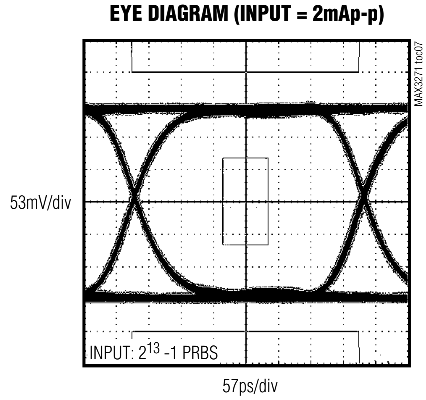
BANDWIDTH vs. TEMPERATURE



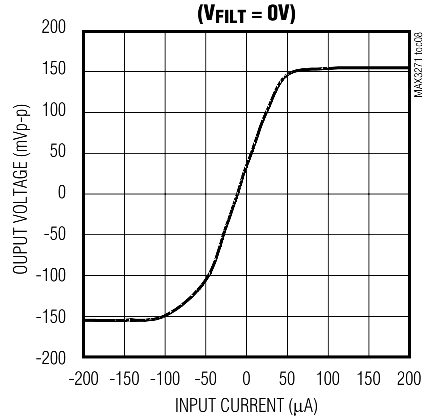
EYE DIAGRAM (INPUT = 20µAp-p)



EYE DIAGRAM (INPUT = 2mAp-p)



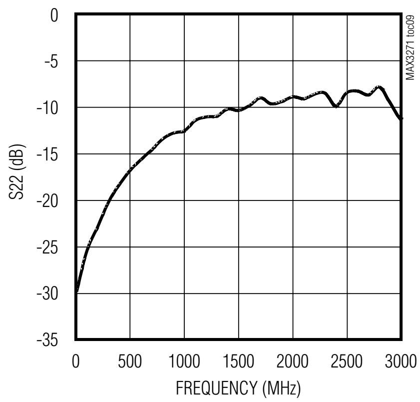
DC TRANSFER FUNCTION (V_{FILT} = 0V)

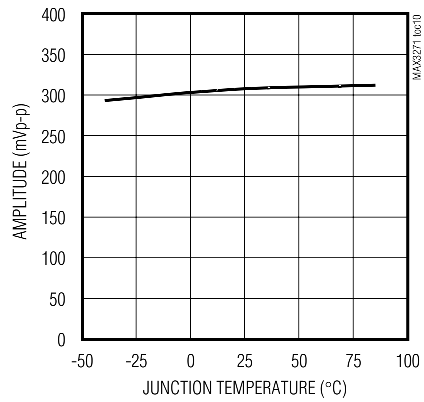


+3.3V, 2.5Gbps Low-Power Transimpedance Amplifier

Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)





Pin Description

BOND PAD	NAME	FUNCTION
1	FILTER	Provides bias voltage for the photodiode through a 750Ω resistor to V_{CC}. When grounded, this pin disables the DC-cancellation amplifier to allow a DC path from IN to OUT+ and OUT- for testing.
2	N.C.	No Connection. Leave unconnected.
3	IN	TIA Input
4, 5	V_{CC}	Power Supply. Both pads must be connected to supply. Bond pad 4 supplies power to the transimpedance stage. Bond pad 5 supplies power to the remaining circuitry.
6, 9	GND	Ground. Both pads must be connected to ground. Bond pad 9 is ground for the transimpedance stage. Bond pad 6 is ground for the remaining circuitry.
7	OUT+	Noninverted Data Output. Current flowing into IN causes V_{OUT+} to increase.
8	OUT-	Inverted Data Output. Current flowing into IN causes V_{OUT-} to decrease.

Detailed Description

The MAX3271 is a transimpedance amplifier designed for 2.5Gbps fiber optic applications. A functional diagram of the MAX3271 is shown in Figure 1. The MAX3271 is comprised of a transimpedance amplifier stage, a voltage amplifier stage, an output buffer, and a direct current feedback cancellation circuit.

Transimpedance Amplifier Stage

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through the resistor R_F converts this current to a voltage. In parallel with the feedback are two back-to-back Schottky diodes that clamp the output signal for large input currents as shown in Figure 2.

Voltage Amplifier Stage

The voltage amplifier stage provides gain and converts the single-ended input to differential outputs.

Output Buffer

The output buffer provides a reverse-terminated voltage output. The buffer is designed to drive a 100Ω differential load between OUT+ and OUT-. The output current is divided between internal 50Ω resistors and the external load resistor. In the *Typical Applications Circuit*, this creates a voltage-divider with gain of 1/2 for a 100Ω differential load. The MAX3271 can also be terminated with higher output impedances, which increases gain and output voltage swing but lowers bandwidth.

For optimum supply-noise rejection, the MAX3271 should be terminated with a differential load. If a single-ended output is required, the unused output should be similarly terminated. The MAX3271 will not drive a DC-coupled 50Ω grounded load.

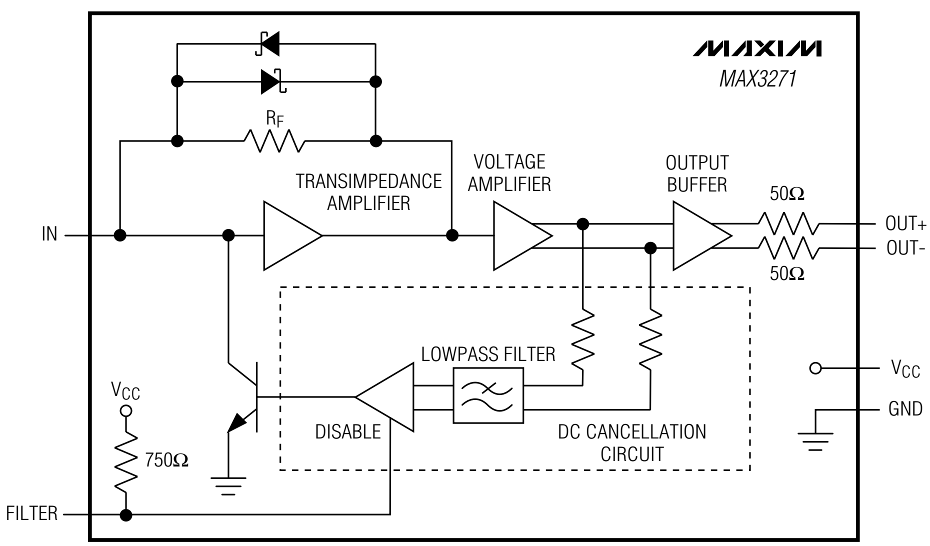


Figure 1. Functional Diagram

+3.3V, 2.5Gbps Low-Power Transimpedance Amplifier

DC Cancellation Circuit

The direct current (DC) cancellation circuit uses low-frequency feedback to remove the DC component of the input signal. This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion caused by large input signals (Figure 3).

The DC cancellation circuit is internally compensated and therefore does not require external capacitors. This circuit minimizes pulse-width distortion for data sequences that exhibit a 50% mark density. A mark density significantly different from 50% will cause the MAX3271 to generate pulse-width distortion.

DC cancellation current is drawn from the input and creates noise. For low-level signals with little or no DC component, this is not a problem. Amplifier noise will increase slightly for signals with significant DC component.

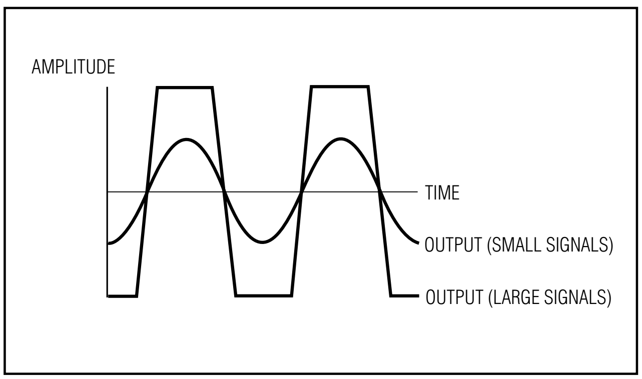


Figure 2. MAX3271 Limited Output

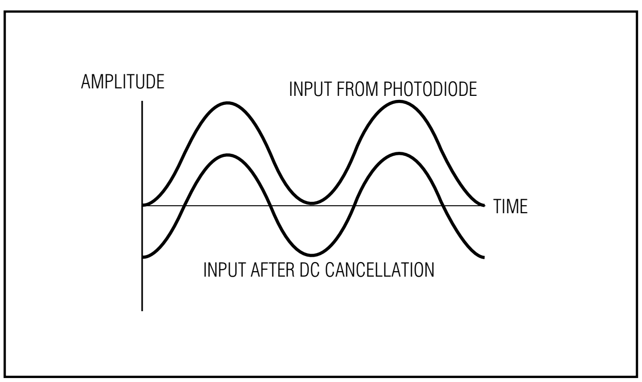


Figure 3. DC Cancellation Effect on Input

Applications Information

Optical Power Relations

Many of the MAX3271 specifications relate to the input signal amplitude. When working with fiber optic receivers, the input is sometimes expressed in terms of average optical power and extinction ratio. Figure 4 shows relations that are helpful for converting optical power to input signal when designing with the MAX3271.

Optical power relations are shown in Table 1; the definitions are true if the average duty cycle of the input data is 50%.

Optical Sensitivity Calculation

The input-referred RMS noise current (I_N) of the MAX3271 generally determines the receiver sensitivity. To obtain a system bit error rate (BER) of 1E-12, the SNR ratio must always exceed 14.1. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{14.1\ I_N\ (r_e + 1)}{2\rho(r_e - 1)}1000\right)\ \text{dBm}$$

where ρ is the photodiode responsivity in A/W.

Input Optical Overload

The overload is the largest input that the MAX3271 accepts while meeting specifications. The optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\log\left(\frac{2\text{mA}}{2\rho}1000\right)\ \text{dBm}$$

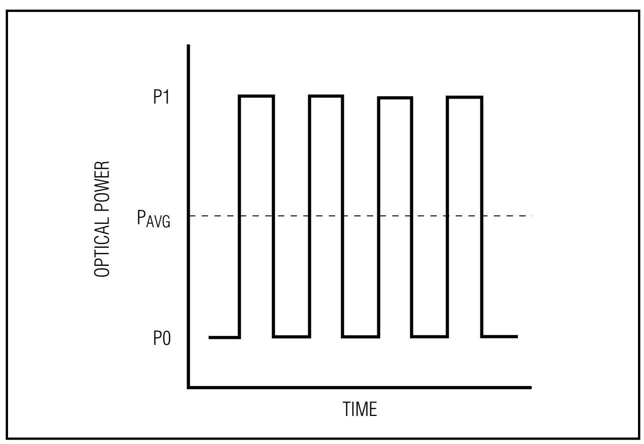


Figure 4. Optical Power Relations

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	P_{AVG} = (P0 + P1) / 2
Extinction Ratio	r_e	r_e = P1/P0
Optical Power of a 1	P1	P1 = 2P_{AVG} (r_e) / (r_e + 1)
Optical Power of a 0	P0	P0 = 2P_{AVG} / (r_e + 1)
Signal Amplitude	P_{IN}	P_{IN} = P1 - P0 = 2P_{AVG} (r_e - 1) / (r_e + 1)

Optical Linear Range

The MAX3271 has high gain, which limits the output when the input signal exceeds 40µAp-p. The MAX3271 operates in a linear range for inputs not exceeding:

$$\text{Linear Range} = 10\log\left(\frac{40\mu A(r_e + 1)}{2\rho(r_e - 1)}1000\right) \text{ dBm}$$

Layout Considerations

Noise performance and bandwidth will be adversely affected by capacitance at the IN pin. Minimize capacitance on this pin and select a low-capacitance photodiode. Assembling the MAX3271 in die form using chip and wire technology provides the best possible performance. Figure 5 shows a suggested layout for a TO header.

Photodiode Filter

Supply voltage noise at the cathode of the photodiode produces a current I = C_{PD} ΔV/Δt, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance.) The filter resistor of the MAX3271, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply

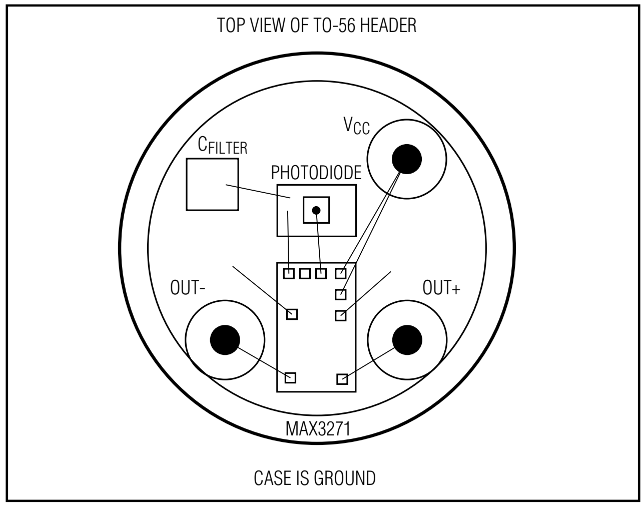


Figure 5. Suggested Layout for TO-56 Header

noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(C_{FILTER})$$

If the amount of tolerable noise is known, the filter capacitor can be easily selected:

$$C_{FILTER} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(I_{NOISE})$$

For example, with maximum noise voltage = 100mVp-p, C_{PD} = 0.85pF, R_{FILTER} = 750Ω, and I_{NOISE} selected to be 250nA (1/2 of the MAX3271's input noise):

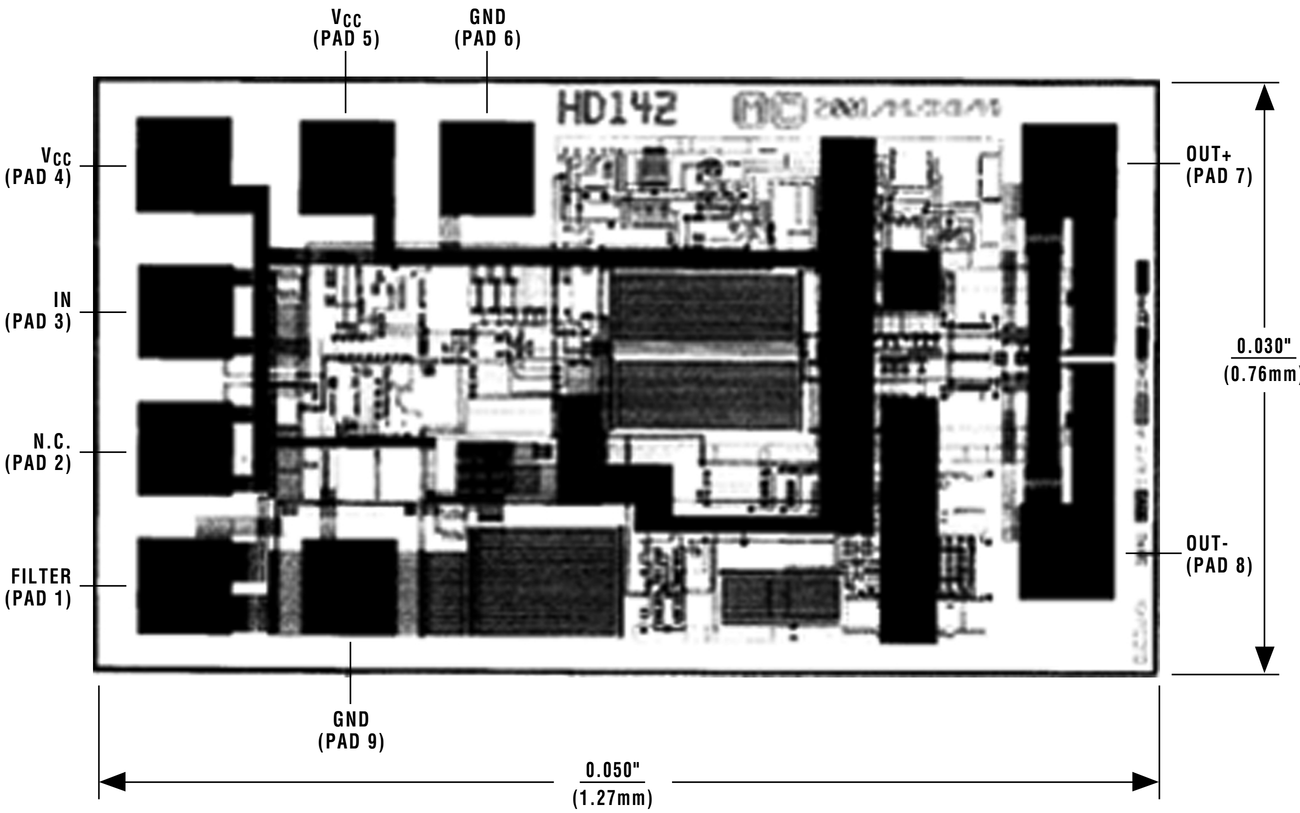
$$C_{FILTER} = (100mV)(0.85pF) / (750\Omega)(250nA) = 450pF$$

Wire Bonding

For high-current density and reliable operation, the MAX3271 uses gold metalization. Connections to the die should be made with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die thickness is typically 15mils (0.375mm).

+3.3V, 2.5Gbps Low-Power Transimpedance Amplifier

Chip Topography



Pad Coordinates

PAD#	COORDINATES (MILS)
1	47, 47
2	47, 197
3	47, 346
4	44, 507
5	222, 505
6	374, 505
7	1006, 505
8	1006, 89
9	226, 47

Coordinates are for the center of the pad.

Coordinate 0, 0 is the lower left corner of the passivation opening for pad 1.

TRANSISTOR COUNT: 340

SUBSTRATE: ELECTRICALLY ISOLATED

PROCESS: SiGe BIPOLAR