SLOS437G - APRIL 2004 - REVISED DECEMBER 2004

OPERATIONAL AMPLIFIER

- Low Offset Voltage Max of:
 - TL103WA . . . 3 mV (25°C) and 5 mV (Full Temperature)
 - TL103W . . . 4 mV (25°C) and 5 mV (Full Temperature)
- Low Supply Current . . . 350 μA/Channel (Typ)
- Unity Gain Bandwidth . . . 0.9 MHz (Typ)
- Input Common-Mode Range Includes GND
- Large Output-Voltage Swing . . .
 0 V to V_{CC} 1.5 V
- Wide Supply-Voltage Range . . . 3 V to 32 V
- 2-kV ESD Protection (HBM)

VOLTAGE REFERENCE

- Fixed 2.5-V Reference
- Tight Tolerance Max of:
 - TL103WA . . . 0.4% (25°C) and 0.8% (Full Temperature)
 - TL103W . . . 0.7% (25°C) and
 1.4% (Full Temperature)
- Low Temperature Drift . . .7 mV (Typ) Over Operating Temperature Range
- Wide Sink-Current Range . . .0.5 mA (Typ) to 100 mA
- Output Impedance . . . 0.2 Ω (Typ)

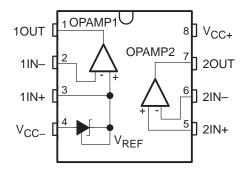
description/ordering information

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference — both of which often are used in the control circuitry of both switch-mode and linear power supplies. OPAMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OPAMP2 is independent, with both inputs uncommitted.

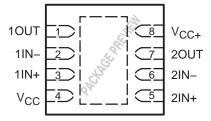
TYPICAL APPLICATIONS

- Battery Charger
- Switch-Mode Power Supply
- Linear Voltage Regulation
- Data-Acquisition Systems

D (SOIC) PACKAGE (TOP VIEW)



DRJ (QFN) PACKAGE (TOP VIEW)



For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from -40°C to 105°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

SLOS437G - APRIL 2004 - REVISED DECEMBER 2004

ORDERING INFORMATION

TA	MAX V _{IO} AND V _{REF} TOLERANCE (25°C)	PACKAGE [†]		TOLERANCE PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
		QFN (DRJ)	Reel of 1000	TL103WAIDRJR	PREVIEW		
	A grade 3 mV, 0.4% Standard grade 4 mV, 0.7%	SOIC (D)	Tube of 75	TL103WAID	Z103WA		
4000 1- 40500			Reel of 2500	TL103WAIDR			
-40°C to 105°C		QFN (DRJ)	Reel of 1000	TL103WIDRJR	PREVIEW		
		SOIC (D)	Tube of 75	TL103WID	7402\\		
	, 5 75	SOIC (D)	Reel of 2500	TL103WIDR	Z103W		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	36 V
Operational amplifier input differential voltage, V _{id}	36 V
Operational amplifier input voltage range, V _I	. -0.3 V to 36 V
Voltage reference cathode current, I _{KA}	100 mA
Package thermal impedance, θ _{JA} (see Notes 1 and 2): D package	97°C/W
(see Notes 1 and 3): DRJ package	TBD°C/W
Maximum junction temperature, T _J	150°C
Storage temperature range, T _{stg}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions

		MIN	MAX	UNIT
VIN	Supply voltage	3	32	V
ΙK	Cathode current	1	100	mA
TA	Operating free-air temperature	-40	105	°C



typical application circuit

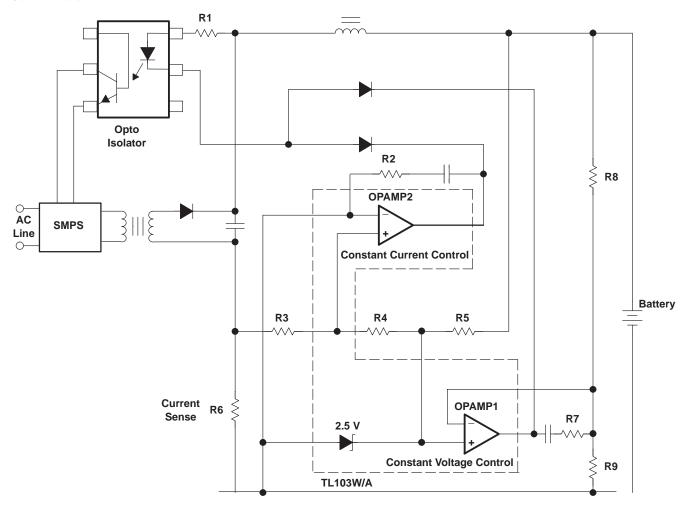


Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger

TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

SLOS437G - APRIL 2004 - REVISED DECEMBER 2004

OPAMP1, operational amplifier with noninverting input connected to the internal V_{REF} electrical characteristics, V_{CC+} = 5 V, V_{CC} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT		
	TI 400144		25°C		1	4			
land offert college	1L103W	Vicm = 0 V	Full range			5	mV		
input offset voltage	TI 400\\/	V 0V	25°C		0.5	3			
	TL103VVA	vicm = 0 v	Full range			5			
Input offset-voltage drift			25°C		7		μV/°C		
Input bias current (negati	ve input)		25°C		20		nA		
Large-signal voltage gain	l	$V_{CC+} = 15 \text{ V, R}_{L} = 2 \text{ k}\Omega,$ $V_{icm} = 0 \text{ V}$	25°C		100		V/mV		
Supply-voltage rejection	ratio	V _{CC+} = 5 V to 30 V, V _{icm} = 0 V	25°C	65	100		dB		
Output source current		V _{CC+} = 15 V, V _O = 2 V, V _{id} = 1 V	25°C	20	40		mA		
Short circuit to GND		V _{CC+} = 15 V	25°C		40	60	mA		
I _{sink} Output sink current		$V_{CC+} = 15 \text{ V}, V_{O} = 2 \text{ V}, V_{id} = -1 \text{ V}$				10	12		mA
		Sutput sink current $V_{CC+} = 15 \text{ V}, V_O = 0.2 \text{ V}, V_{id} = -1 \text{ V}$		12	50		μΑ		
		V 00 V D 01 O	25°C	26	27				
		$VCC^{+} = 30 \text{ V, RL} = 2 \text{ K}\Omega$	Full range	26			V		
nigri-level output voltage		V 20 V D. 40 kO		27	28		V		
		VCC+ = 30 V, KL = 10 K52	Full range	27					
Low lovel output voltage		P ₁ = 10 kO	25°C		5	20	mV		
Low-level output voltage		IN_ = 10 KS2	Full range			20	IIIV		
Slew rate at unity gain		$\begin{split} &V_{CC+}=15\text{ V,}\\ &C_L=100\text{ pF, }R_L=2\text{ k}\Omega,\\ &V_I=0.5\text{ V to 2 V, unity gain} \end{split}$	25°C	0.2	0.4		V/μs		
Gain bandwidth product		$V_{CC+} = 30 \text{ V}, V_I = 10 \text{ mV},$ $C_L = 100 \text{ pF}, R_L = 2 \text{ k}\Omega,$ $f = 100 \text{ kHz}$	25°C	0.5	0.9		MHz		
Total harmonic distortion		$V_{CC+} = 30 \text{ V}, V_O = 2 \text{ V}_{pp},$ $C_L = 100 \text{ pF}, R_L = 2 \text{ k}\Omega,$ $f = 1 \text{ kHz}, A_V = 20 \text{ dB}$	25°C		0.02		%		
	Input offset voltage Input offset-voltage drift Input bias current (negati Large-signal voltage gain Supply-voltage rejection Output source current Short circuit to GND Output sink current High-level output voltage Low-level output voltage Slew rate at unity gain Gain bandwidth product	Input offset voltage Input offset-voltage drift Input bias current (negative input) Large-signal voltage gain Supply-voltage rejection ratio Output source current Short circuit to GND Output sink current High-level output voltage Low-level output voltage Slew rate at unity gain Gain bandwidth product					$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		

SLOS437G - APRIL 2004 - REVISED DECEMBER 2004

OPAMP2, independent operational amplifier electrical characteristics, V_{CC+} = 5 V, V_{CC} = GND, V_O = 1.4 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT	
				25°C		1	4	
l		TL103W	V _{icm} = 0 V	Full range			5	.,
V _{IO}	Input offset voltage	TI 4001444		25°C		0.5	3	mV
		TL103WA	V _{icm} = 0 V	Full range			5	
∝VIO	Input offset voltage drift	•		25°C		7		μV/°C
	lanut effect coment			25°C		2	75	- ^
lio	Input offset current			Full range			150	nA
	Lancet Idea accomment			25°C		20	150	^
I _{IB}	Input bias current			Full range			200	nA
			$V_{CC+} = 15 \text{ V, R}_{L} = 2 \text{ k}\Omega,$	25°C	50	100		.,, .,
AVD	Large-signal voltage gain		$V_0 = 1.4 \text{ V to } 11.4 \text{ V}$	Full range	25			V/mV
k _{SVR}	Supply-voltage rejection	ratio	$V_{CC+} = 5 \text{ V to } 30 \text{ V}$	25°C	65	100		dB
.,			20.7/() 1/()	25°C	0		(V _{CC+}) – 1.5	.,
VICR	Input common-mode vol	tage range	$V_{CC+} = 30 \text{ V (see Note 4)}$	Full range	0		(V _{CC+}) – 2	V
01.100				25°C	70	85		
CMRR	MRR Common-mode rejection ratio			Full range	60			dB
I _{source}	Output source current		V _{CC+} = 15 V, V _O = 2 V, V _{id} = 1 V	25°C	20	40		mA
Isc	Short circuit to GND		V _{CC+} = 15 V	25°C		40	60	mA
			V _{CC+} = 15 V, V _O = 2 V, V _{id} = -1 V	_	10	12		mA
^I sink	Output sink current		V _{CC+} = 15 V, V _O = 0.2 V, V _{id} = -1 V	25°C	12	50		μΑ
				25°C	26	27		
.,			$V_{CC+} = 30 \text{ V}, R_L = 2 \text{ k}\Omega$	Full range	26			.,
VOH	High-level output voltage	9	V 00 V D 40 LO	25°C	27	28		V
			$V_{CC+} = 30 \text{ V}, R_L = 10 \text{ k}\Omega$	Full range	27			
.,	Landard and and and and		D 4010	25°C		5	20	>/
VOL	Low-level output voltage		$R_L = 10 \text{ k}\Omega$	Full range			20	mV
SR	Slew rate at unity gain	Slew rate at unity gain		25°C	0.2	0.4		V/μs
GBW	Gain bandwidth product		$V_{CC+} = 30 \text{ V, } V_I = 10 \text{ mV,}$ $C_L = 100 \text{ pF, } R_L = 2 \text{ k}\Omega,$ $f = 100 \text{ kHz,}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion		$V_{CC+} = 30 \text{ V}, V_O = 2 \text{ V}_{pp},$ $C_L = 100 \text{ pF}, R_L = 2 \text{ k}\Omega,$ $f = 1 \text{ kHz}, A_V = 20 \text{ dB}$	25°C		0.02		%
Vn	Equivalent input noise vo	oltage	$V_{CC} = 30 \text{ V, R}_{S} = 100 \Omega,$ f = 1 kHz			50		nV/√ Hz

NOTE 4: The input common-mode voltage of either input should not be allowed to go below -0.3 V. The upper end of the common-mode voltage range is $(V_{CC+}) - 1.5$ V, but either input can go to $(V_{CC+}) + 0.3$ V (but ≤ 36 V) without damage.



TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

SLOS437G - APRIL 2004 - REVISED DECEMBER 2004

VOLTAGE REFERENCE electrical characteristics

PARAMETER			TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
		TI 400\\	L. 40 mA	25°C	2.482	2.5	2.518	
\/	Deference voltage	TL103W	I _K = 10 mA	Full range	2.465		2.535	.,
VREF	Reference voltage	TL103WA I _K = 10 mA		25°C	2.49	2.5	2.51	V
				Full range	2.48		2.52	
ΔVREF	VREF Reference input voltage deviation over temperature range		$V_{KA} = V_{REF}$, $I_K = 10 \text{ mA}$	Full range		7	30	mV
I _{min}	Minimum cathode current	for regulation	V _{KA} = V _{REF}	25°C		0.5	1	mA
z _{ka}	Dynamic impedance (see Note 5)		$V_{KA} = V_{REF}$, $\Delta I_{K} = 1$ mA to 100 mA, $f < 1$ kHz	25°C		0.2	0.5	Ω

NOTE 5: The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_{K}}$.

TOTAL DEVICE electrical characteristics

	PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
laa	Total supply current,	V _{CC+} = 5 V, No load	Full range		0.7	1.2	mA
'CC	excluding cathode-current reference	$V_{CC+} = 30 \text{ V}$, No load	Tuillange			2	IIIA





ti.com 30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL103WAID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
TL103WID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR Level-1-235C-UNLIM
TL103WIDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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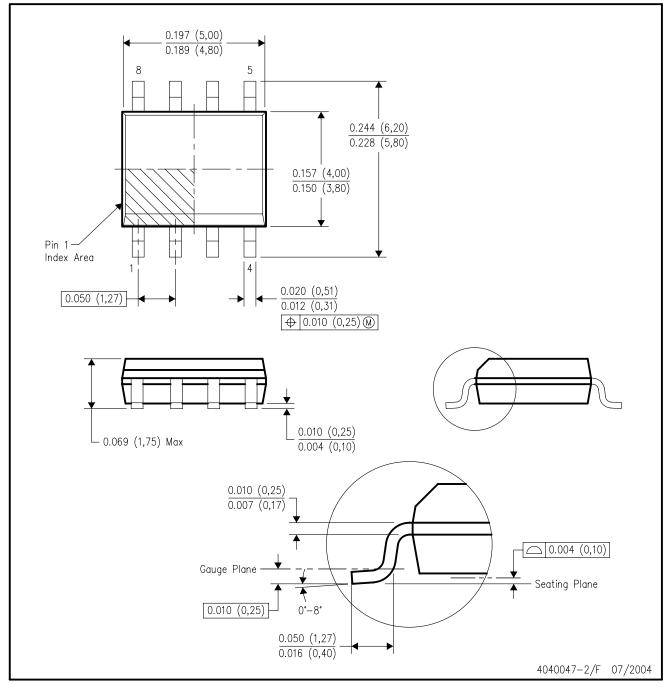
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.



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