# HD404339 Series

HITACHI

Rev. 7.0
Sept. 1999

## Description

The HD404339 Series is 4-bit HMCS400-Series microcomputer with large-capacity memory designed to increase program productivity. Each microcomputer has an A/D converter, input capture timer, and a 32-kHz oscillator circuit for clock use all built in. They also come with high-voltage I/O pins that can directly drive a fluorescent display.

The HD404339 Series includes six chips: the HD404339 with 16-kword ROM; the HD4043312 with 12-kword ROM; the HD404338 with 8-kword ROM; the HD404336 with 6-kword ROM; the HD404334 with 4-kword ROM; the HD4074339 with 16-kword PROM.

The HD4074339 is a PROM version ZTAT™ microcomputer. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

## Features

- 54 I/O pins
  - — One input-only pin
  - — 53 input/output pins: 30 pins are high-voltage pins (40 V, max.)
- On-chip A/D converter (8-bit × 12-channel)
- Three timers
  - — One event counter input
  - — One timer output
  - — One input capture timer
- 8-bit clock-synchronous serial interface (1 channel)
- Alarm output
- Built-in oscillators
  - — Ceramic or crystal oscillator
  - — External clock drive is also possible
  - — Subclock: 32.768-kHz crystal oscillator

Hitachi semiconductor

- Seven interrupt sources
  - — Two by external sources
  - — Three by timers
  - — One each by the A/D converter and serial interface
- Four low-power dissipation modes
  - — Standby mode
  - — Stop mode
  - — Watch mode
  - — Subactive mode
- Instruction cycle time: 1 µs ($f_{OSC}$ = 4 MHz, 1/4 division ratio)
  - — 1/4, 1/8, 1/16, 1/32 system clock division ratio can be selected

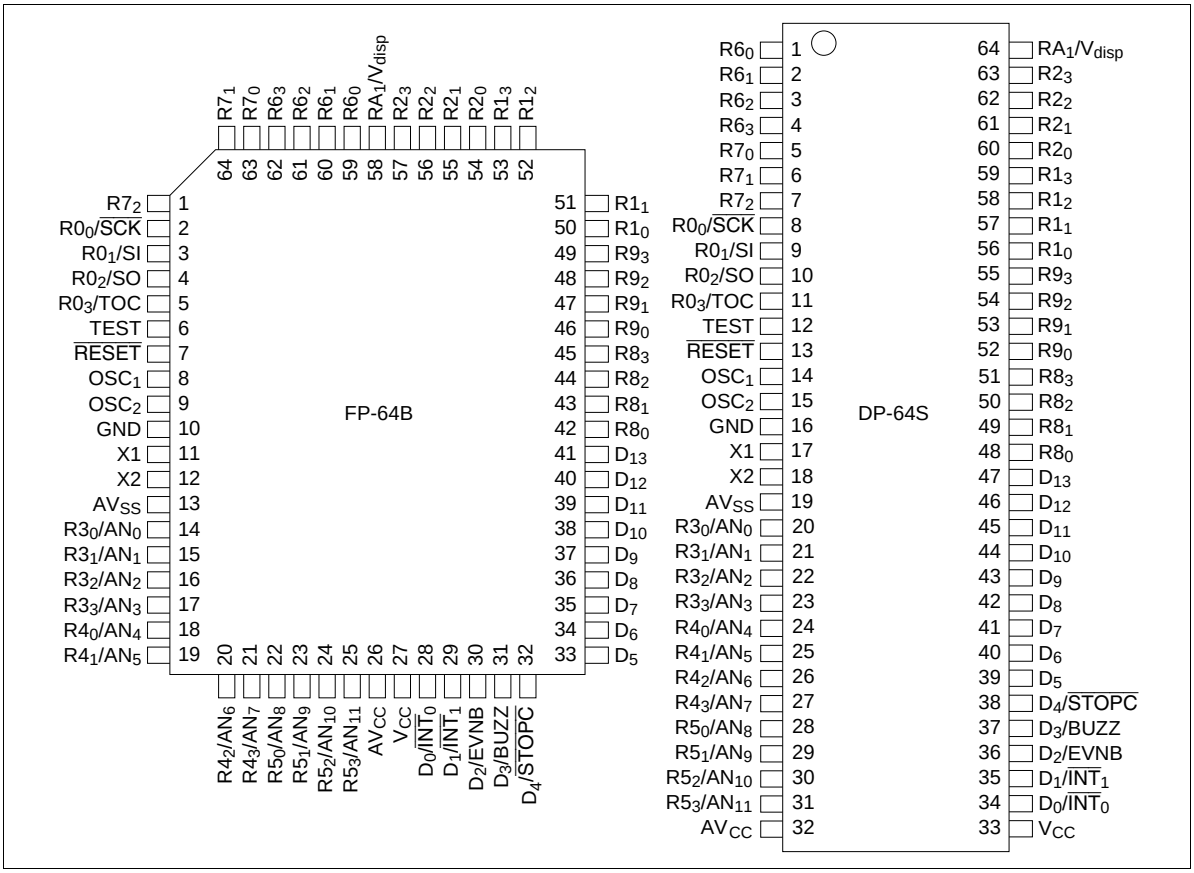
## Ordering Information

| Type | Product Name | Model Name | ROM (words) | RAM (digit) | Package |
|---|---|---|---|---|---|
| Mask ROM | HD404334 | HD404334S | 4,096 | 512 | DP-64S |
| | | HD404334FS | | | FP-64B |
| | HD404336 | HD404336S | 6,144 | | DP-64S |
| | | HD404336FS | | | FP-64B |
| | HD404338 | HD404338S | 8,912 | | DP-64S |
| | | HD404338FS | | | FP-64B |
| | HD4043312 | HD4043312S | 12,288 | | DP-64S |
| | | HD4043312FS | | | FP-64B |
| | HD404339 | HD404339S | 16,384 | | DP-64S |
| | | HD404339FS | | | FP-64B |
| ZTAT™ | HD4074339 | HD4074339S | 16,384 | | DP64S |
| | | HD4074339FS | | | FP-64B |

## Recommended PROM Programmers and Socket Adapters

| PROM Programmer | | Socket Adapter | | |
|---|---|---|---|---|
| **Manufacture** | **Model Name** | **Package** | **Manufacture** | **Model Name** |
| DATA I/O corp | 121 B | DP-64S | Hitachi | HS4339ESS01H |
| | | FP-64B | | HS4339ESF01H |
| AVAL corp | PKW-1000 | DP-64S | Hitachi | HS4339ESS01H |
| | | FP-64B | | HS4339ESF01H |

## Pin Arrangement



## Pin Description

| Item | Symbol | Pin Number DP-64S | Pin Number FP-64B | I/O | Function |
|---|---|---|---|---|---|
| Power supply | $V_{CC}$ | 33 | 27 | | Applies power voltage |
| | GND | 16 | 10 | | Connected to ground |
| | $V_{disp}$ (shared with $RA_1$) | 64 | 58 | | Used as a high-voltage output power supply pin when selected by the mask option |
| Test | TEST | 12 | 6 | I | Cannot be used in user applications. Connect this pin to GND. |
| Reset | $\overline{RESET}$ | 13 | 7 | I | Resets the MCU |
| Oscillator | $OSC_1$ | 14 | 8 | I | Input/output pin for the internal oscillator. Connect these pins to the ceramic or crystal oscillator, or $OSC_1$ to an external oscillator circuit. |
| | $OSC_2$ | 15 | 9 | O | |
| | X1 | 17 | 11 | I | Used with a 32.768-kHz crystal oscillator for clock purposes |
| | X2 | 18 | 12 | O | |
| Port | $D_0$–$D_{13}$ | 34–47 | 28–41 | I/O | Input/output pins addressed individually by bits; $D_0$–$D_{13}$ are all high-voltage I/O pins. Each pin can be individually configured as selected by the mask option. |
| | $RA_1$ | 64 | 58 | I | One-bit high-voltage input port pin |
| | $R0_0$–$R0_3$, $R3_0$–$R7_2$ | 1–11, 20–31 | 1–5, 14–25, 59–64 | I/O | Four-bit input/output pins consisting of standard voltage pins |
| | $R1_0$–$R2_3$, $R8_0$–$R9_3$ | 48–63 | 42–57 | I/O | Four-bit input/output pins consisting of high voltage pins |
| Interrupt | $\overline{INT}_0$, $\overline{INT}_1$ | 34, 35 | 28, 29 | I | Input pins for external interrupts |
| Stop clear | $\overline{STOPC}$ | 38 | 32 | I | Input pin for transition from stop mode to active mode |
| Serial interface | $\overline{SCK}$ | 8 | 2 | I/O | Serial interface clock input/output pin |
| | SI | 9 | 3 | I | Serial interface receive data input pin |
| | SO | 10 | 4 | O | Serial interface transmit data output pin |
| Timer | TOC | 11 | 5 | O | Timer output pin |
| | EVNB | 36 | 30 | I | Event count input pin |
| Alarm | BUZZ | 37 | 31 | O | Square waveform output pin |

| Item | Symbol | Pin Number DP-64S | Pin Number FP-64B | I/O | Function |
|---|---|---|---|---|---|
| A/D converter | $AV_{CC}$ | 32 | 26 | | Power supply for the A/D converter. Connect this pin as close as possible to the $V_{CC}$ pin and at the same voltage as $V_{CC}$. If the power supply voltage to be used for the A/D converter is not equal to $V_{CC}$, connect a 0.1-µF bypass capacitor between the $AV_{CC}$ and $AV_{SS}$ pins. (However, this is not necessary when the $AV_{CC}$ pin is directly connected to the $V_{CC}$ pin.) |
| | $AV_{SS}$ | 19 | 13 | | Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND. |
| | $AN_0$–$AN_{11}$ | 20–31 | 14–25 | I | Analog input pins for the A/D converter |

## Pin Description in PROM Mode

The HD4074339 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

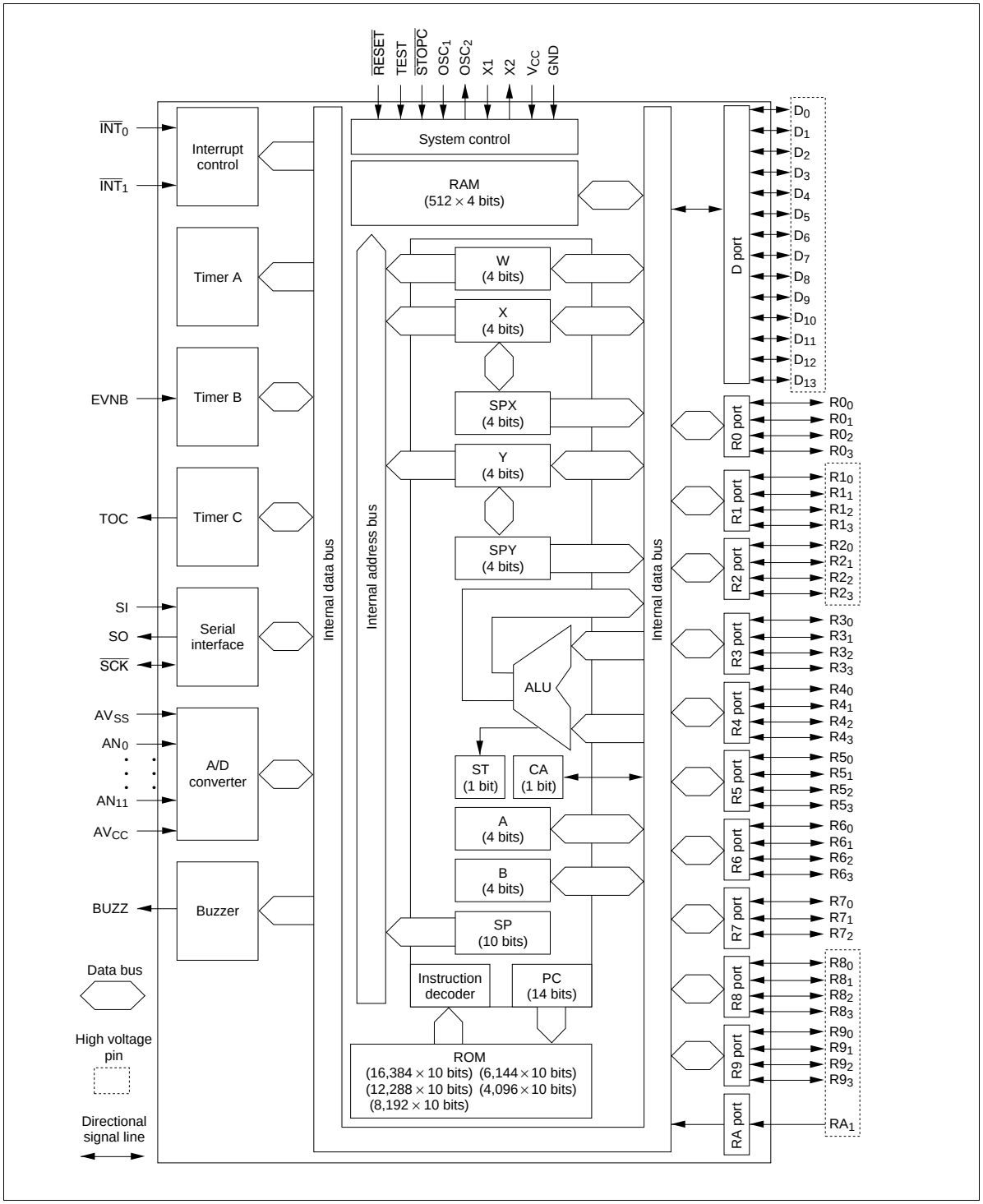
| Pin Number | | MCU Mode | | PROM Mode | |
|---|---|---|---|---|---|
| DP-64S | FP-64B | Pin | I/O | Pin | I/O |
| 1 | 59 | $R6_0$ | I/O | $O_4$ | I/O |
| 2 | 60 | $R6_1$ | I/O | $O_3$ | I/O |
| 3 | 61 | $R6_2$ | I/O | $O_2$ | I/O |
| 4 | 62 | $R6_3$ | I/O | $O_1$ | I/O |
| 5 | 63 | $R7_0$ | I/O | $O_0$ | I/O |
| 6 | 64 | $R7_1$ | I/O | | |
| 7 | 1 | $R7_2$ | I/O | | |
| 8 | 2 | $R0_0/\overline{SCK}$ | I/O | $V_{CC}$ | |
| 9 | 3 | $R0_1$/SI | I/O | $V_{CC}$ | |
| 10 | 4 | $R0_2$/SO | I/O | | |
| 11 | 5 | $R0_3$/TOC | I/O | | |
| 12 | 6 | TEST | I | $V_{PP}$ | |
| 13 | 7 | $\overline{RESET}$ | I | $\overline{RESET}$ | I |
| 14 | 8 | $OSC_1$ | I | $V_{CC}$ | |
| 15 | 9 | $OSC_2$ | O | | |
| 16 | 10 | GND | — | GND | |
| 17 | 11 | X1 | I | GND | |
| 18 | 12 | X2 | O | | |
| 19 | 13 | $AV_{SS}$ | — | GND | |
| 20 | 14 | $R3_0/AN_0$ | I/O | $O_0$ | I/O |
| 21 | 15 | $R3_1/AN_1$ | I/O | $O_1$ | I/O |
| 22 | 16 | $R3_2/AN_2$ | I/O | $O_2$ | I/O |
| 23 | 17 | $R3_3/AN_3$ | I/O | $O_3$ | I/O |
| 24 | 18 | $R4_0/AN_4$ | I/O | $O_4$ | I/O |
| 25 | 19 | $R4_1/AN_5$ | I/O | $O_5$ | I/O |
| 26 | 20 | $R4_2/AN_6$ | I/O | $O_6$ | I/O |
| 27 | 21 | $R4_3/AN_7$ | I/O | $O_7$ | I/O |
| 28 | 22 | $R5_0/AN_8$ | I/O | | |
| 29 | 23 | $R5_1/AN_9$ | I/O | | |
| 30 | 24 | $R5_2/AN_{10}$ | I/O | | |

| Pin Number | | MCU Mode | | PROM Mode | |
|---|---|---|---|---|---|
| **DP-64S** | **FP-64B** | **Pin** | **I/O** | **Pin** | **I/O** |
| 31 | 25 | $R5_3/AN_{11}$ | I/O | | |
| 32 | 26 | $AV_{CC}$ | — | $V_{CC}$ | |
| 33 | 27 | $V_{CC}$ | — | $V_{CC}$ | |
| 34 | 28 | $D_0/\overline{INT}_0$ | I/O | $M_0$ | I |
| 35 | 29 | $D_1/\overline{INT}_1$ | I/O | $M_1$ | I |
| 36 | 30 | $D_2$/EVNB | I/O | $A_1$ | I |
| 37 | 31 | $D_3$/BUZZ | I/O | $A_2$ | I |
| 38 | 32 | $D_4/\overline{STOPC}$ | I/O | | |
| 39 | 33 | $D_5$ | I/O | $A_3$ | I |
| 40 | 34 | $D_6$ | I/O | $A_4$ | I |
| 41 | 35 | $D_7$ | I/O | $A_9$ | I |
| 42 | 36 | $D_8$ | I/O | $V_{CC}$ | |
| 43 | 37 | $D_9$ | I/O | | |
| 44 | 38 | $D_{10}$ | I/O | | |
| 45 | 39 | $D_{11}$ | I/O | | |
| 46 | 40 | $D_{12}$ | I/O | | |
| 47 | 41 | $D_{13}$ | I/O | | |
| 48 | 42 | $R8_0$ | I/O | $\overline{CE}$ | I |
| 49 | 43 | $R8_1$ | I/O | $\overline{OE}$ | I |
| 50 | 44 | $R8_2$ | I/O | $A_{13}$ | I |
| 51 | 45 | $R8_3$ | I/O | $A_{14}$ | I |
| 52 | 46 | $R9_0$ | I/O | | |
| 53 | 47 | $R9_1$ | I/O | | |
| 54 | 48 | $R9_2$ | I/O | | |
| 55 | 49 | $R9_3$ | I/O | | |
| 56 | 50 | $R1_0$ | I/O | $A_5$ | I |
| 57 | 51 | $R1_1$ | I/O | $A_6$ | I |
| 58 | 52 | $R1_2$ | I/O | $A_7$ | I |
| 59 | 53 | $R1_3$ | I/O | $A_8$ | I |
| 60 | 54 | $R2_0$ | I/O | $A_0$ | I |
| 61 | 55 | $R2_1$ | I/O | $A_{10}$ | I |
| 62 | 56 | $R2_2$ | I/O | $A_{11}$ | I |
| 63 | 57 | $R2_3$ | I/O | $A_{12}$ | I |
| 64 | 58 | $RA_1/V_{disp}$ | I | | |

Notes: 1. I/O: Input/output pin; I: Input pin; O: Output pin

2. $O_0$ to $O_4$ consist of two pins each. Tie each pair together before using them.

## Block Diagram



## Memory Map

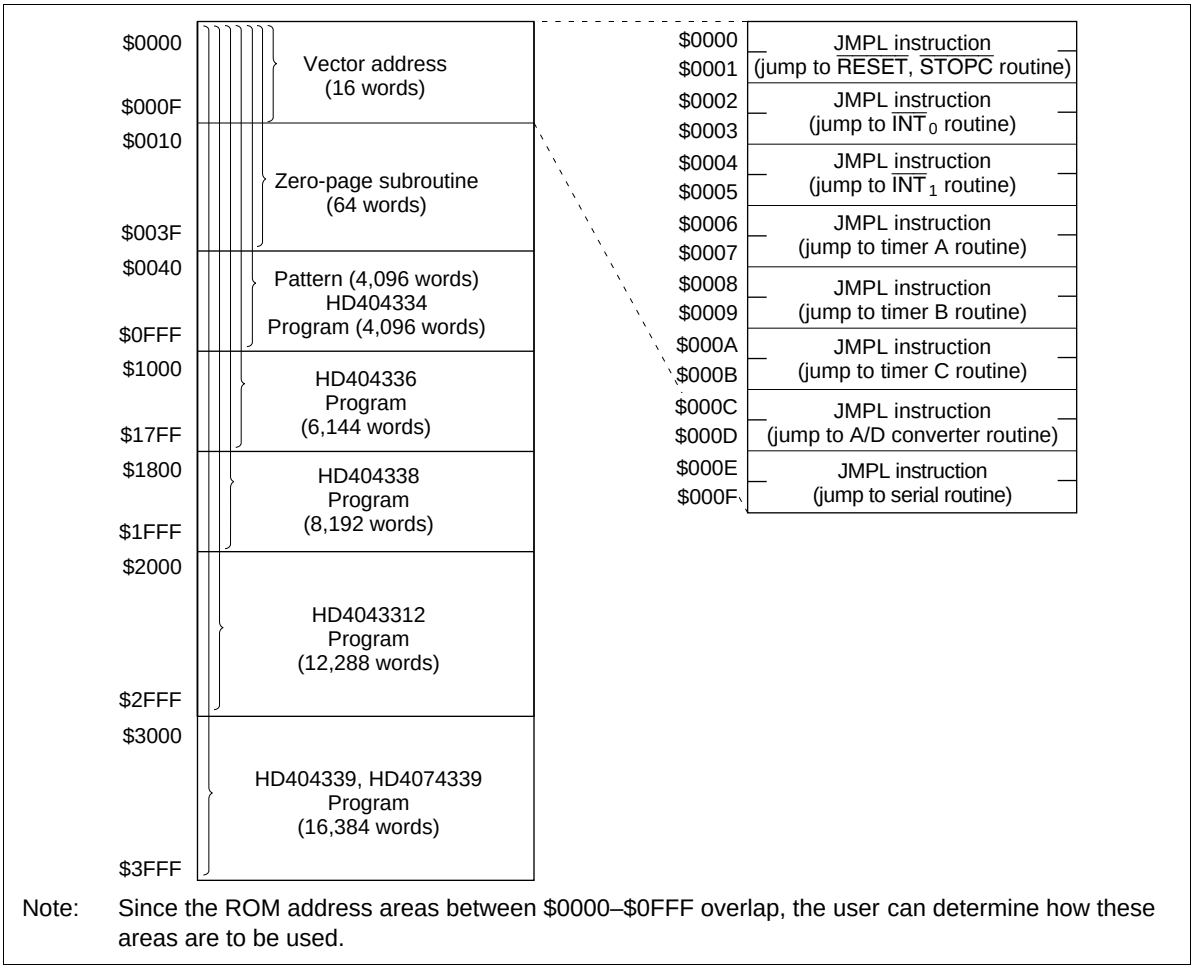
### ROM Memory Map

**Vector Address Area ($0000–$000F):** Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines.

**Zero-Page Subroutine Area ($0000–$003F):** Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

**Pattern Area ($0000–$0FFF):** Contains ROM data that can be referenced with the P instruction.

**Program Area ($0000-$0FFF (HD404334), $0000-$17FF (HD404336), $0000–$1FFF (HD404338), $0000–$2FFF (HD4043312), $0000–$3FFF (HD404339, HD4074339)):** The entire ROM area can be used for program coding.




Note: Since the ROM address areas between $0000–$0FFF overlap, the user can determine how these areas are to be used.

**Figure 1 ROM Memory Map**

## RAM Memory Map

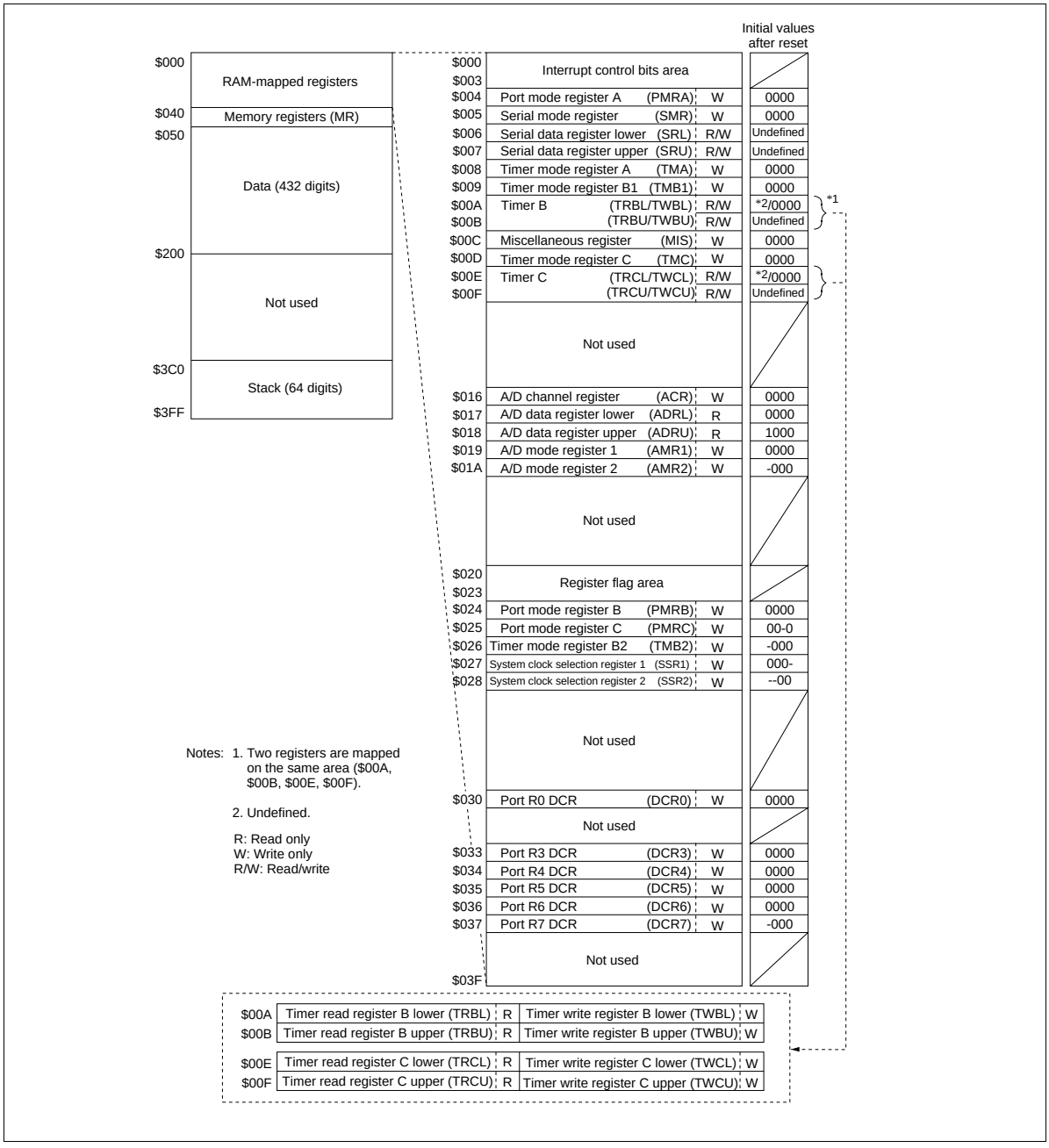



**Figure 2 RAM Memory Map and Initial Values**

**Table 1 Initial Values of Flags after MCU Reset**

| Item | | Initial Value |
|---|---|---|
| Interrupt flags/mask | Interrupt enable flag (IE) | 0 |
| | Interrupt request flag (IF) | 0 |
| | Interrupt mask (IM) | 1 |
| Bit registers | Watchdog timer on flag (WDON) | 0 |
| | A/D start flag (ADSF) | 0 |
| | Input capture status flag (ICSF) | 0 |
| | Input capture error flag (ICEF) | 0 |
| | $I_{AD}$ off flag (IAOF) | 0 |
| | RAM enable flag (RAME) | 0 |
| | Low speed on flag (LSON) | 0 |
| | Direct transfer on flag (DTON) | 0 |

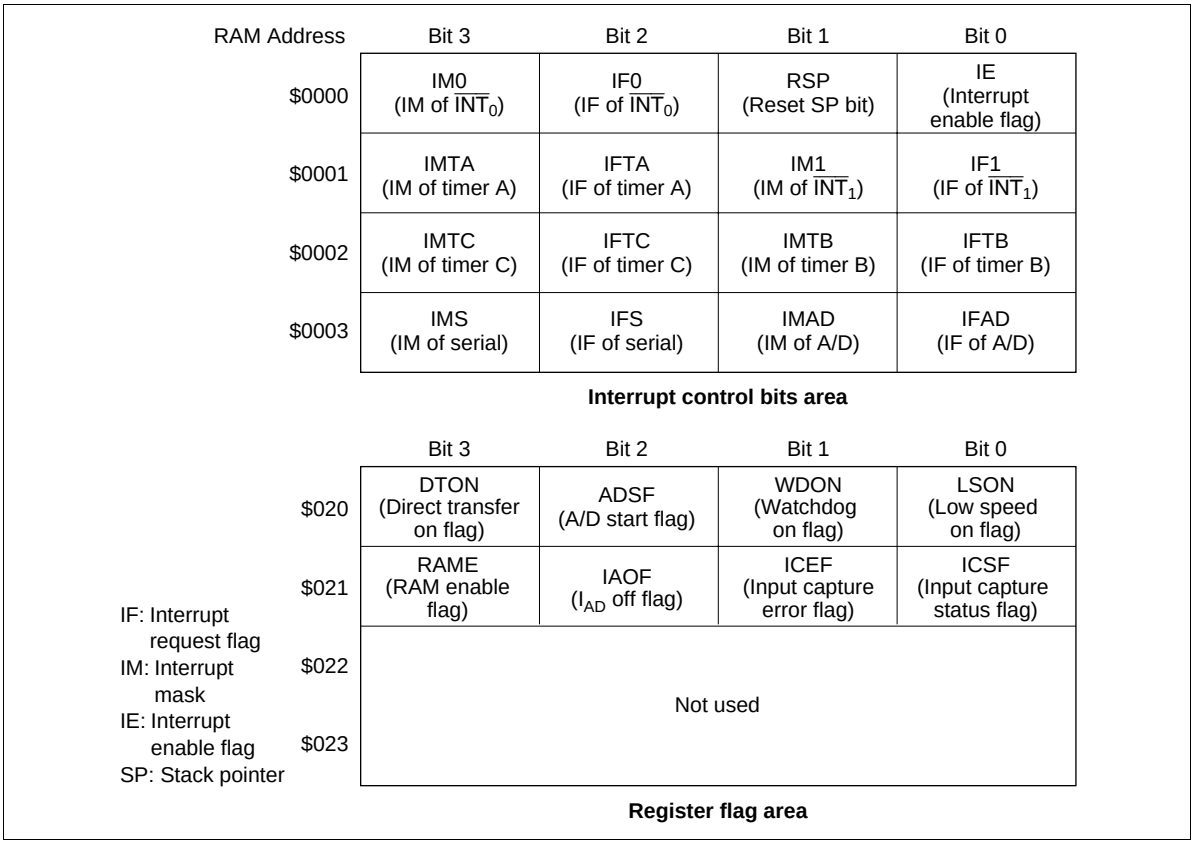
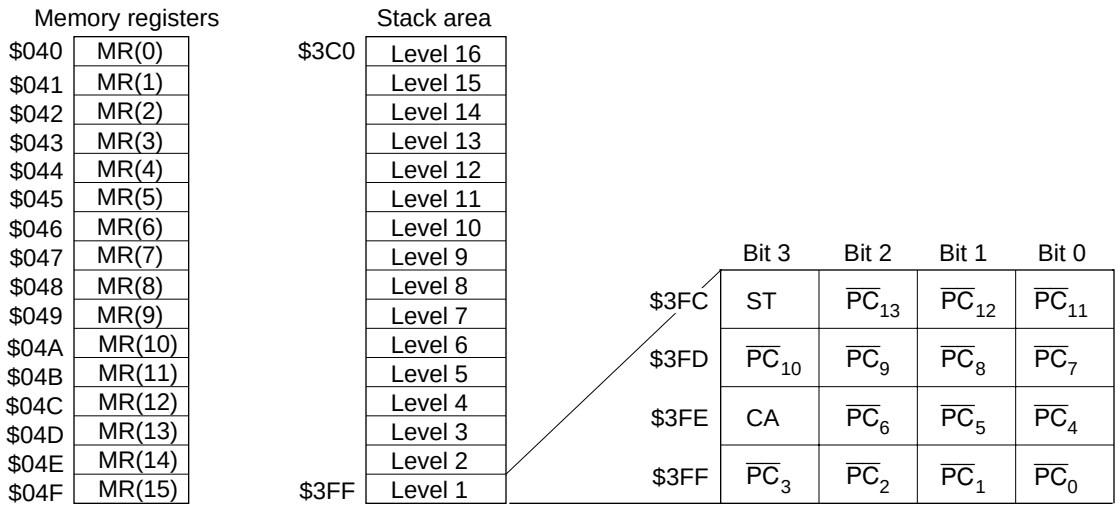



**Figure 3 Interrupt Control Bits and Register Flag Areas Configuration**

| | SEM/SEMD | REM/REMD | TM/TMD |
|---|---|---|---|
| IE | Allowed | Allowed | Allowed |
| IM | | | |
| LSON | | | |
| IAOF | | | |
| IF | Not executed | Allowed | Allowed |
| ICSF | | | |
| ICEF | | | |
| RAME | | | |
| RSP | Not executed | Allowed | Inhibited |
| WDON | Allowed | Not executed | Inhibited |
| ADSF | Allowed | Inhibited | Allowed |
| DTON | Not executed in active mode | Allowed | Allowed |
| | Used in subactive mode | | |
| Not used | Not executed | Not executed | Inhibited |

Note: WDON is reset by MCU reset or by STOPC enable for stop mode cancellation.
The REM or REMD instruction must not be executed for ADSF during A/D conversion.
DTON is always reset in active mode. If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

**Figure 4 Usage Limitations of RAM Bit Manipulation Instructions**




$PC_{13}$–$PC_0$ : Program counter
ST: Status flag
CA: Carry flag

**Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position**

## Registers and Flags

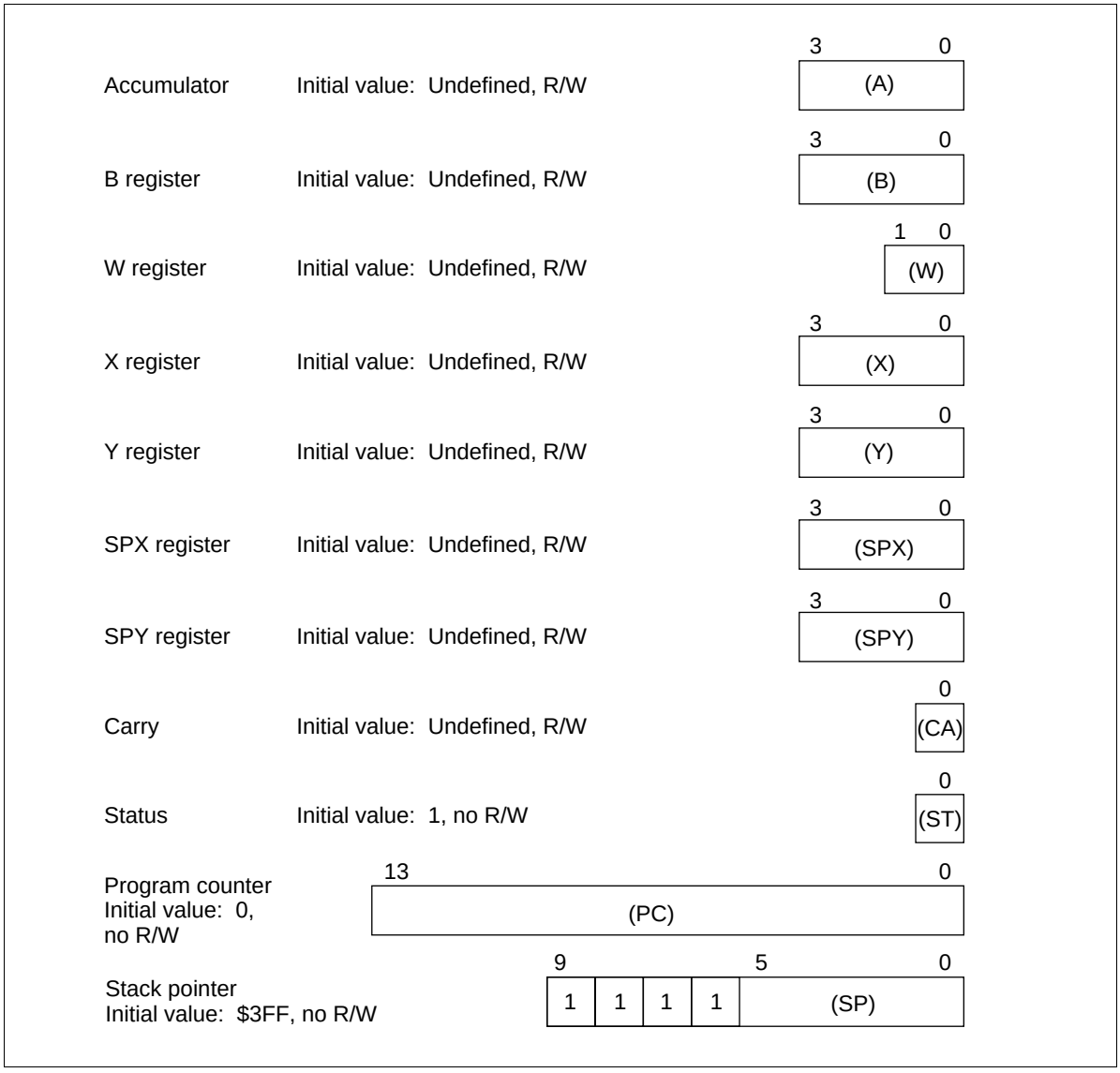



**Figure 6 Registers and Flags**

## Addressing Modes

### RAM Addressing Modes

**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

**Memory Register Addressing Mode (LAMR, XMRA):** The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

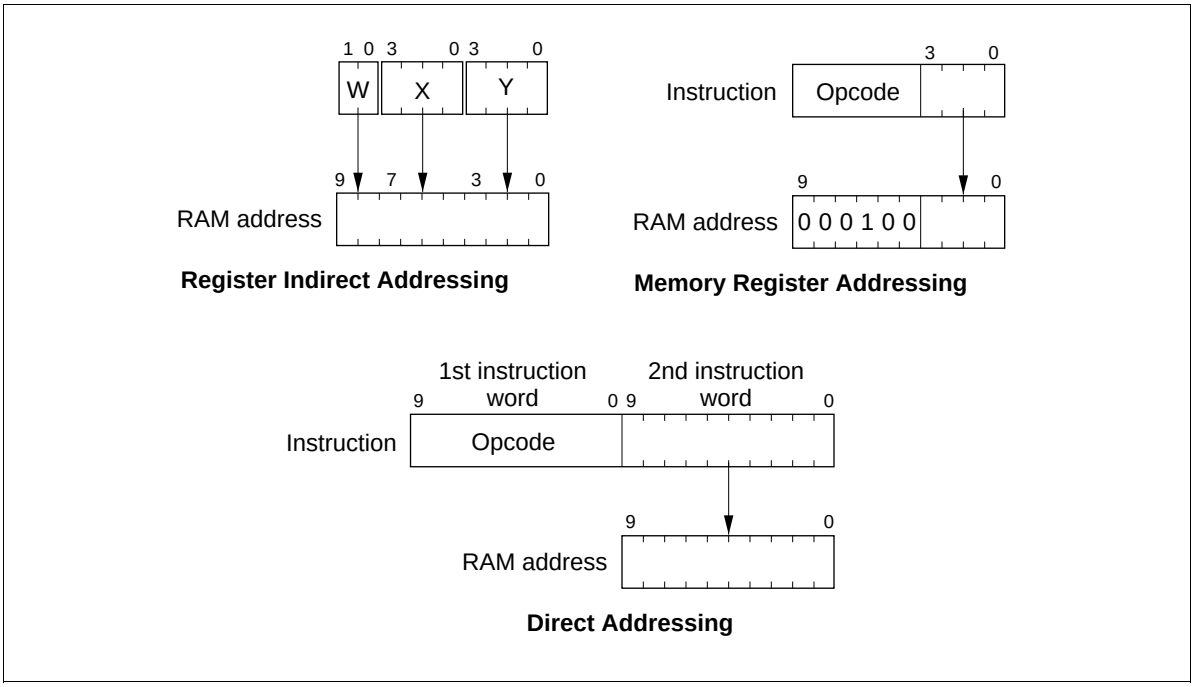



**Figure 7 RAM Addressing Modes**

**ROM Addressing Modes**

**Direct Addressing Mode:** A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

**Current Page Addressing Mode:** A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

**Zero-Page Addressing Mode:** A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

**Table Data Addressing Mode:** A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

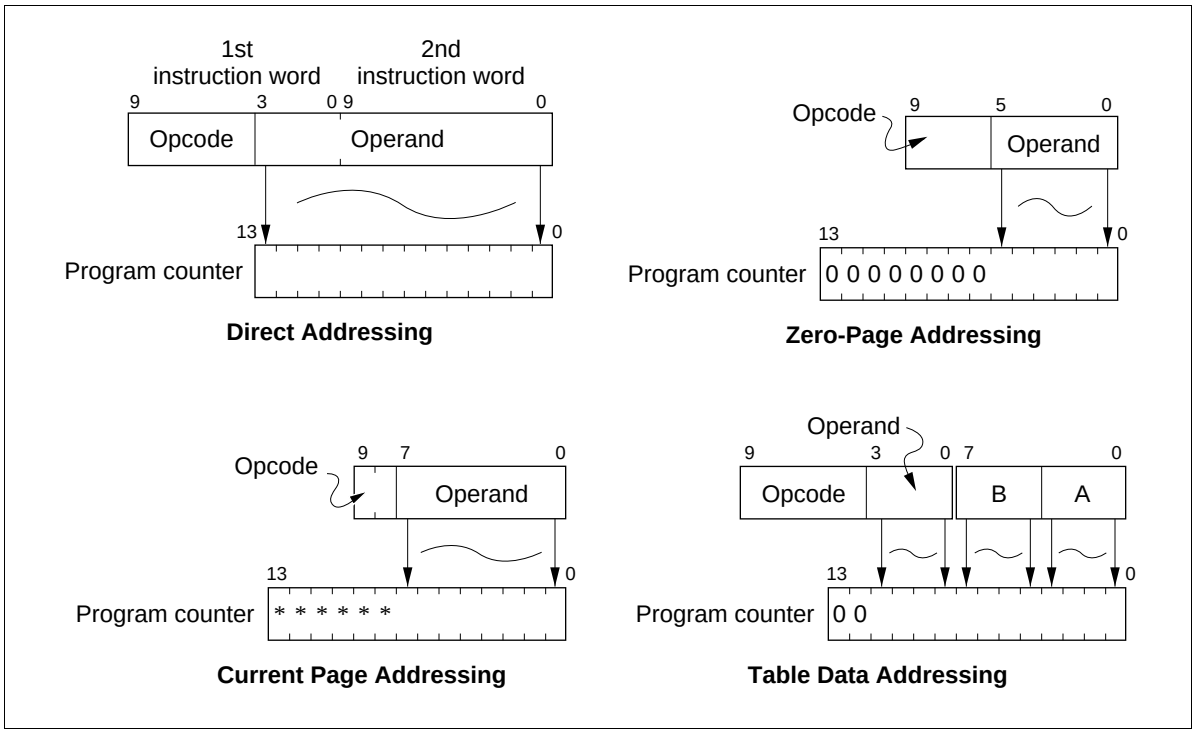



**Figure 8 ROM Addressing Modes**

## Instruction Set

**Table 2 Instruction Set Classification**

| Instruction Type | Function | Number of Instructions |
|---|---|---|
| Immediate | Transferring constants to the accumulator, B register, and RAM. | 4 |
| Register-to-register | Transferring contents of the B, Y, SPX, SPY, or memory registers to the accumulator. | 8 |
| RAM addressing | Available when accessing RAM in register indirect addressing mode. | 13 |
| RAM register | Transferring data between the accumulator and memory. | 10 |
| Arithmetic | Performing arithmetic operations with the contents of the accumulator, B register, or memory. | 25 |
| Compare | Comparing contents of the accumulator or memory with a constant. | 12 |
| RAM bit manipulation | Bit set, bit reset, and bit test. | 6 |
| ROM addressing | Branching and jump instructions based on the status condition. | 8 |
| Input/output | Controlling the input/output of the R and D ports; ROM data reference with the P instruction. | 11 |
| Control | Controlling the serial communication interface and low-power dissipation modes. | 4 |
| | | Total: 101 instructions |

## Interrupts

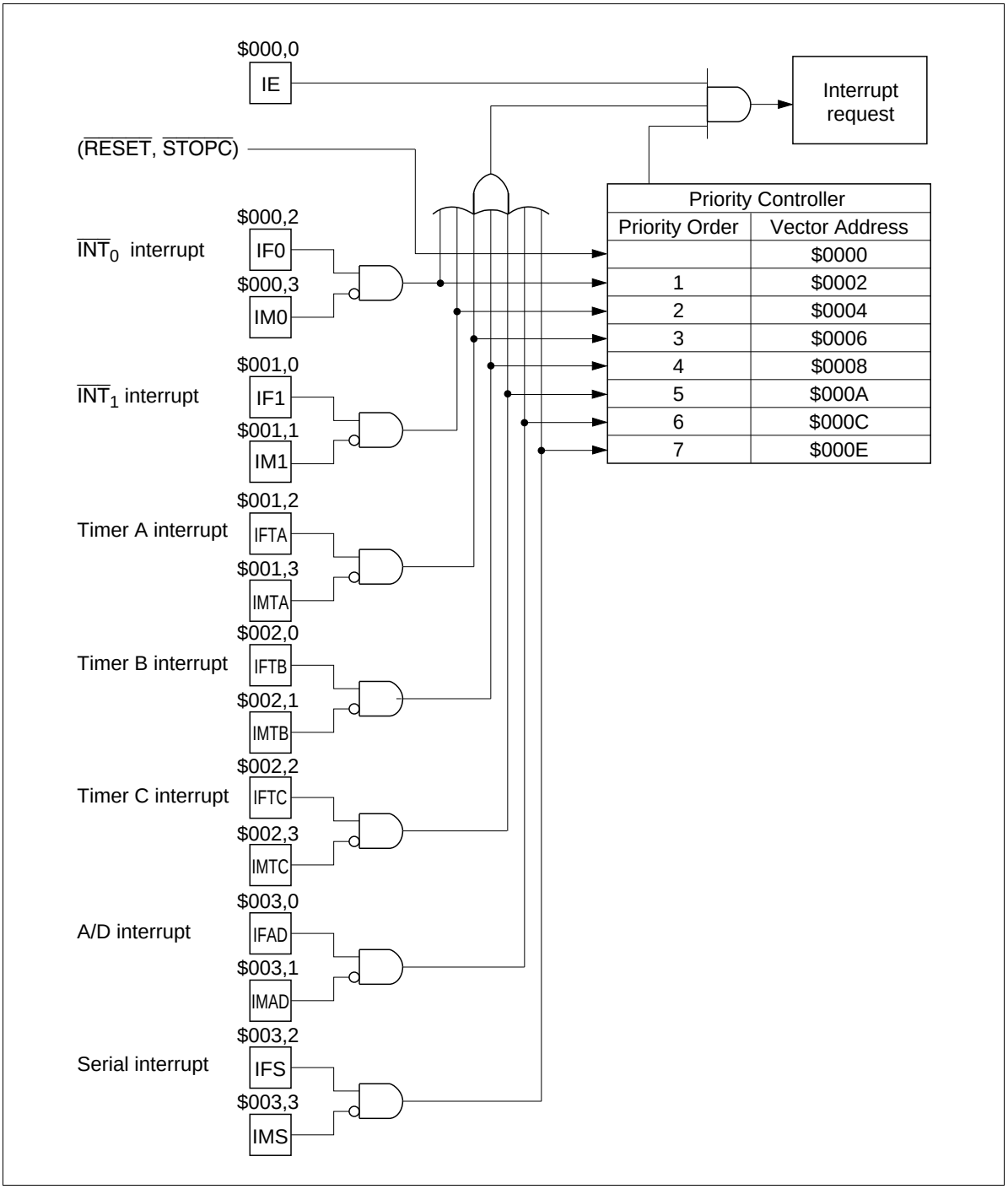
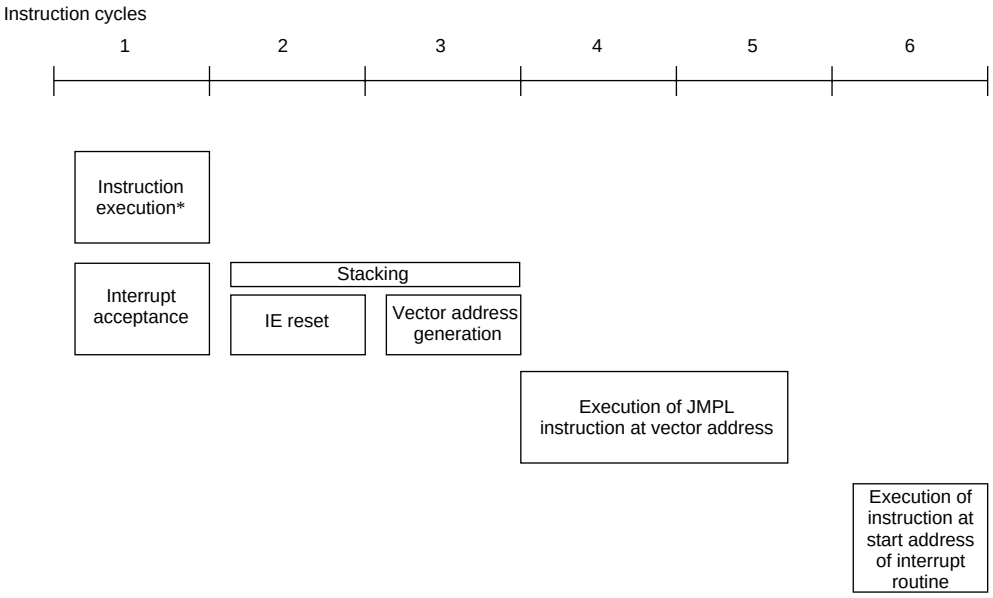



**Figure 9 Interrupt Control Circuit**




Note: * The stack is accessed and the interrupt enable flag is reset after the instruction is executed, even if it is a two-cycle instruction.

**Figure 10 Interrupt Processing Sequence**

## Operating Modes

The MCU has five operating modes as shown in table 3. Transitions between operating modes are shown in figure 11.

**Table 3 Operations in Each Operating Mode**

| Function | Active Mode | Subactive Mode | Standby Mode | Watch Mode | Stop Mode |
|---|---|---|---|---|---|
| System oscillator | OP | Stopped | OP | Stopped | Stopped |
| Subsystem oscillator | OP | OP | OP | OP | * OP |
| CPU | OP | OP | Retained | Retained | Reset |
| RAM | OP | OP | Retained | Retained | Retained |
| Timer A | OP | OP | OP | OP | Reset |
| Timers B, C | OP | OP | OP | Stopped | Reset |
| Serial | OP | OP | OP | Stopped | Reset |
| A/D | OP | Stopped | OP | Stopped | Reset |
| I/O | OP | OP | Retained | Retained | Reset |

Notes: OP implies in operation.

* Oscillation can be switched on or off with bit 3 of system clock selection register 1 (SSR1: $027).

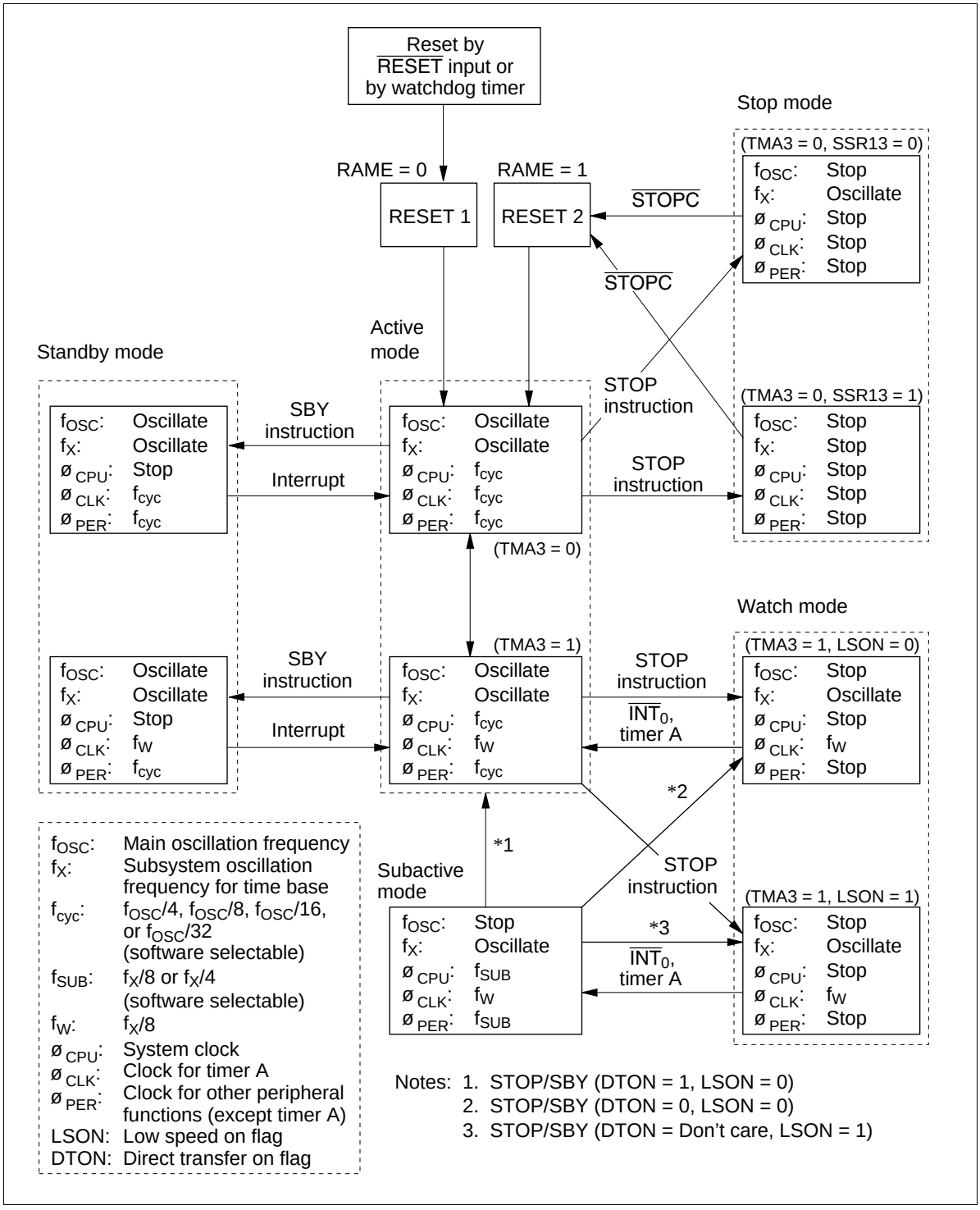



**Figure 11 MCU Status Transitions**

In stop mode, the system oscillator is stopped. To ensure a proper oscillation stabilization period of at least $t_{RC}$ when clearing stop mode, execute the cancellation according to the timing chart in figure 12.

In watch and subactive modes, a timer A or $\overline{INT_0}$ interrupt can be accepted during the interrupt frame period T (see figure 13).

Note: In watch and subactive modes, an interrupt will not be properly detected if the $\overline{INT_0}$ high or low level period is shorter than the interrupt frame period T. Thus, when operating in watch and subactive modes, maintain the $\overline{INT_0}$ high or low level period longer than period T to ensure interrupt detection.

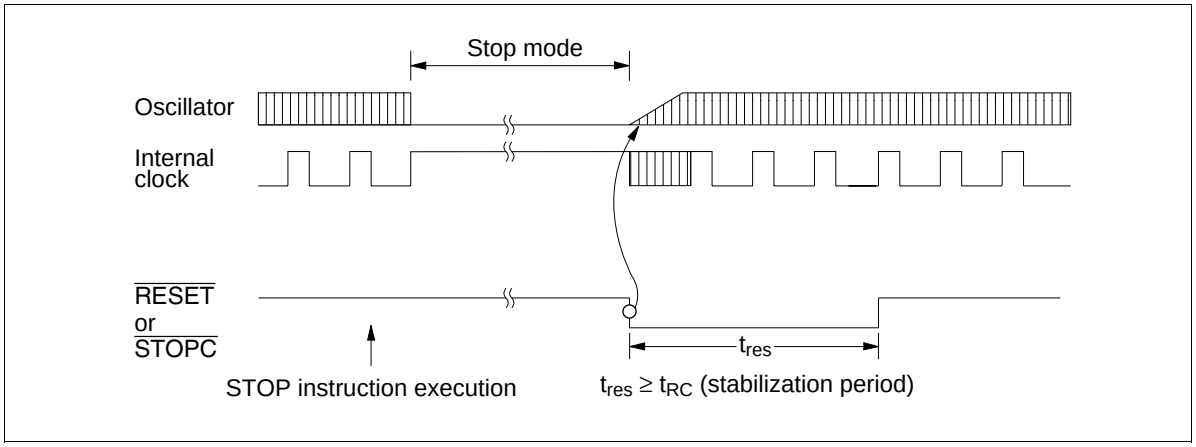



**Figure 12 Timing of Stop Mode Cancellation**

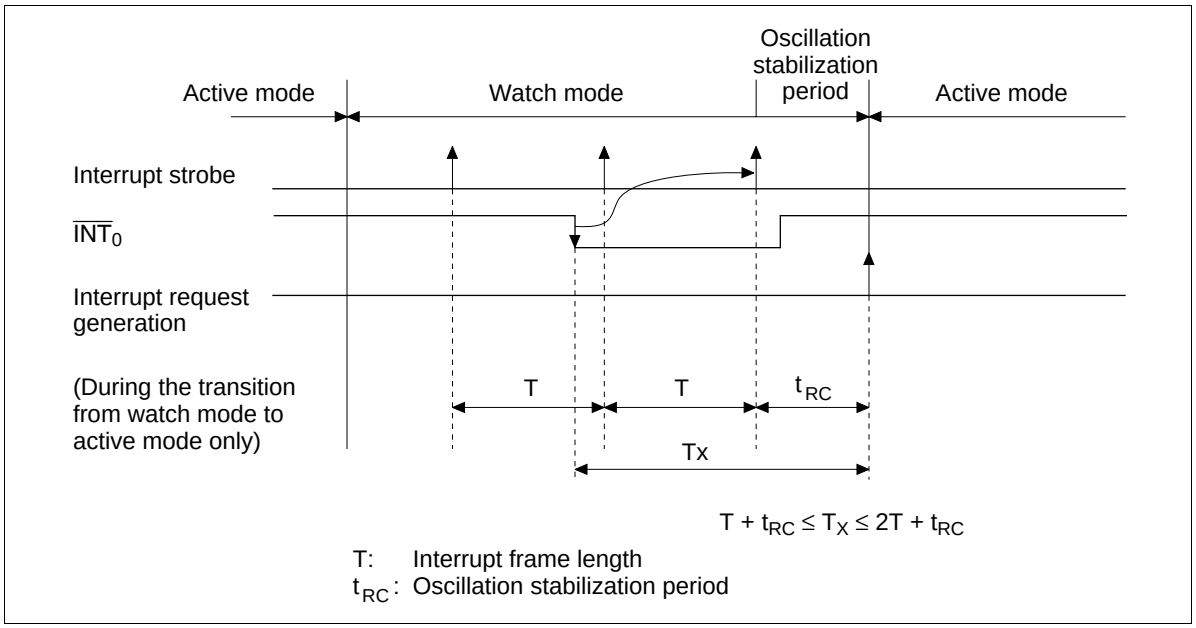



**Figure 13 Interrupt Frame**

The MCU automatically provides an oscillation stabilization period $t_{RC}$ when operation switches from watch mode to active mode. The interrupt frame period T and one of three values for $t_{RC}$ can be selected with the miscellaneous register (MIS: $00C), as listed in figure 14.

Operation can switch directly from subactive mode to active mode, as illustrated in figure 15. In this case, the transition time $T_D$ obeys the following relationship.

$t_{RC} < T_D < T + t_{RC}$

**Miscellaneous register (MIS: $00C)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | MIS3 | MIS2 | MIS1 | MIS0 |

| MIS3 | MIS2 | MIS1 | MIS0 | T*1 | $t_{RC}$*1 | Oscillation Circuit Conditions |
|---|---|---|---|---|---|---|
| Buffer control. Refer to figure 24. | | 0 | 0 | 0.24414 ms | 0.12207 ms | External clock input |
| | | | | | 0.24414 ms*2 | |
| | | 0 | 1 | 15.625 ms | 7.8125 ms | Ceramic oscillator |
| | | 1 | 0 | 125 ms | 62.5 ms | Crystal oscillator |
| | | 1 | 1 | Not used | | — |

Notes: 1. The values of T and $t_{RC}$ are applied when a 32.768-kHz crystal oscillator is used.
2. The value is applied only when direct transfer operation is used.

**Figure 14 Miscellaneous Register**

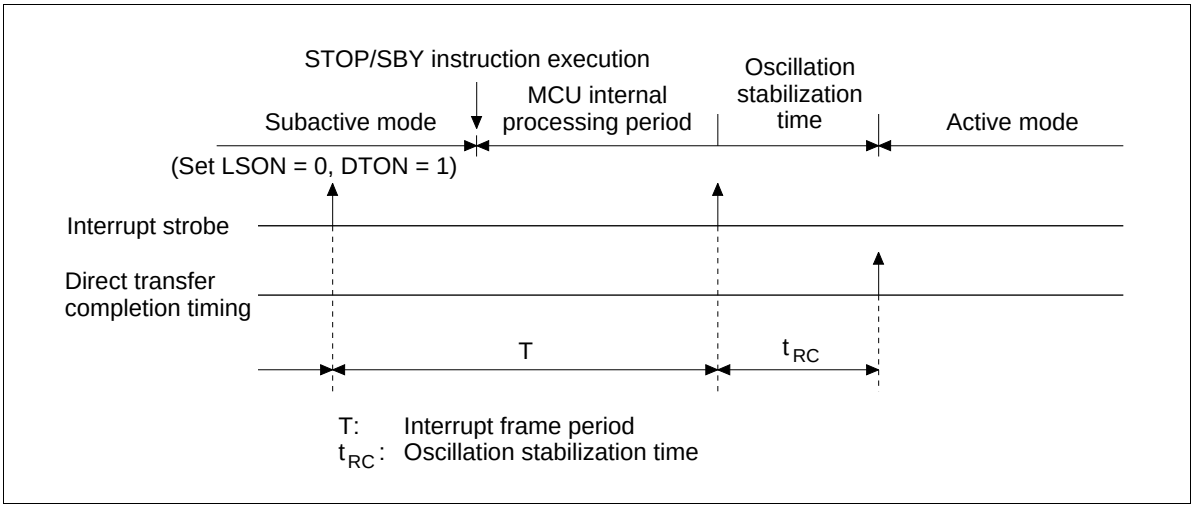



**Figure 15 Direct Transition Timing**

**MCU Operation Sequence:** The MCU operation flow is shown in figures 16 and 17. $\overline{\text{RESET}}$ input is asynchronous, and causes an immediate transition to the reset state from any MPU operation state.

The low-power mode operation sequence is shown in figure 17. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

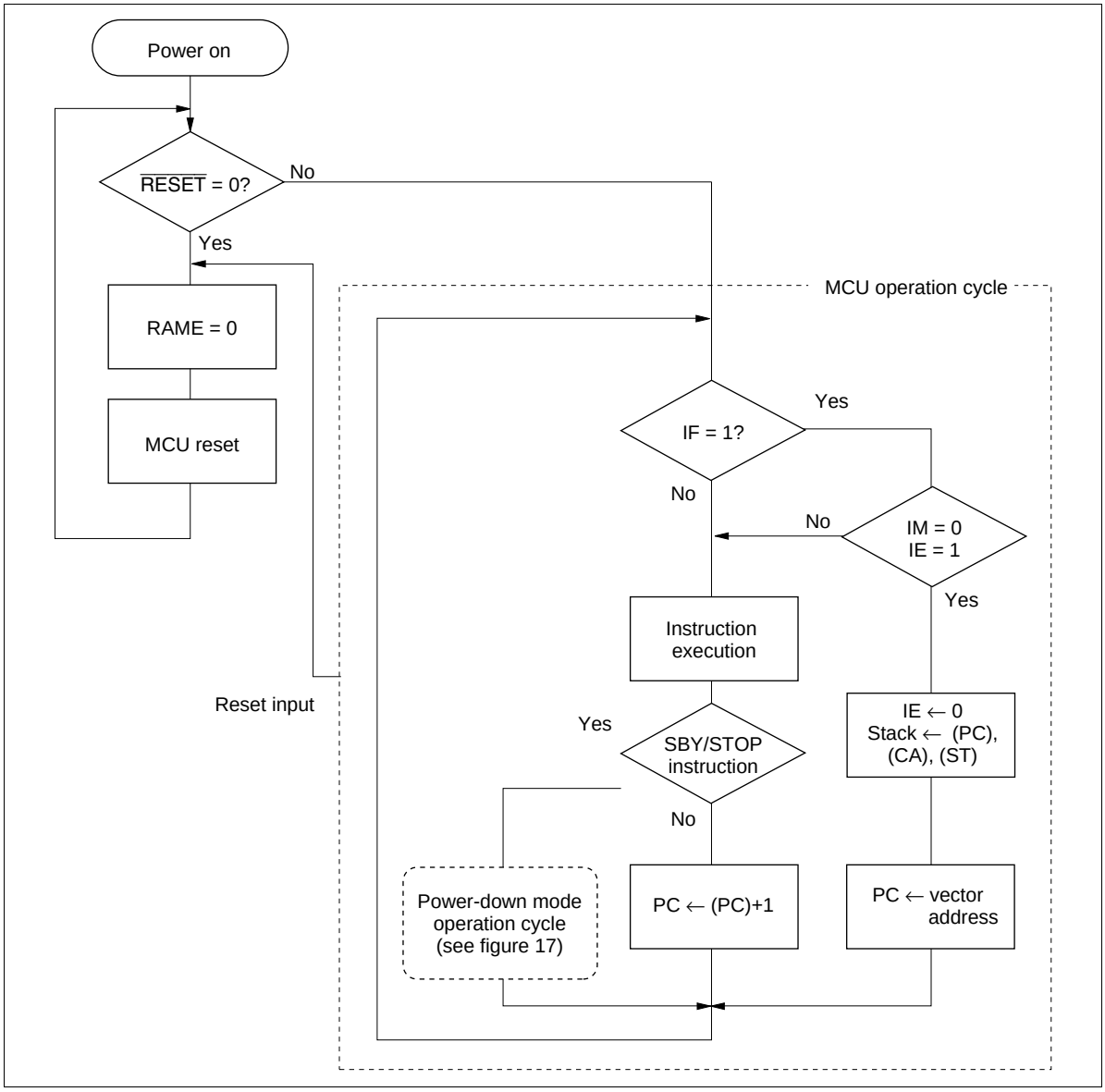



**Figure 16 MCU Operation Sequence (Power On)**

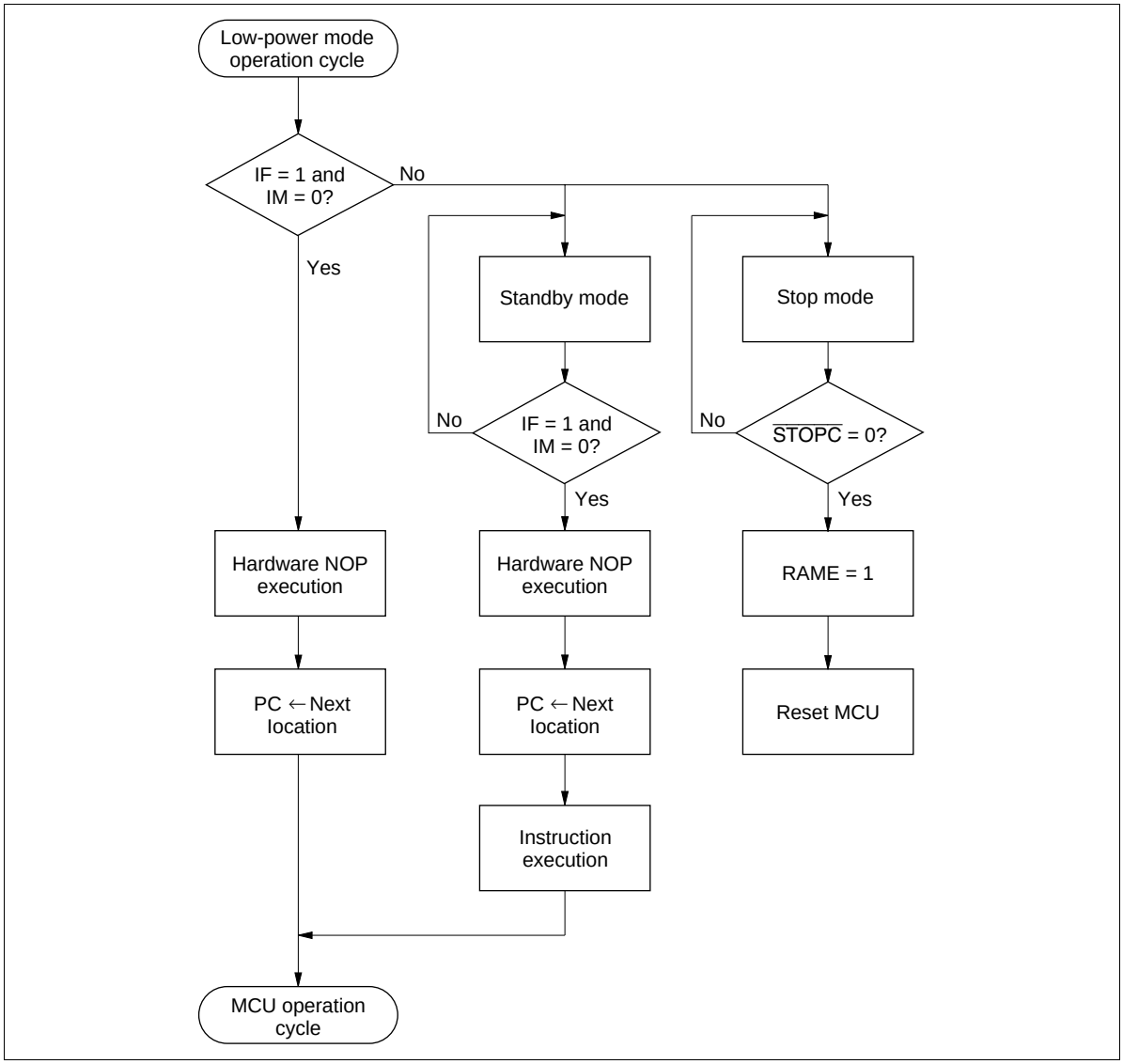
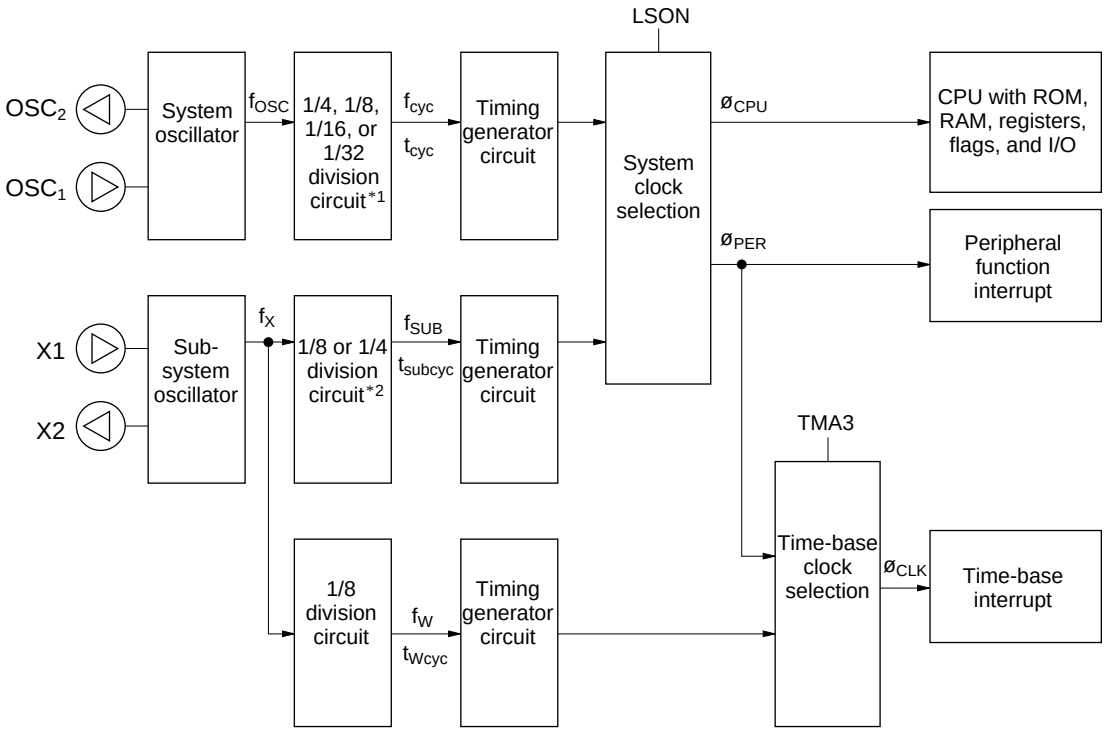



**Figure 17 MCU Operating Sequence (Low-Power Mode Operation)**

## Oscillator Circuit

Figure 18 shows a block diagram of the clock generation circuit. The system clock frequency of the oscillator connected to $OSC_1$ and $OSC_2$ can be selected by system clock selection registers 1 and 2 (SSR1, 2: $027, $028) as shown in figures 20 and 21.

The system clock division ratio can be set by software to be 1/4, 1/8, 1/16, or 1/32. The subsystem clock division ratio can be set by software to be 1/4 or 1/8.




Notes: 1. The system clock division ratio can be selected by setting bit 1 or 0 of the system clock select register 2 (SSR2: $028).

2. The system clock division ratio can be selected by setting bit 2 of the system clock select register 1 (SSR1: $027).

**Figure 18 Clock Generation Circuit**

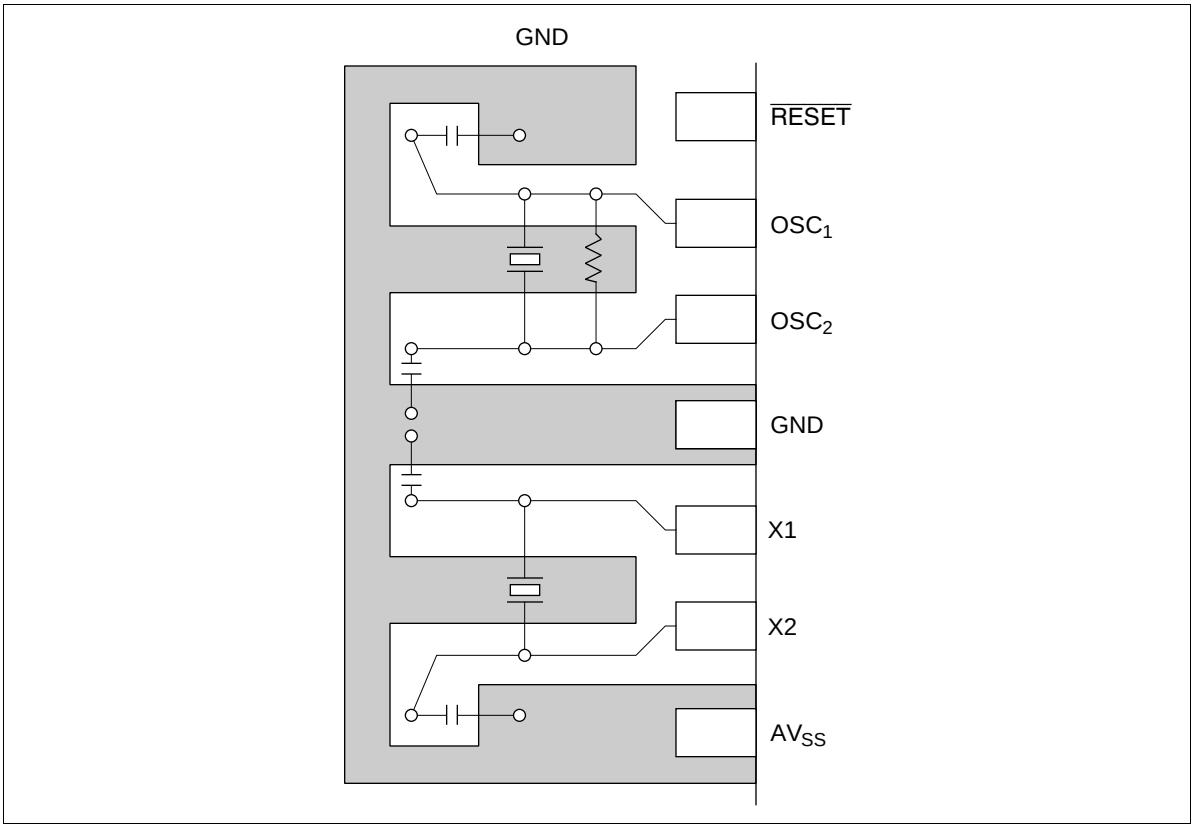
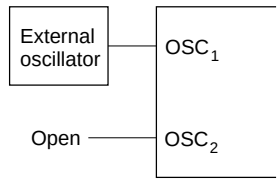
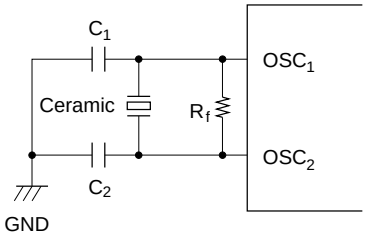
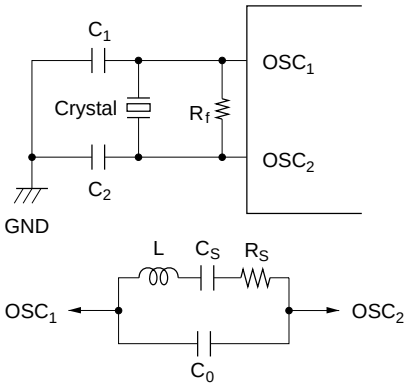
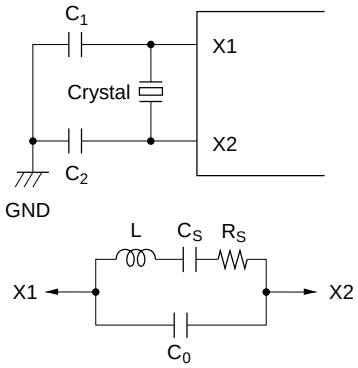



**Figure 19 Typical Layout of Crystal and Ceramic Oscillators**

**Table 4 Oscillator Circuit Examples**

| | Circuit Configuration | Circuit Constants |
|---|---|---|
| External clock operation |  | |
| Ceramic oscillator ($OSC_1$, $OSC_2$) |  | Ceramic oscillator: CSA4.00MG (Murata)<br>$R_f$ = 1 MΩ ±20%<br>$C_1 = C_2$ = 30 pF ±20% |
| Crystal oscillator ($OSC_1$, $OSC_2$) |  | $R_f$ = 1 MΩ ±20%<br>$C_1 = C_2$ = 10 to 22 pF ±20%<br>Crystal: Equivalent to circuit shown below<br>$C_0$ = 7 pF max.<br>$R_S$ = 100 Ω max. |
| Crystal oscillator (X1, X2) |  | Crystal: 32.768 kHz: MX38T (Nippon Denpa)<br>$C_1 = C_2$ = 20 pF ±20%<br>$R_S$ = 14 kΩ<br>$C_0$ = 1.5 pF |

Notes:
1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.
2. Wiring among $OSC_1$, $OSC_2$, X1, X2 and elements should be as short as possible, and must not cross other wiring (see figure 19).
3. When a 32.768-kHz crystal oscillator is not used, fix pin X1 to GND and leave pin X2 open.

**System clock selection register 1 (SSR1: $027)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | — |
| Read/Write | W | W | W | — |
| Bit name | SSR13*1 | SSR12 | SSR11 | Not used |

| SSR11 | System Clock Selection*2 |
|---|---|
| 0 | 0.4 to 1.0 MHz |
| 1 | 1.6 to 4.5 MHz |

| SSR12 | 32-kHz Oscillation Division Ratio Selection |
|---|---|
| 0 | $f_{SUB} = f_X/8$ |
| 1 | $f_{SUB} = f_X/4$ |

| SSR13 | 32-kHz Oscillation Stop |
|---|---|
| 0 | Oscillation operates in stop mode |
| 1 | Oscillation stops in stop mode |

Notes: *1 SSR13 will only be cleared to 0 by a $\overline{\text{RESET}}$ input. A $\overline{\text{STOPC}}$ input during stop mode will not clear SSR13. Also note that SSR13 will not be cleared upon transition to stop mode.

*2 When the subsystem oscillator (32.768 kHz crystal oscillator) is used, set 0.4 MHz≤ $f_{OSC}$ ≤ 1.0MHz or 1.6 MHz ≤ $f_{OSC}$ ≤ 4.5 MHz.

**Figure 20 System Clock Selection Register 1 (SSR1)**

**System clock selection register 2 (SSR2: $028)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | — | — | 0 | 0 |
| Read/Write | — | — | W | W |
| Bit name | Not used | Not used | SSR21 | SSR20 |

| SSR21 | SSR20 | System Clock Division Ratio |
|---|---|---|
| 0 | 0 | 1/4 division |
| 0 | 1 | 1/8 division |
| 1 | 0 | 1/16 division |
| 1 | 1 | 1/32 division |

**Figure 21 System Clock Selection Register 2 (SSR2)**

## I/O Ports

The MCU has 53 input/output pins ($D_0$–$D_{13}$, $R0_0$–$R9_3$) and one input-only pin ($RA_1$).

- The 30 pins consisting of ports $D_0$–$D_{13}$, R1, R2, R8, and R9 are all high-voltage I/O pins. $RA_1$ is a high-voltage input-only pin. The high-voltage pins can be equipped with or without pull-down resistance, as selected by the mask option.
- All standard voltage output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed for NMOS open-drain output.
- In stop mode, input/output pins go to the high-impedance state.
- All standard voltage input/output pins have pull-up MOS built in, which can be individually turned on or off by software (Table 5).

  Pull-up MOS on/off settings can be made independently of settings as on-chip supporting module pins.

**Table 5 Control of Standard I/O Pins by Program**

| **MIS3 (bit 3 of MIS)** | | **0** | | | | **1** | | | |
|---|---|---|---|---|---|---|---|---|---|
| **DCR** | | **0** | | **1** | | **0** | | **1** | |
| **PDR** | | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** |
| CMOS buffer | PMOS | — | — | — | On | — | — | — | On |
| | NMOS | — | — | On | — | — | — | On | — |
| Pull-up MOS | | — | — | — | — | — | On | — | On |

Note: — indicates off.

**Data control register (DCR0: $030, DCR3 to DCR7: $033 to $037)**

**DCR0, DCR3 to DCR7**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | DCR03, DCR33 to DCR63 | DCR02, DCR32 to DCR72 | DCR01, DCR31 to DCR71 | DCR00, DCR30 to DCR70 |

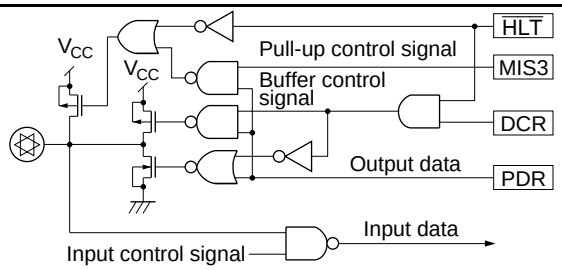
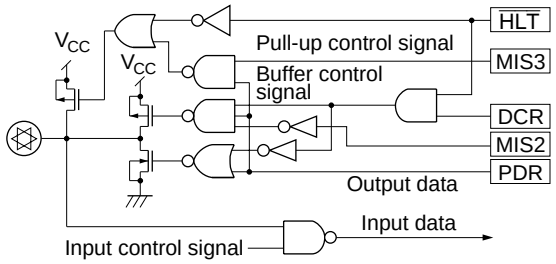
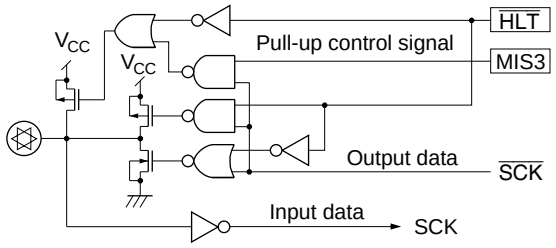
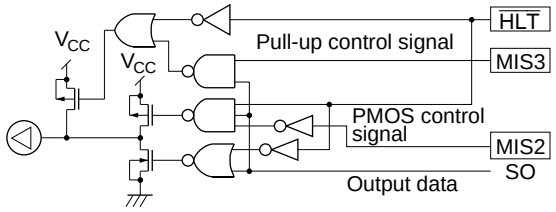
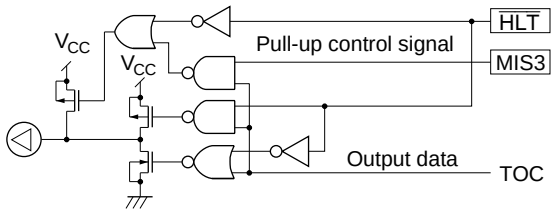
| Bits 0 to 3 | CMOS Buffer Control |
|---|---|
| 0 | CMOS buffer off (high impedance) |
| 1 | CMOS buffer on |

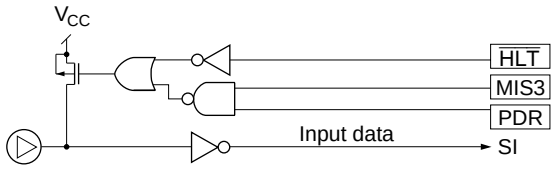
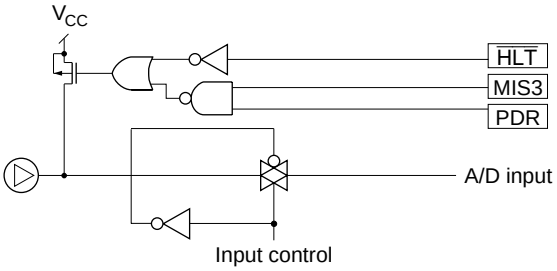
Correspondence between ports and DCR bits

| Register | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| DCR0 | $R0_3$ | $R0_2$ | $R0_1$ | $R0_0$ |
| DCR3 | $R3_3$ | $R3_2$ | $R3_1$ | $R3_0$ |
| DCR4 | $R4_3$ | $R4_2$ | $R4_1$ | $R4_0$ |
| DCR5 | $R5_3$ | $R5_2$ | $R5_1$ | $R5_0$ |
| DCR6 | $R6_3$ | $R6_2$ | $R6_1$ | $R6_0$ |
| DCR7 | Not used | $R7_2$ | $R7_1$ | $R7_0$ |

**Figure 22 Data Control Register (DCR)**

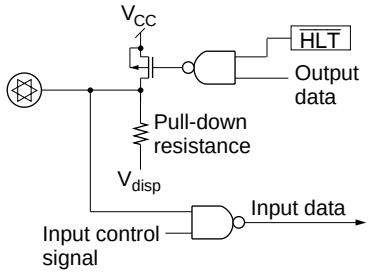
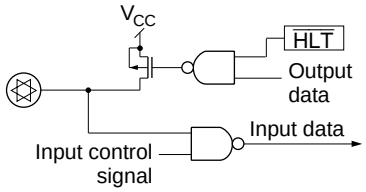
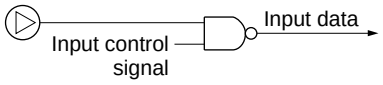
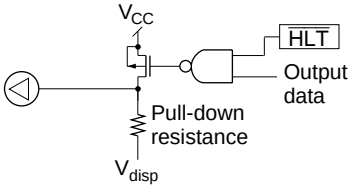
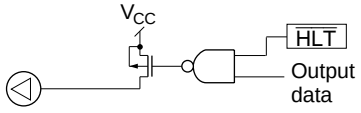
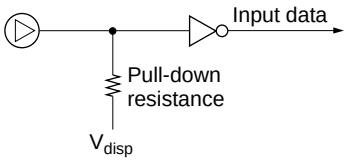
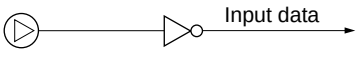
**Table 6 Circuit Configurations of Standard I/O Pins**

| I/O Pin Type | | Circuit | Pins |
|---|---|---|---|
| Input/output pins | |  | $R0_0$, $R0_1$, $R0_3$,<br>$R3_0$–$R3_3$,<br>$R4_0$–$R4_3$,<br>$R5_0$–$R5_3$,<br>$R6_0$–$R6_3$,<br>$R7_0$–$R7_2$ |
| | |  | $R0_2$ |
| Peripheral function pins | Input/ output pins |  | $\overline{SCK}$ |
| | Output pins |  | SO |
| | |  | TOC |

| I/O Pin Type | | Circuit | Pins |
|---|---|---|---|
| Peripheral function pins | Input/ pins |  | SI |
| | |  | $AN_0$–$AN_{11}$ |

Notes: 1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The $\overline{HLT}$ signal goes low, and input/output pins enter the high-impedance state.
2. The $\overline{HLT}$ signal is 1 in active, standby, watch, and subactive modes.

**Table 7 Circuit Configurations for High-Voltage Input/Output Pins**

| I/O Pin Type | | With Pull-Down Resistance | Without Pull-Down Resistance | Pins |
|---|---|---|---|---|
| Input/output pins | |  |  | $D_0$–$D_{13}$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R8_0$–$R8_3$, $R9_0$–$R9_3$ |
| Input pins | | |  | $RA_1$ |
| Peripheral function pins | Output pins |  |  | BUZZ |
| | Input pins |  |  | $\overline{INT}_0$, $\overline{INT}_1$, EVNB, $\overline{STOPC}$ |

Note: $\overline{HLT}$ goes high in active, standby, watch, and subactive modes.

**Port mode register A (PMRA: $004)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | PMRA3 | PMRA2 | PMRA1 | PMRA0 |

| PMRA2 | $R0_3$/TOC Mode Selection |
|---|---|
| 0 | $R0_3$ |
| 1 | TOC |

| PMRA3 | $D_3$/BUZZ Mode Selection |
|---|---|
| 0 | $D_3$ |
| 1 | BUZZ |

| PMRA0 | $R0_2$/SO Mode Selection |
|---|---|
| 0 | $R0_2$ |
| 1 | SO |

| PMRA1 | $R0_1$/SI Mode Selection |
|---|---|
| 0 | $R0_1$ |
| 1 | SI |

**Figure 23 Port Mode Register A (PMRA)**

**Port mode register B (PMRB: $024)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | PMRB3* | PMRB2 | PMRB1 | PMRB0 |

| PMRB2 | $D_2$/EVNB Mode Selection |
|---|---|
| 0 | $D_2$ |
| 1 | EVNB |

| PMRB3 | $D_4$/$\overline{\text{STOPC}}$ Mode Selection |
|---|---|
| 0 | $D_4$ |
| 1 | $\overline{\text{STOPC}}$ |

| PMRB0 | $D_0$/$\overline{INT}_0$ Mode Selection |
|---|---|
| 0 | $D_0$ |
| 1 | $\overline{INT}_0$ |

| PMRB1 | $D_1$/$\overline{INT}_1$ Mode Selection |
|---|---|
| 0 | $D_1$ |
| 1 | $\overline{INT}_1$ |

Note: * PMRB3 is reset to 0 only by $\overline{\text{RESET}}$ input. When $\overline{\text{STOPC}}$ is input in stop mode, PMRB3 is not reset but retains its value.

**Figure 24 Port Mode Register B (PMRB)**

**Miscellaneous register (MIS: $00C)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | MIS3 | MIS2 | MIS1 | MIS0 |

| MIS3 | Pull-Up MOS On/Off Selection |
|---|---|
| 0 | Pull-up MOS off |
| 1 | Pull-up MOS on (refer to table 5) |

| MIS2 | CMOS Buffer On/Off Selection for Pin $R0_2$/SO |
|---|---|
| 0 | CMOS on |
| 1 | CMOS off |

| MIS1 | MIS0 |
|---|---|
| $t_{RC}$ selection. Refer to figure 14 in the operation modes section. | |

Note: The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

**Figure 25 Miscellaneous Register**

## Prescaler

The MCU has two built-in prescalers, S and W (PSS, PSW). They divide the system clock and subsystem clock, and output these divided clocks to the peripheral function modules, as shown in figure 26.

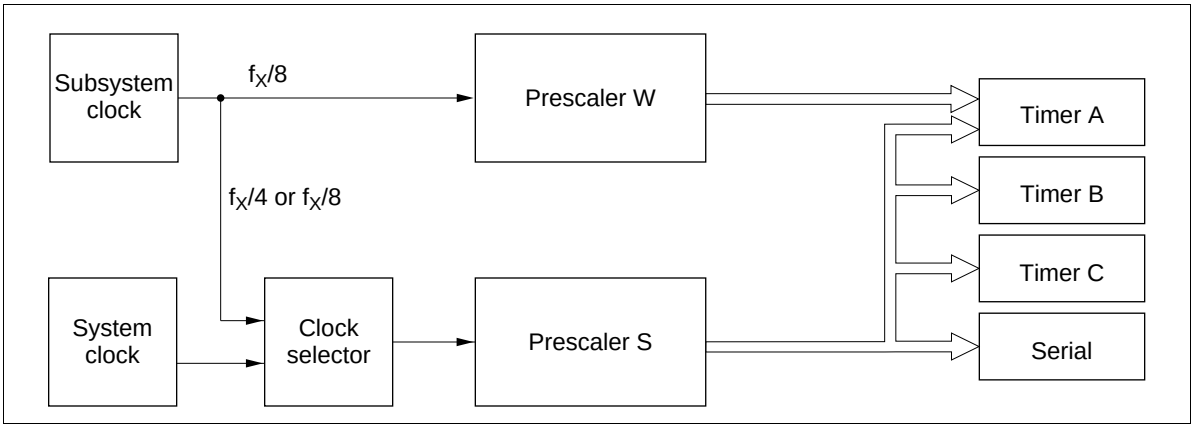



**Figure 26 Prescaler Output Supply**

## Timers

The MCU has three built-in timers A, B, and C. The functions of each timer are listed in table 7.

### Timer A

Timer A is an 8-bit free-running timer that can also be used as a clock time-base with a 32.768-kHz subsystem oscillator. Timer A has the following features:

- One of eight internal clocks can be selected from prescaler S according to the setting of timer mode register A (TMA: $008)
- In time-base mode, one of five internal clocks can be selected from prescaler W according to the setting of timer mode register A
- An interrupt request can be generated when timer counter A (TCA) overflows
- Input clock frequency must not be modified during timer A operation

**Table 7 Timer Functions**

| Functions | | Timer A | Timer B | Timer C |
|---|---|---|---|---|
| Clock source | Prescaler S | Available | Available | Available |
| | Prescaler W | Available | — | — |
| | External event | — | Available | — |
| Timer functions | Free-running | Available | Available | Available |
| | Time base | Available | — | — |
| | Event counter | — | Available | — |
| | Reload | — | Available | Available |
| | Watchdog | — | — | Available |
| | Input capture | — | Available | — |
| Timer output | PWM | — | — | Available |

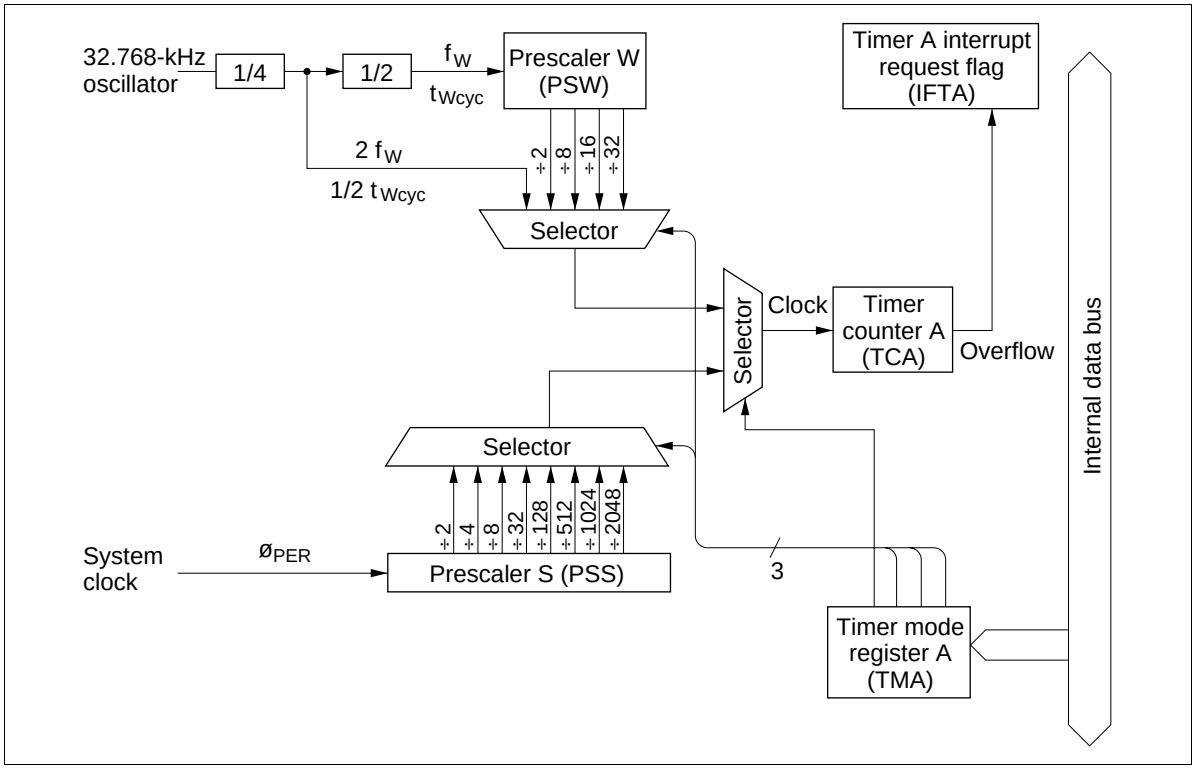



**Figure 27 Timer A Block Diagram**

**Timer mode register A (TMA: $008)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TMA3 | TMA2 | TMA1 | TMA0 |

| TMA3 | TMA2 | TMA1 | TMA0 | Source Prescaler | Input Clock Frequency | Operating Mode |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | PSS | $2048t_{cyc}$ | Timer A mode |
| | | | 1 | PSS | $1024t_{cyc}$ | |
| | | 1 | 0 | PSS | $512t_{cyc}$ | |
| | | | 1 | PSS | $128t_{cyc}$ | |
| | 1 | 0 | 0 | PSS | $32t_{cyc}$ | |
| | | | 1 | PSS | $8t_{cyc}$ | |
| | | 1 | 0 | PSS | $4t_{cyc}$ | |
| | | | 1 | PSS | $2t_{cyc}$ | |
| 1 | 0 | 0 | 0 | PSW | $32t_{Wcyc}$ | Time-base mode |
| | | | 1 | PSW | $16t_{Wcyc}$ | |
| | | 1 | 0 | PSW | $8t_{Wcyc}$ | |
| | | | 1 | PSW | $2t_{Wcyc}$ | |
| | 1 | 0 | 0 | PSW | $1/2t_{Wcyc}$ | |
| | | | 1 | Not used | | |
| | | 1 | X | PSW and TCA reset | | |

X = Don't care.

Notes: 1. $t_{Wcyc}$ = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. Timer counter overflow output period (seconds) = input clock period (seconds) × 256.
3. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

**Figure 28 Timer Mode Register A (TMA)**

**Timer B**

Timer B is an 8-bit multifunction timer that includes free-running, reload, and input capture timer features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter
- By setting timer mode register B2 (TMB2: $026), detection edge type of EVNB can be selected.
- By setting timer write register BL, U (TWBL, U: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation
- By setting timer read register BL, U (TRBL, U: $00A, $00B), the contents of timer counter B can be read out
- Timer B can be used as an input capture timer to count the clock cycles between trigger edges input as an external event
- An interrupt can be requested when timer counter B overflows or when a trigger input edge is received during input capture operation

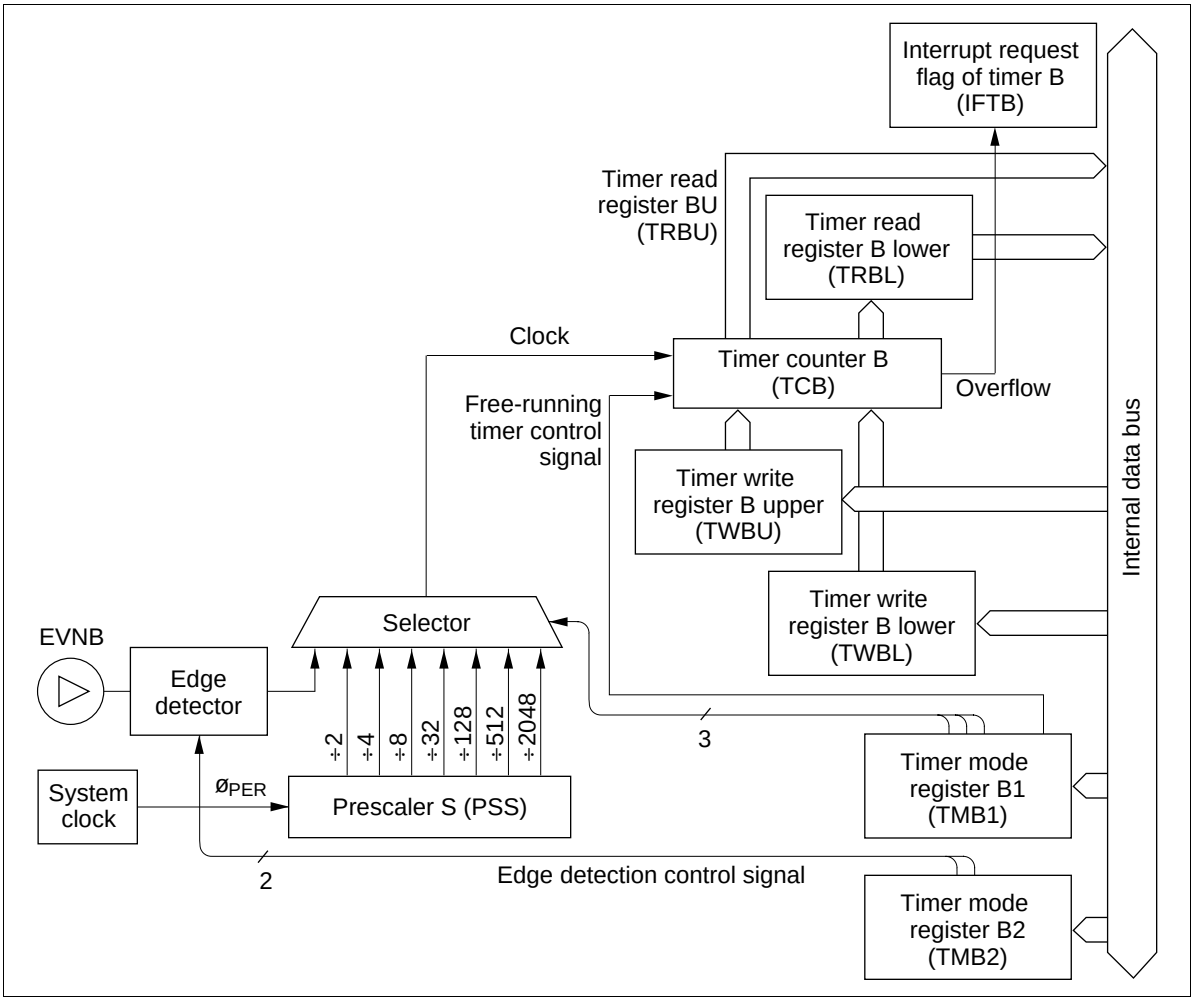



**Figure 29 Timer B Free-Running and Reload Operation Block Diagram**

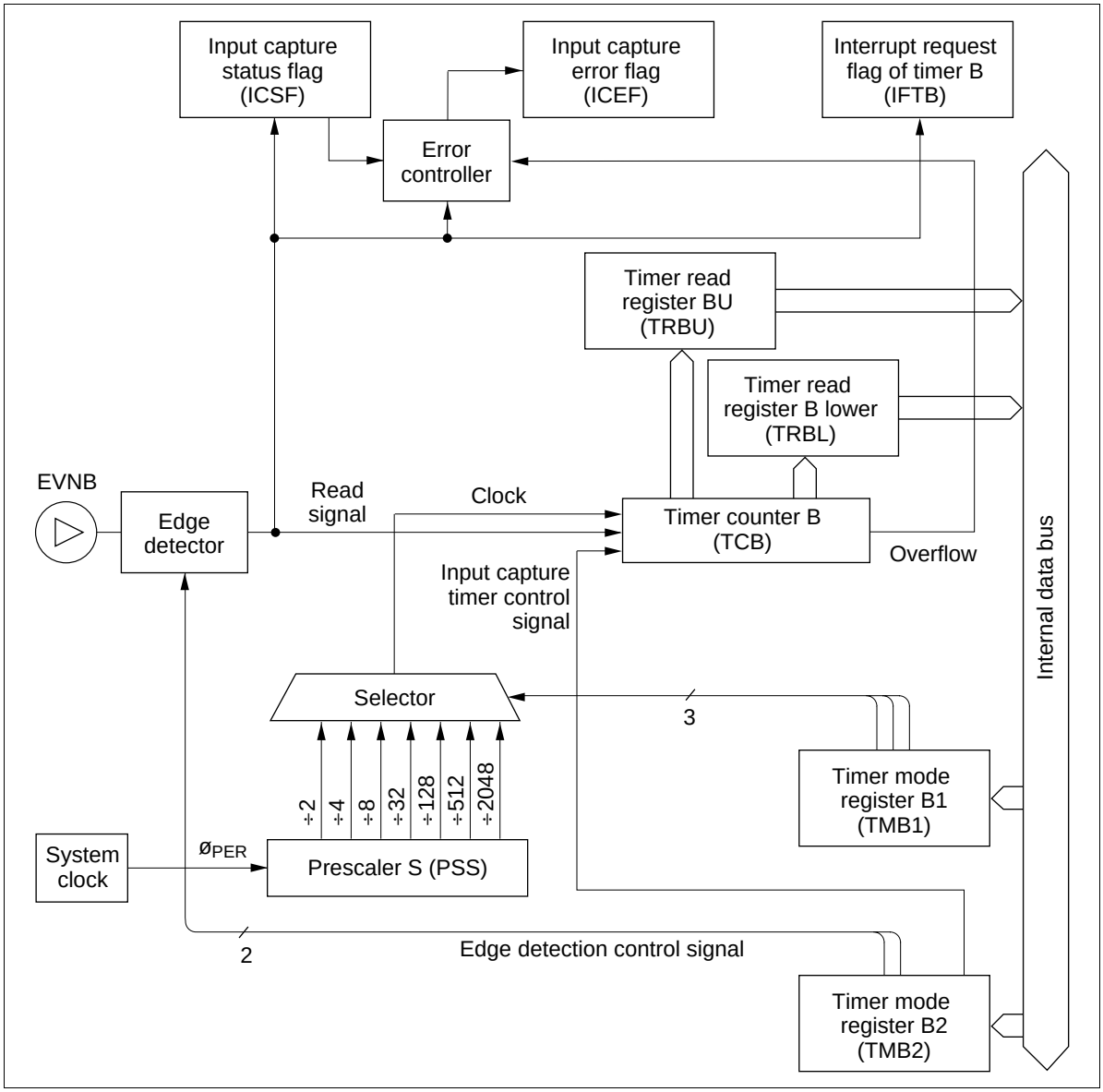



**Figure 30 Timer B Input Capture Operation Block Diagram**

**Timer mode register B1 (TMB1: $009)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TMB13 | TMB12 | TMB11 | TMB10 |

| TMB13 | Free-Running/Reload Timer Selection |
|---|---|
| 0 | Free-running timer |
| 1 | Reload timer |

| TMB12 | TMB11 | TMB10 | Input Clock Period and Input Clock Source |
|---|---|---|---|
| 0 | 0 | 0 | $2048t_{cyc}$ |
| | | 1 | $512t_{cyc}$ |
| | 1 | 0 | $128t_{cyc}$ |
| | | 1 | $32t_{cyc}$ |
| 1 | 0 | 0 | $8t_{cyc}$ |
| | | 1 | $4t_{cyc}$ |
| | 1 | 0 | $2t_{cyc}$ |
| | | 1 | $D_2$/EVNB (External event input) |

**Figure 31 Timer Mode Register B1 (TMB1)**

**Timer mode register B2 (TMB2: $026)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | — | 0 | 0 | 0 |
| Read/Write | — | W | W | W |
| Bit name | Not used | TMB22 | TMB21 | TMB20 |

| TMB21 | TMB20 | EVNB Edge Detection Selection |
|---|---|---|
| 0 | 0 | No detection |
| | 1 | Falling edge detection |
| 1 | 0 | Rising edge detection |
| | 1 | Rising and falling edge detection |

| TMB22 | Free-Running/Reload and Input Capture Selection |
|---|---|
| 0 | Free-Running/Reload |
| 1 | Input Capture |

**Figure 32 Timer Mode Register B2 (TMB2)**

**Timer C**

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled
- By setting timer write register CL, U (TWCL, U: $00E, $00F), timer counter C (TCC) can be written to
- By setting timer read register CL, U (TRCL, U: $00E, $00F), the contents of timer counter C can be read out
- An interrupt can be requested when timer counter C overflows
- Timer counter C can be used as a watchdog timer for detecting runaway programs

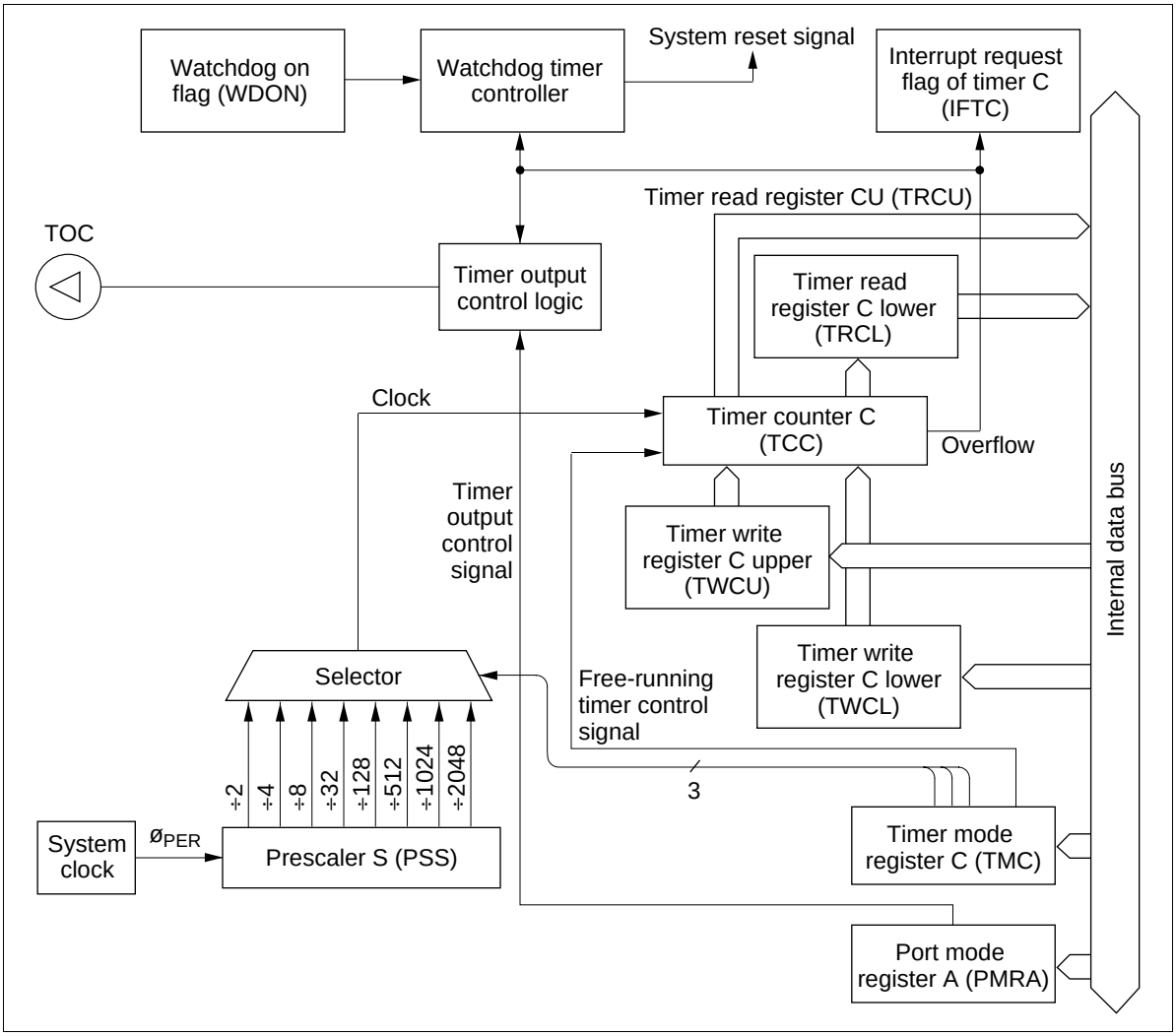



**Figure 33 Timer C Block Diagram**

**Timer mode register C (TMC: $00D)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TMC3 | TMC2 | TMC1 | TMC0 |

| TMC3 | Free-Running/Reload Timer Selection |
|---|---|
| 0 | Free-running timer |
| 1 | Reload timer |

| TMC2 | TMC1 | TMC0 | Input Clock Period |
|---|---|---|---|
| 0 | 0 | 0 | $2048t_{cyc}$ |
| | | 1 | $1024t_{cyc}$ |
| | 1 | 0 | $512t_{cyc}$ |
| | | 1 | $128t_{cyc}$ |
| 1 | 0 | 0 | $32t_{cyc}$ |
| | | 1 | $8t_{cyc}$ |
| | 1 | 0 | $4t_{cyc}$ |
| | | 1 | $2t_{cyc}$ |

**Figure 34 Timer Mode Register C (TMC)**

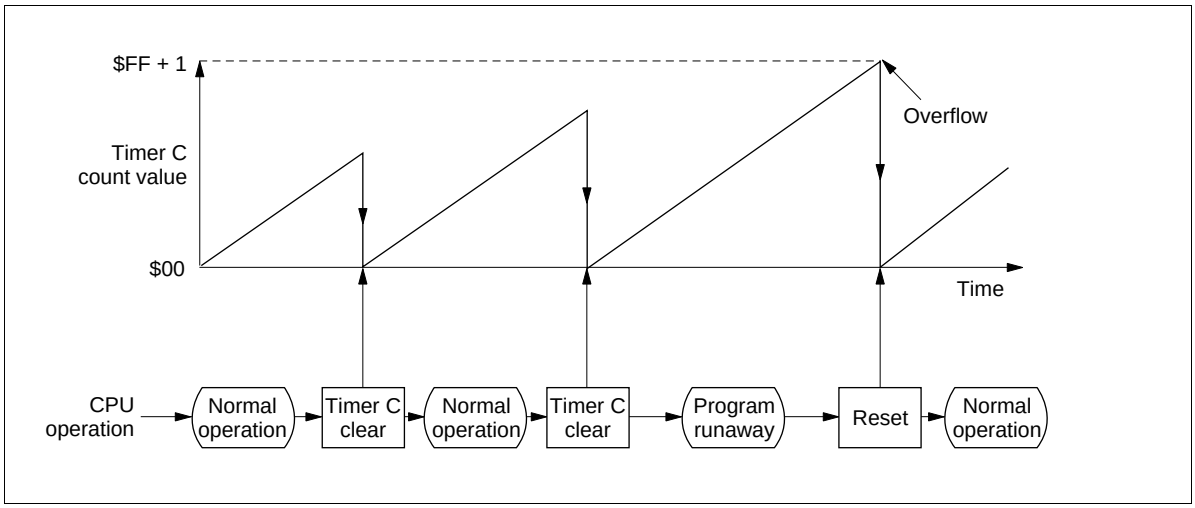
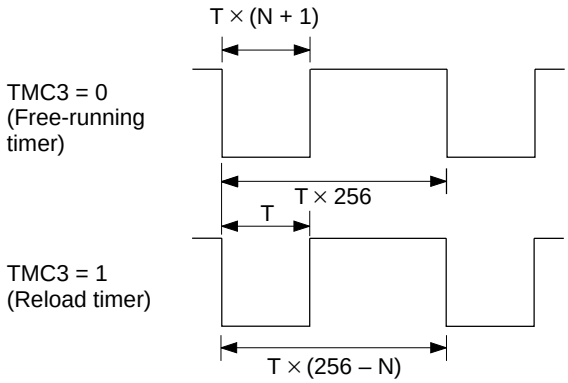



**Figure 35 Watchdog Timer Operation Flowchart**



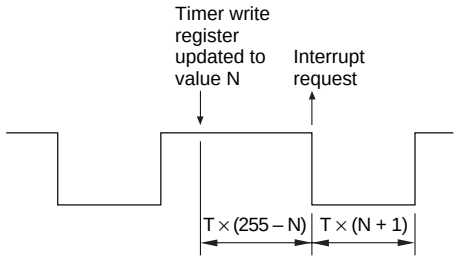
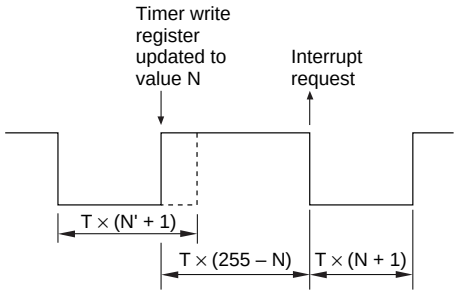
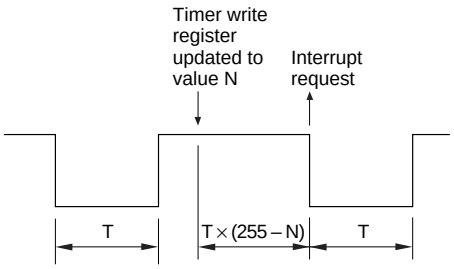
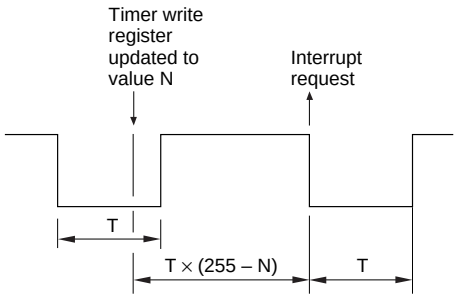

Notes: T: Input clock period supplied to counter.
(The clock source and system clock division ratio are determined by timer mode register C.)
N: Value of timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

**Figure 36 PWM Output Waveform**

**Notes on Use**

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 8. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

**Table 8 PWM Output Following Update of Timer Write Register**

| | PWM Output | |
|---|---|---|
| **Mode** | **Timer Write Register is Updated during High PWM Output** | **Timer Write Register is Updated during Low PWM Output** |
| Free running |  |  |
| Reload |  |  |

## Alarm Output Function

The MCU has an alarm output function built in. By setting port mode register C (PMRC: $025), one of four alarm frequencies supplied from the PSS can be selected.

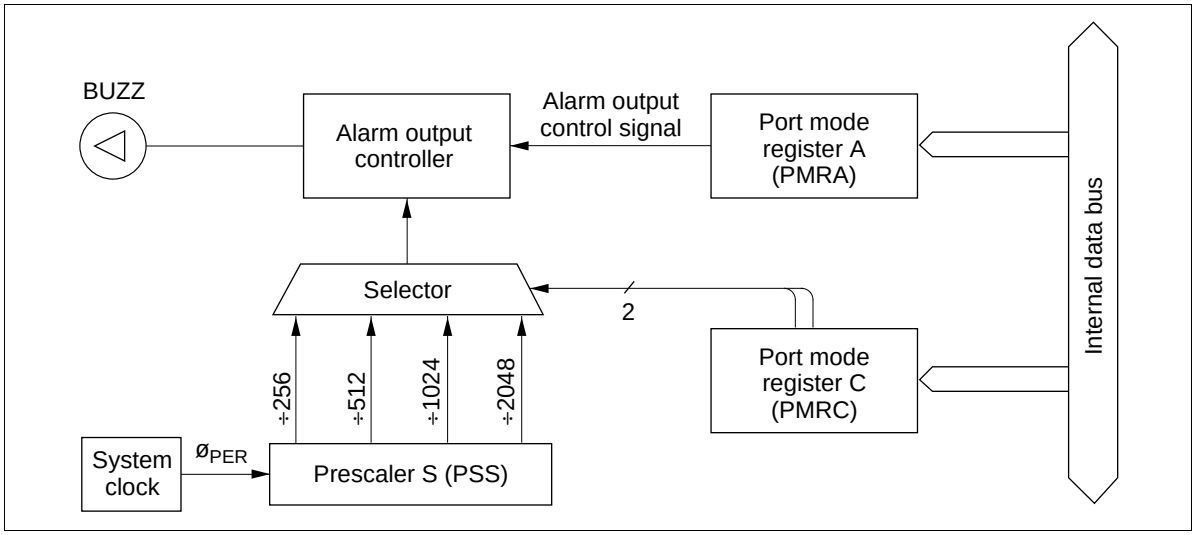



**Figure 37 Alarm Output Function Block Diagram**

**Table 9 Port Mode Register C**

| PMRC | | |
|---|---|---|
| **Bit 3** | **Bit 2** | **System Clock Divisor** |
| 0 | 0 | ÷ 2048 |
| | 1 | ÷ 1024 |
| 1 | 0 | ÷ 512 |
| | 1 | ÷ 256 |

## Serial Interface

The MCU has a one-channel serial interface built in with the following features.

- One of 13 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle status, the serial output pin can be controlled to be high or low output
- Transmit clock errors can be detected
- An interrupt request can be generated after transfer has completed when an error occurs

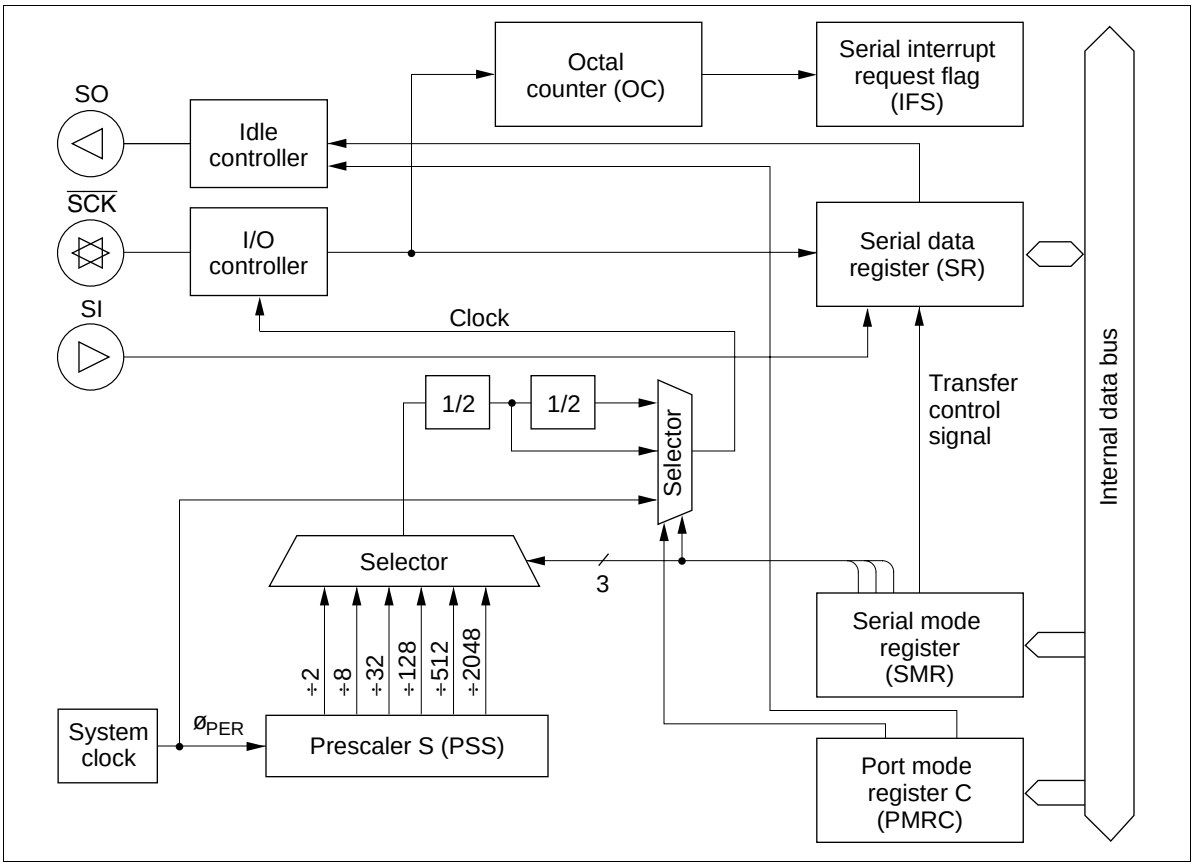



**Figure 38 Serial Interface Block Diagram**

**Table 10 Serial Interface Operating Modes**

| SMR | PMRA | | |
|---|---|---|---|
| **Bit 3** | **Bit 1** | **Bit 0** | **Operating Mode** |
| 1 | 0 | 0 | Continuous clock output mode |
| | | 1 | Transmit mode |
| | 1 | 0 | Receive mode |
| | | 1 | Transmit/receive mode |

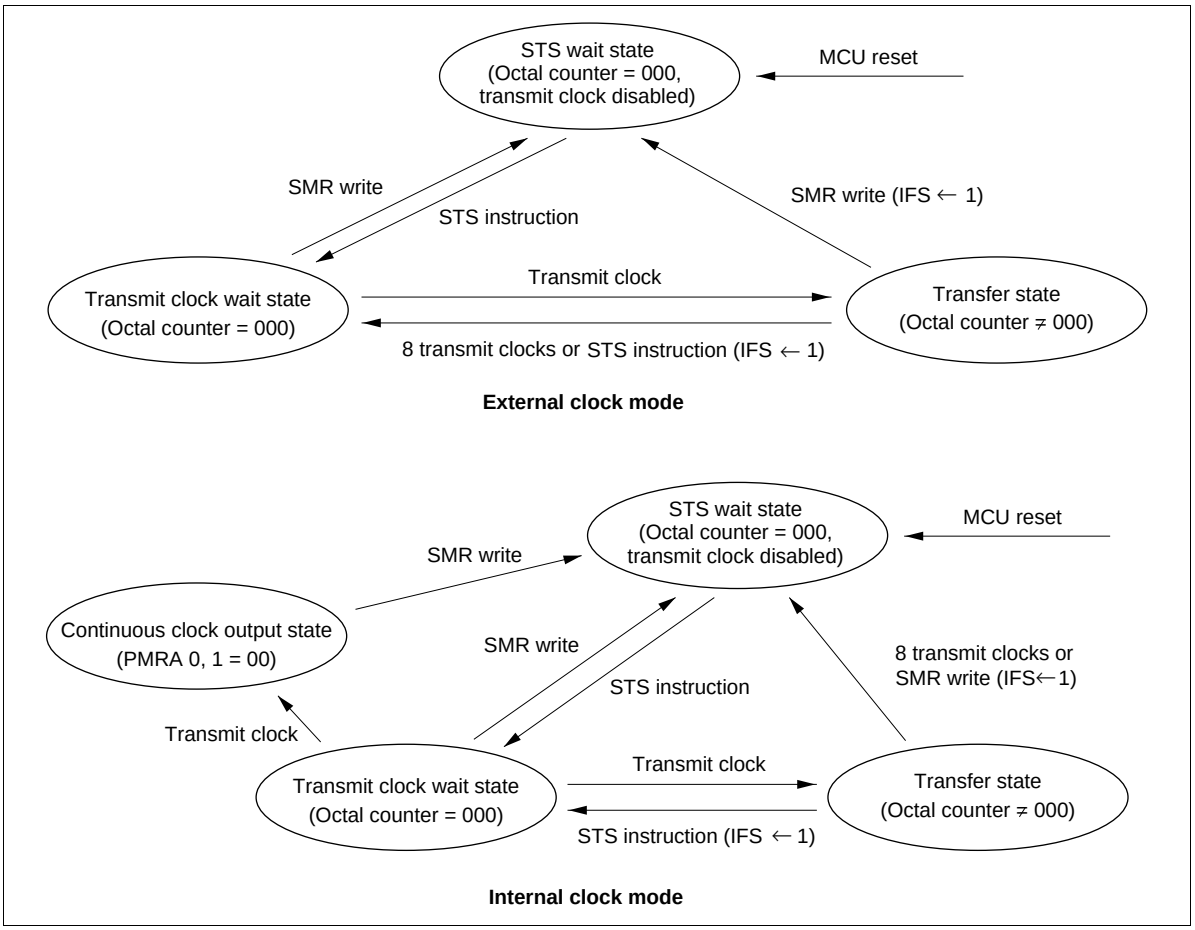



**Figure 39 Serial Interface State Transitions**

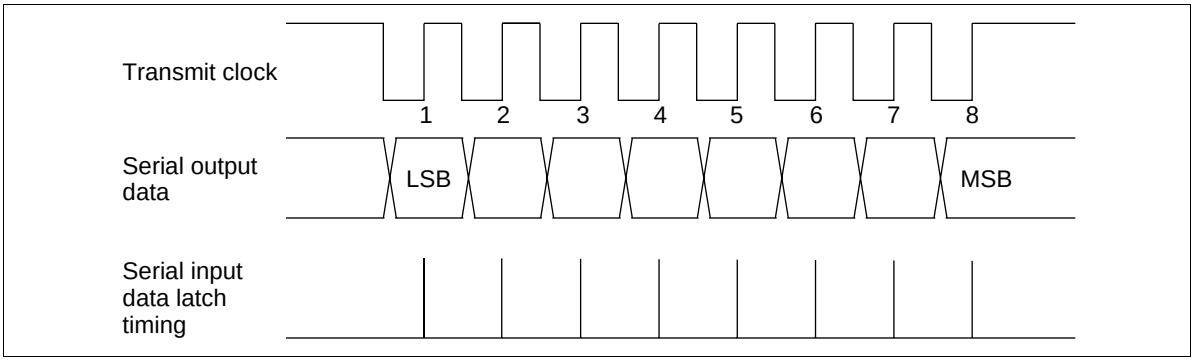



**Figure 40 Serial Interface Timing**

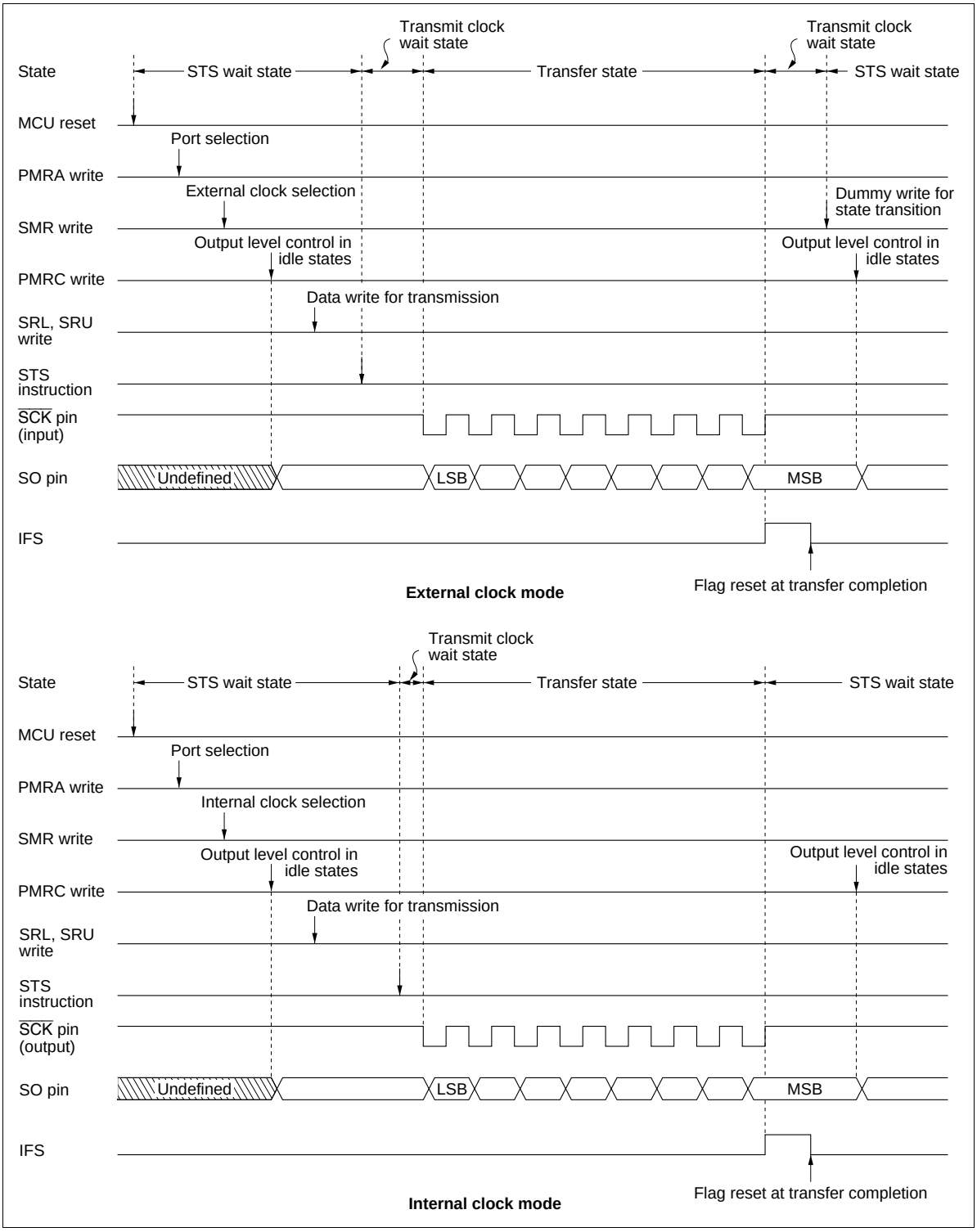
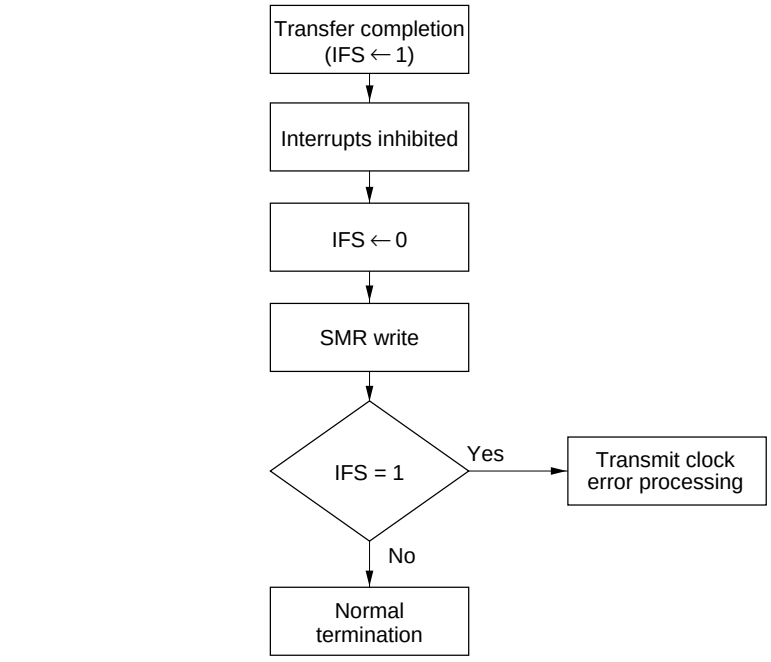
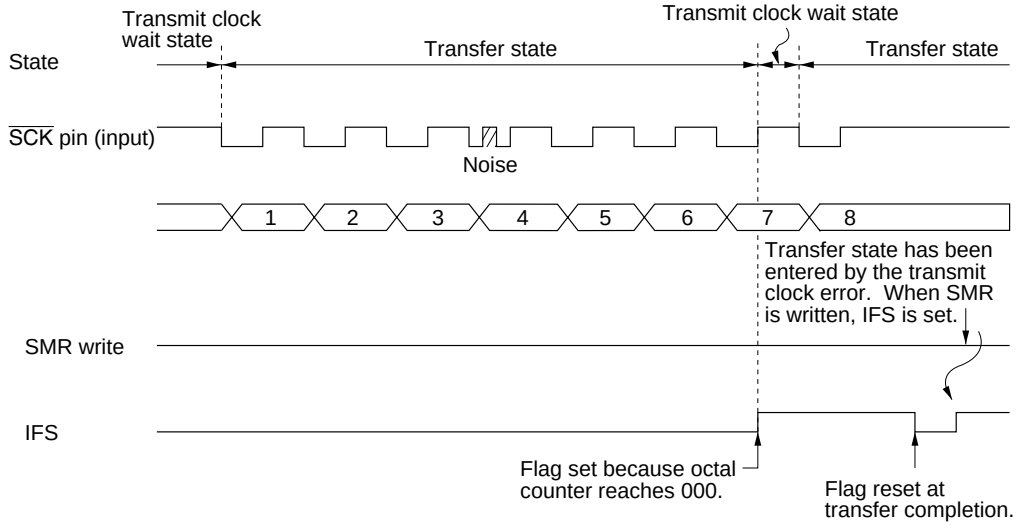



**Figure 41 Example of Serial Interface Operation Sequence**

Transmit clock errors are detected as illustrated in figure 42.




**Transmit clock error detection flowchart**




**Transmit clock error detection procedure**

**Figure 42 Transmit Clock Error Detection**

**Table 11 Transmit Clock Selection**

| PMRC | SMR | | | | |
|---|---|---|---|---|---|
| **Bit 0** | **Bit 2** | **Bit 1** | **Bit 0** | **System Clock Divisor** | **Transmit Clock Frequency** |
| 0 | 0 | 0 | 0 | ÷ 2048 | $4096t_{cyc}$ |
| | | | 1 | ÷ 512 | $1024t_{cyc}$ |
| | | 1 | 0 | ÷ 128 | $256t_{cyc}$ |
| | | | 1 | ÷ 32 | $64t_{cyc}$ |
| | 1 | 0 | 0 | ÷ 8 | $16t_{cyc}$ |
| | | | 1 | ÷ 2 | $4t_{cyc}$ |
| 1 | 0 | 0 | 0 | ÷ 4096 | $8192t_{cyc}$ |
| | | | 1 | ÷ 1024 | $2048t_{cyc}$ |
| | | 1 | 0 | ÷ 256 | $512t_{cyc}$ |
| | | | 1 | ÷ 64 | $128t_{cyc}$ |
| | 1 | 0 | 0 | ÷ 16 | $32t_{cyc}$ |
| | | | 1 | ÷ 4 | $8t_{cyc}$ |

**Serial mode register (SMR: $005)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | SMR3 | SMR2 | SMR1 | SMR0 |

| SMR3 | $R0_0/\overline{SCK}$ Mode Selection |
|---|---|
| 0 | $R0_0$ |
| 1 | $\overline{SCK}$ |

| SMR2 | SMR1 | SMR0 | $\overline{SCK}$ | Clock Source | Prescaler Division Ratio |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Output | Prescaler | Refer to table 11 |
| | | 1 | | | |
| | 1 | 0 | | | |
| | | 1 | | | |
| 1 | 0 | 0 | | | |
| | | 1 | | | |
| | 1 | 0 | Output | System clock | — |
| | | 1 | Input | External clock | — |

**Figure 43 Serial Mode Register (SMR)**

**Port mode register C (PMRC: $025)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | Undefined | 0 |
| Read/Write | W | W | W | W |
| Bit name | PMRC3 | PMRC2 | PMRC1 | PMRC0 |

Alarm output function.
Refer to table 9.

| PMRC0 | Serial Clock Division Ratio |
|---|---|
| 0 | Prescaler output divided by 2 |
| 1 | Prescaler output divided by 4 |

| PMRC1 | Output Level Control in Idle States |
|---|---|
| 0 | Low level |
| 1 | High level |

**Figure 44 Port Mode Register C (PMRC)**

## A/D Converter

The MCU also contains a built-in A/D converter that uses a sequential comparison method with a resistance ladder. It can perform digital conversion of twelve analog inputs with 8-bit resolution. The following describes the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed and to select digital or analog ports
- The A/D channel register (ACR: $016) is used to select an analog input channel
- A/D conversion is started by setting the A/D start flag (ADSF: $020, 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time the A/D start flag is cleared to 0.
- By setting the $I_{AD}$ off flag (IAOF: $021, 2) to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode
- The A/D data register is a read-only register consisting of a lower 4 bits and upper 4 bits (ADRL: $017, ADRU: $018). This register is not cleared by a reset. Data reads during A/D conversion are not guaranteed. After A/D conversion ends, the resultant 8-bit data is set in this register and held until the start of the next conversion (figures 51 to 53).

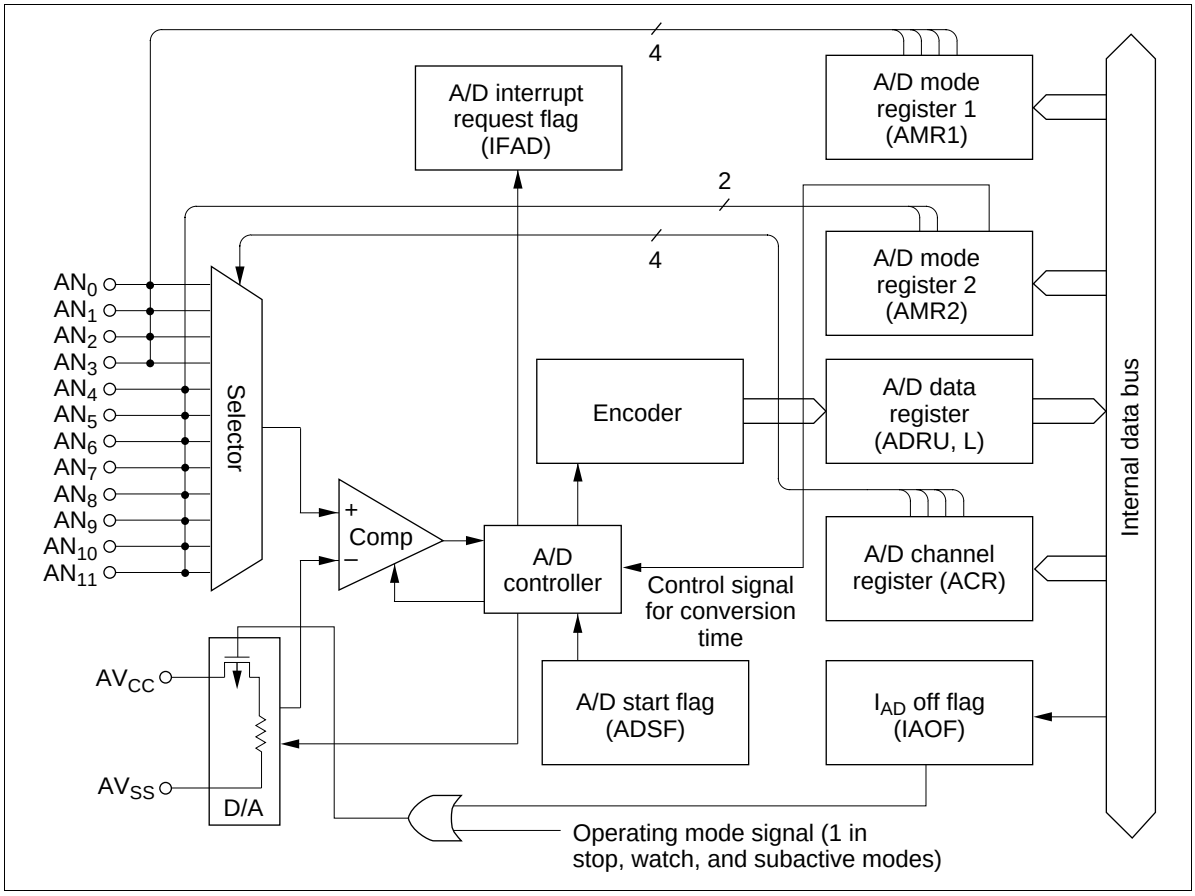



**Figure 45 A/D Converter Block Diagram**

**Notes on Usage**

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop, watch, or subactive mode. In addition, to save power while in these modes, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from $V_{CC}$, connect a 0.1-µF bypass capacitor between the $AV_{CC}$ and $AV_{SS}$ pins. (However, this is not necessary when the $AV_{CC}$ pin is directly connected to the $V_{CC}$ pin.)
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to $V_{CC}$. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode registr as an analog pin will remain pulled up.

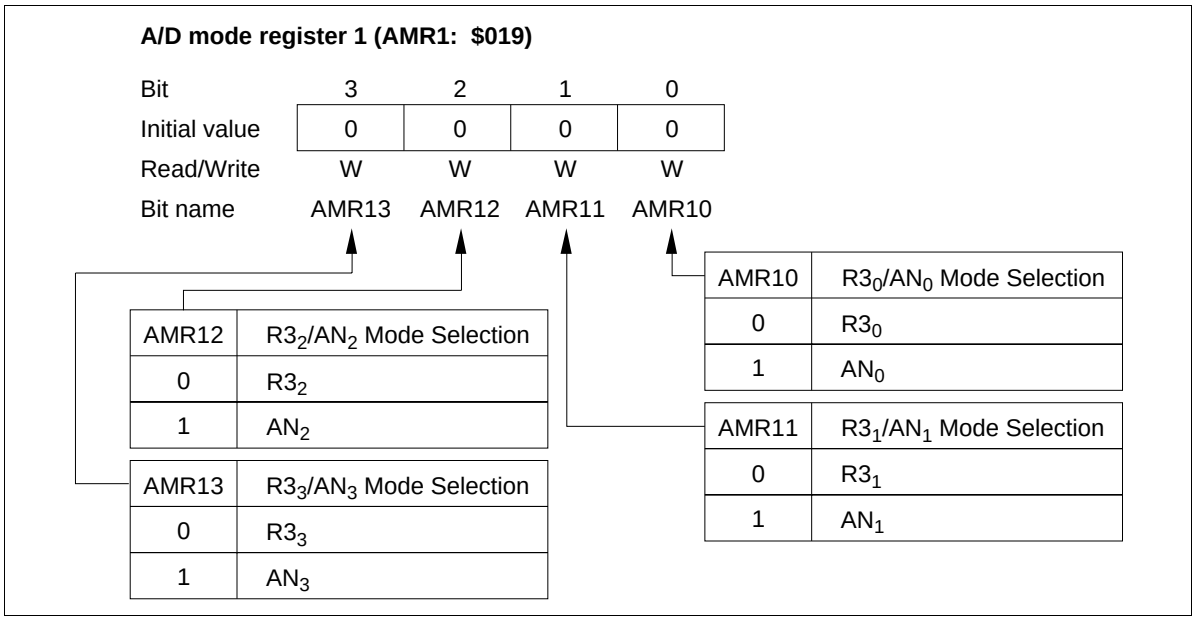



**Figure 46 A/D Mode Register 1 (AMR1)**

**A/D mode register 2 (AMR2: $01A)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | — | 0 | 0 | 0 |
| Read/Write | — | W | W | W |
| Bit name | Not used | AMR22 | AMR21 | AMR20 |

| AMR20 | Conversion Time |
|---|---|
| 0 | $34t_{cyc}$ |
| 1 | $67t_{cyc}$ |

| AMR22 | $R5/AN_8–AN_{11}$ Pin Selection |
|---|---|
| 0 | R5 |
| 1 | $AN_8–AN_{11}$ |

| AMR21 | $R4/AN_4–AN_7$ Pin Selection |
|---|---|
| 0 | R4 |
| 1 | $AN_4–AN_7$ |

**Figure 47 A/D Mode Register 2 (AMR2)**

**A/D channel register (ACR: $016)**

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | ACR3 | ACR2 | ACR1 | ACR0 |

| ACR3 | ACR2 | ACR1 | ACR0 | Analog Input Selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $AN_0$ |
| | | | 1 | $AN_1$ |
| | | 1 | 0 | $AN_2$ |
| | | | 1 | $AN_3$ |
| | 1 | 0 | 0 | $AN_4$ |
| | | | 1 | $AN_5$ |
| | | 1 | 0 | $AN_6$ |
| | | | 1 | $AN_7$ |
| 1 | 0 | 0 | 0 | $AN_8$ |
| | | | 1 | $AN_9$ |
| | | 1 | 0 | $AN_{10}$ |
| | | | 1 | $AN_{11}$ |
| | 1 | Don't care | Don't care | Not used |

**Figure 48 A/D Channel Register (ACR)**

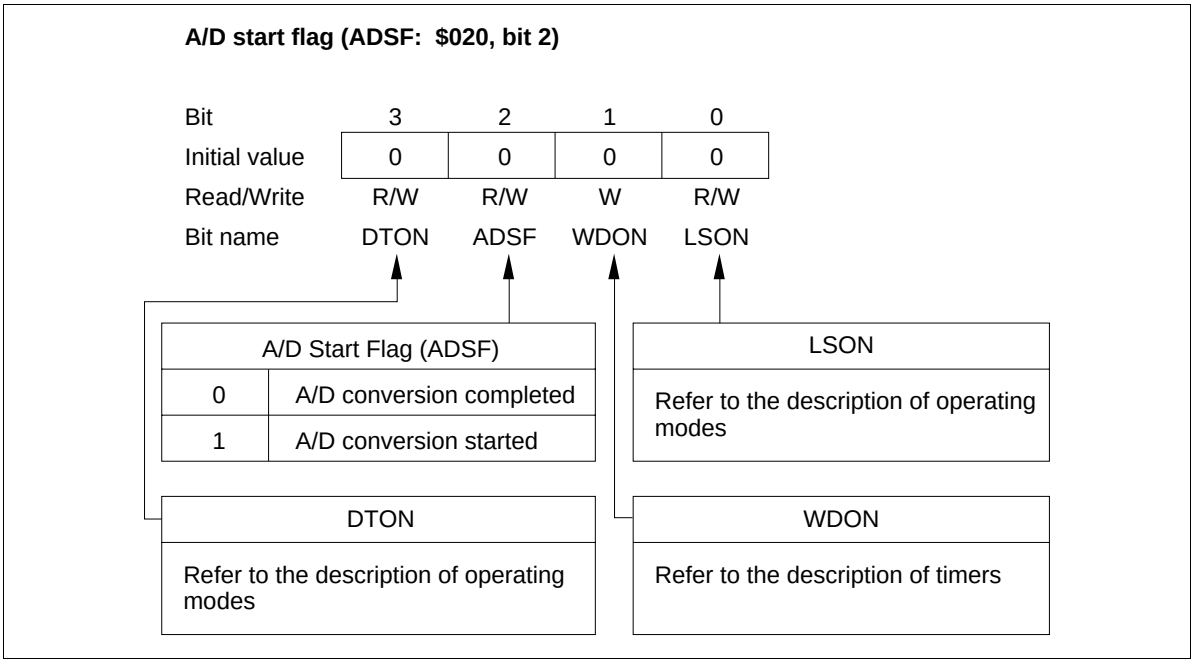



**Figure 49 A/D Start Flag (ADSF)**

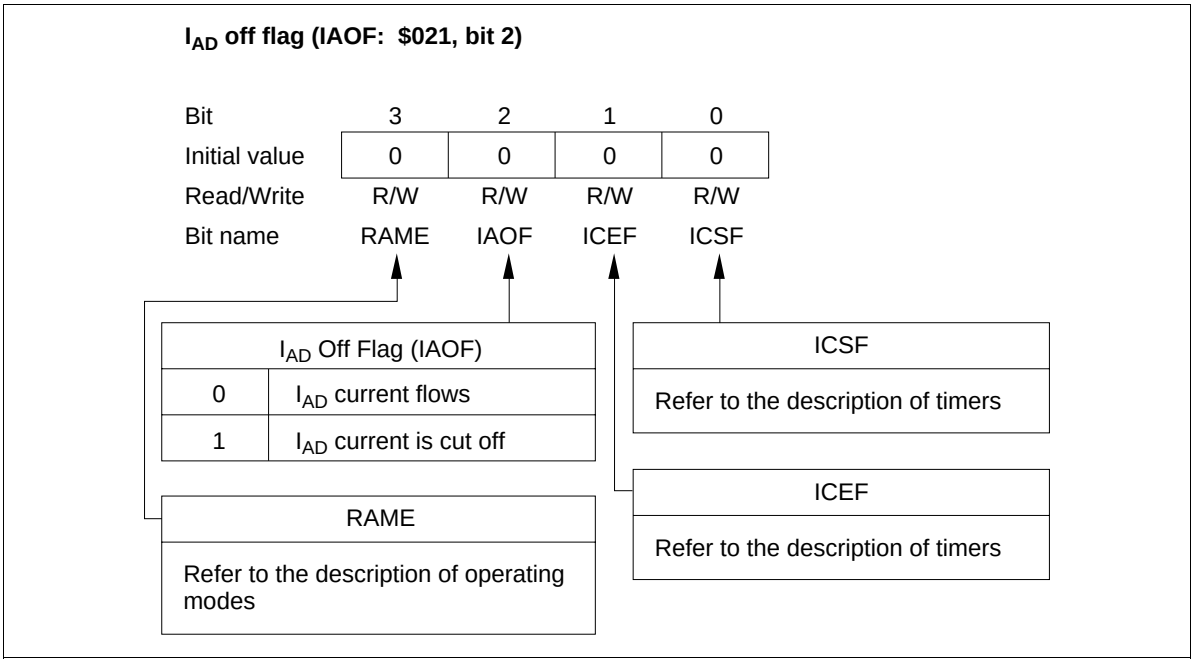



**Figure 50 $I_{AD}$ Off Flag (IAOF)**

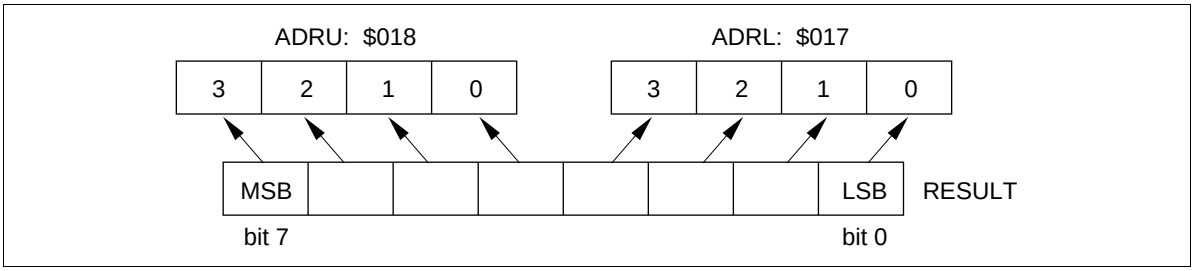



**Figure 51 A/D Data Register**

A/D data register (lower) (ADRL: $017)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/write | R | R | R | R |
| Initial value after reset | 0 | 0 | 0 | 0 |
| Bit name | ADRL3 | ADRL2 | ADRL1 | ADRL0 |

**Figure 52 A/D Data Register (Lower) (ADRL)**

A/D data register (upper) (ADRU: $018)

| Bit | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Read/write | R | R | R | R |
| Initial value after reset | 1 | 0 | 0 | 0 |
| Bit name | ADRU3 | ADRU2 | ADRU1 | ADRU0 |

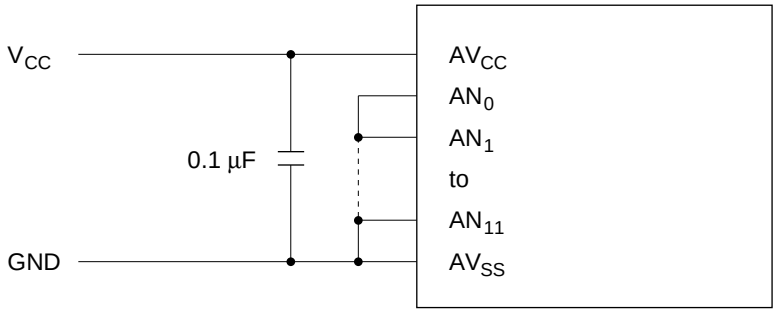
**Figure 53 A/D Data Register (Upper) (ADRU)**

## Notes on Mounting

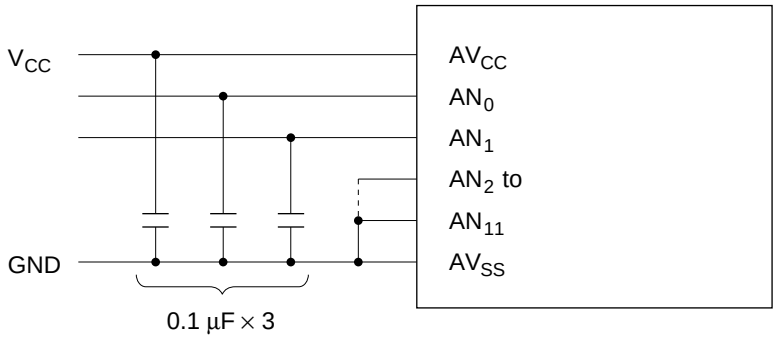
Assemble all parts including the HD404339 Series on a board, noting the points described below.

1. Connect layered ceramic type capacitors (about 0.1 μF) between $AV_{CC}$ and $AV_{SS}$, between $V_{CC}$ and GND, and between used analog pins and $AV_{SS}$.
2. Connect unused analog pins to $AV_{SS}$.

1. When not using an A/D converter.




2. When using pins $AN_0$ and $AN_1$ but not using $AN_2$ to $AN_{11}$.




3. When using all analog pins.

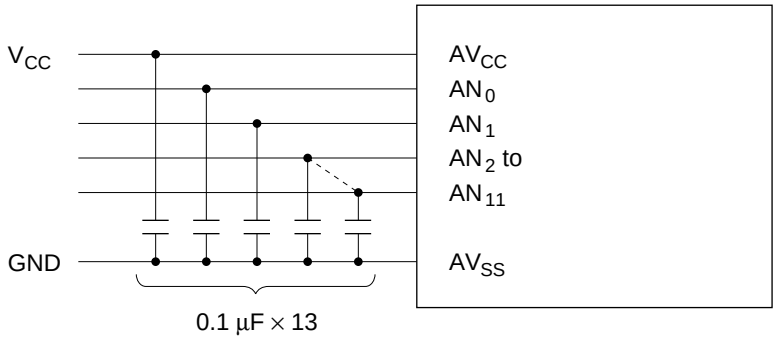



**Figure 54 Example of Connections ($AV_{CC}$ to $AV_{SS}$)**

Between the $V_{CC}$ and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 54.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance $C_1$ and a small capacitance $C_2$.

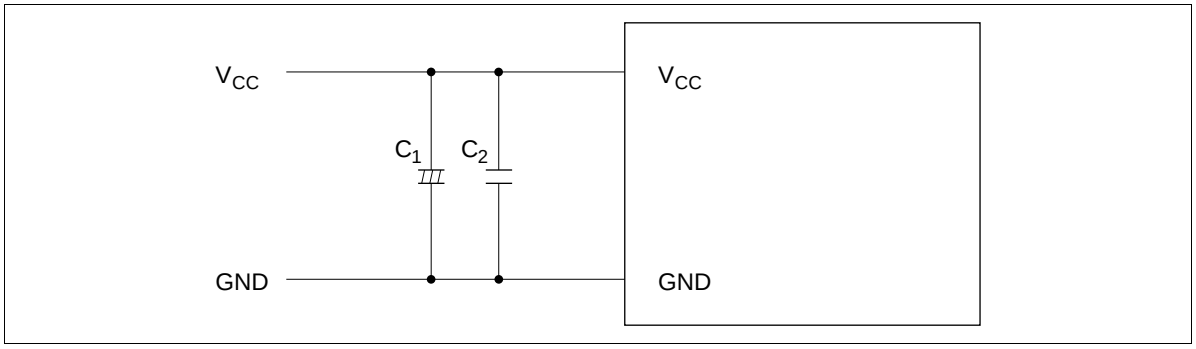



**Figure 55 Example of Connections ($V_{CC}$ to GND)**

## Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.3 to +7.0 | V | |
| Programming voltage | $V_{PP}$ | –0.3 to +14.0 | V | 1 |
| Pin voltage | $V_T$ | –0.3 to $V_{CC}$ + 0.3 | V | 2 |
| | | $V_{CC}$ – 45 to $V_{CC}$ + 0.3 | V | 3 |
| Total permissible input current | $\sum I_O$ | 70 | mA | 4 |
| Total permissible output current | $-\sum I_O$ | 150 | mA | 5 |
| Maximum input current | $I_O$ | 4 | mA | 6, 7 |
| | | 20 | mA | 6, 8 |
| Maximum output current | $-I_O$ | 4 | mA | 9, 10 |
| | | 30 | mA | 10, 11 |
| Operating temperature | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C | |

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST ($V_{PP}$) of HD4074339.
2. Applies to all standard voltage pins.
3. Applies to high-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from $V_{CC}$ to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports R3, R4, and R5.
8. Applies to ports R0, R6, and R7.
9. Applies to ports R0 and R3 to R7.
10. The maximum output current is the maximum current flowing from $V_{CC}$ to each I/O pin.
11. Applies to ports $D_0$–$D_{13}$, R1, R2, R8, and R9.

## Electrical Characteristics

**DC Characteristics ($V_{CC}$ = 4.0 to 5.5 V, GND = 0 V, $V_{disp}$ = $V_{CC}$ – 40 V to $V_{CC}$, $T_a$ = –20 to +75°C, unless otherwise specified)**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $\overline{RESET}$, $\overline{SCK}$, SI, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB | $0.8V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $\overline{RESET}$, $\overline{SCK}$, SI | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB | $V_{CC}$ – 40 | — | $0.2V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.5 | V | | |
| Output high voltage | $V_{OH}$ | $\overline{SCK}$, SO, TOC | $V_{CC}$ – 0.5 | — | — | V | $–I_{OH}$ = 0.5 mA | |
| Output low voltage | $V_{OL}$ | $\overline{SCK}$, SO, TOC | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| I/O leakage current | $\|I_{IL}\|$ | $\overline{RESET}$, $\overline{SCK}$, SI, SO,TOC, $OSC_1$ | — | — | 1 | µA | $V_{in}$ = 0 V to $V_{CC}$ | 1 |
| | | $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB | — | — | 20 | µA | $V_{in}$ = $V_{CC}$ – 40 to $V_{CC}$ | 1 |
| Current dissipation in active mode | $I_{CC}$ | $V_{CC}$ | — | — | 5.0 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 2, 5 |
| | | | — | — | 8.0 | mA | | 2, 6 |
| Current dissipation in standby mode | $I_{SBY}$ | $V_{CC}$ | — | — | 2.0 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 3 |
| Current dissipation in subactive mode | $I_{SUB}$ | $V_{CC}$ | — | — | 100 | µA | $V_{CC}$ = 5 V, 32 kHz oscillator | 4, 5 |
| | | | — | — | 320 | µA | | 4, 6 |
| Current dissipation in watch mode | $I_{WTC}$ | $V_{CC}$ | — | — | 20 | µA | $V_{CC}$ = 5 V, 32 kHz oscillator | 4 |
| Current dissipation in stop mode | $I_{STOP}$ | $V_{CC}$ | — | — | 10 | µA | X1 = GND, X2 = Open | 4, 5 |
| | | | — | — | 20 | µA | | 4, 6 |
| Stop mode retaining voltage | $V_{STOP}$ | $V_{CC}$ | 2 | — | — | V | | |

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2. $I_{CC}$ is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND
   R0, $R3_0$ to $R7_2$ at $V_{CC}$
   $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$ at $V_{disp}$

3. $I_{SBY}$ is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at $V_{CC}$
   TEST at GND
   R0, $R3_0$ to $R7_2$ at $V_{CC}$
   $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$ at $V_{disp}$

4. This is the source current when no I/O current is flowing.
   Test conditions: Pins: R0, $R3_0$ to $R7_2$ at $V_{CC}$
   $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$ at GND

5. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.

6. Applies to the HD4074339.

**I/O Characteristics for High-Voltage Pins ($V_{CC}$ = 4.0 to 5.5 V, GND = 0 V, $V_{disp}$ = $V_{CC}$ – 40 V to $V_{CC}$, $T_a$ = –20 to +75°C, unless otherwise specified)**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$ | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$ | $V_{CC}$ – 40 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_0$–$D_{13}$, R1, R2, R8, R9, BUZZ | $V_{CC}$ – 3.0 | — | — | V | $–I_{OH}$ = 15 mA | |
| | | | $V_{CC}$ – 2.0 | — | — | V | $–I_{OH}$ = 10 mA | |
| | | | $V_{CC}$ – 1.0 | — | — | V | $–I_{OH}$ = 4 mA | |
| Output low voltage | $V_{OL}$ | $D_0$–$D_{13}$, R1, R2, R8, R9, BUZZ | — | — | $V_{CC}$ – 37 | V | $V_{disp}$ = $V_{CC}$ – 40 V | 1 |
| | | | — | — | $V_{CC}$ – 37 | V | 150 kΩ at $V_{CC}$ – 40 V | 2 |
| I/O leakage current | $\|I_{IL}\|$ | $D_0$–$D_{13}$, R1, R2, R8, R9, $RA_1$, BUZZ | — | — | 20 | µA | $V_{in}$ = $V_{CC}$ – 40 V to $V_{CC}$ | 3 |
| Pull-down MOS current | $I_{PD}$ | $D_0$–$D_{13}$, R1, R2, R8, R9 | 200 | 600 | 1000 | µA | $V_{disp}$ = $V_{CC}$ – 35 V, $V_{in}$ = $V_{CC}$ | 1 |

Notes: 1. Applies to pins with pull-down MOS as selected by the mask option .
2. Applies to pins without pull-down MOS as selected by the mask option.
3. Excludes output buffer current.

**A/D Converter Characteristics ($V_{CC}$ = 4.0 to 5.5 V, GND = 0 V, $V_{disp}$ = $V_{CC}$ – 40 V to $V_{CC}$, $T_a$ = –20 to +75°C, unless otherwise specified)**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Analog supply voltage | $AV_{CC}$ | $AV_{CC}$ | $V_{CC}$ – 0.3 | $V_{CC}$ | $V_{CC}$ + 0.3 | V | | 1 |
| Analog input voltage | $AV_{in}$ | $AN_0$–$AN_{11}$ | $AV_{SS}$ | — | $AV_{CC}$ | V | | |
| Current flowing between $AV_{CC}$ and $AV_{SS}$ | $I_{AD}$ | | — | — | 200 | µA | $V_{CC}$ = $AV_{CC}$ = 5.0 V | |
| Analog input capacitance | $CA_{in}$ | $AN_0$–$AN_{11}$ | — | — | 30 | pF | | |
| Resolution | | | 8 | 8 | 8 | Bit | | |
| Number of input channels | | | 0 | — | 12 | Channel | | |
| Absolute accuracy | | | — | — | ±2.0 | LSB | | |
| Conversion time | | | 34 | — | 67 | $t_{cyc}$ | | |
| Input impedance | | $AN_0$–$AN_{11}$ | 1 | — | — | MΩ | | |

Note: 1. Connect this to $V_{CC}$ if the A/D converter is not used.

**AC Characteristics ($V_{CC}$ = 4.0 to 5.5 V, GND = 0 V, $V_{disp}$ = $V_{CC}$ – 40 V to $V_{CC}$, $T_a$ = –20 to +75°C)**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Clock oscillation frequency | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 0.4 | 4 | 4.5 | MHz | System clock divided by 4 | 1 |
| | | X1, X2 | — | 32.768 | — | kHz | | |
| Instruction cycle time | $t_{cyc}$ | | 0.89 | 1 | 10 | µs | | 1 |
| | $t_{subcyc}$ | | — | 244.14 | — | µs | 32-kHz oscillator, 1/8 system clock division ratio | |
| | | | — | 122.07 | — | µs | 32-kHz oscillator, 1/4 system clock division ratio | |
| Oscillation stabilization time (ceramic oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 7.5 | ms | | 2 |
| Oscillation stabilization time (crystal oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 40 | ms | | 2 |
| | | X1, X2 | — | — | 2 | s | | 2 |
| External clock high width | $t_{CPH}$ | $OSC_1$ | 92 | — | — | ns | | 3 |
| External clock low width | $t_{CPL}$ | $OSC_1$ | 92 | — | — | ns | | 3 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | | 3 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | | 3 |
| $\overline{INT_0}$, $\overline{INT_1}$, EVNB high widths | $t_{IH}$ | $\overline{INT_0}$, $\overline{INT_1}$, EVNB | 2 | — | — | $t_{cyc}$/ $t_{subcyc}$ | | 4 |
| $\overline{INT_0}$, $\overline{INT_1}$, EVNB low widths | $t_{IL}$ | $\overline{INT_0}$, $\overline{INT_1}$, EVNB | 2 | — | — | $t_{cyc}$/ $t_{subcyc}$ | | 4 |
| $\overline{RESET}$ low width | $t_{RSTL}$ | $\overline{RESET}$ | 2 | — | — | $t_{cyc}$ | | 5 |
| $\overline{STOPC}$ low width | $t_{STPL}$ | $\overline{STOPC}$ | 1 | — | — | $t_{RC}$ | | 6 |
| $\overline{RESET}$ rise time | $t_{RSTr}$ | $\overline{RESET}$ | — | — | 20 | ms | | 5 |
| $\overline{STOPC}$ rise time | $t_{STPr}$ | $\overline{STOPC}$ | — | — | 20 | ms | | 6 |
| Input capacitance | $C_{in}$ | All input pins except TEST | — | — | 30 | pF | f = 1 MHz, $V_{in}$ = 0 V | |
| | | TEST | — | — | 30 | pF | f = 1 MHz, $V_{in}$ = 0 V | 7 |
| | | | — | — | 180 | pF | | 8 |

Notes: 1. When using the subsystem oscillator (32.768 kHz), one of the following relationships for $f_{OSC}$ must be applied.

0.4 MHz ≤ $f_{OSC}$ ≤ 1.0 MHz or 1.6 MHz ≤ $f_{OSC}$ ≤ 4.5 MHz

The operating range for $f_{OSC}$ can be set with bit 1 of system selection register 1 (SSR1: $027).

2. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After $V_{CC}$ reaches 4.0 V at power-on.
b. After $\overline{RESET}$ input goes low when stop mode is cancelled.
c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of $t_{RC}$.

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

3. Refer to figure 56.
4. Refer to figure 57.
5. Refer to figure 58.
6. Refer to figure 59.
7. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
8. Applies to the HD4074339.

**Serial Interface Timing Characteristics ($V_{CC}$ = 4.0 to 5.5 V, GND = 0 V, $V_{disp}$ = $V_{CC}$ – 40 V to $V_{CC}$, $T_a$ = –20 to +75°C, unless otherwise specified)**

**During Transmit Clock Output**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | Load shown in figure 61 | 1 |
| Transmit clock high width | $t_{SCKH}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | Load shown in figure 61 | 1 |
| Transmit clock low width | $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | Load shown in figure 61 | 1 |
| Transmit clock rise time | $t_{SCKr}$ | $\overline{SCK}$ | — | — | 80 | ns | Load shown in figure 61 | 1 |
| Transmit clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 80 | ns | Load shown in figure 61 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | Load shown in figure 61 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 100 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 200 | — | — | ns | | 1 |

**During Transmit Clock Input**

| Item | Symbol | Pins | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | | 1 |
| Transmit clock high width | $t_{SCKH}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock low width | $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock rise time | $t_{SCKr}$ | $\overline{SCK}$ | — | — | 80 | ns | | 1 |
| Transmit clock fall time | $t_{SCKf}$ | $\overline{SCK}$ | — | — | 80 | ns | | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 300 | ns | Load shown in figure 61 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 100 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 200 | — | — | ns | | 1 |

Note: 1. Refer to figure 60.

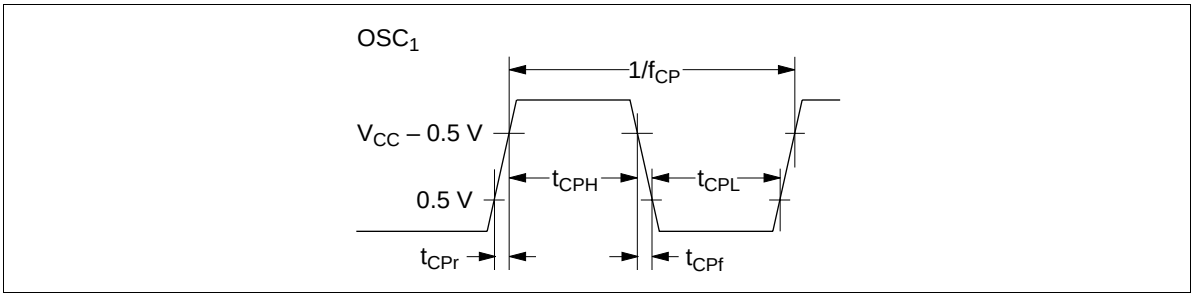



**Figure 56 External Clock Timing**

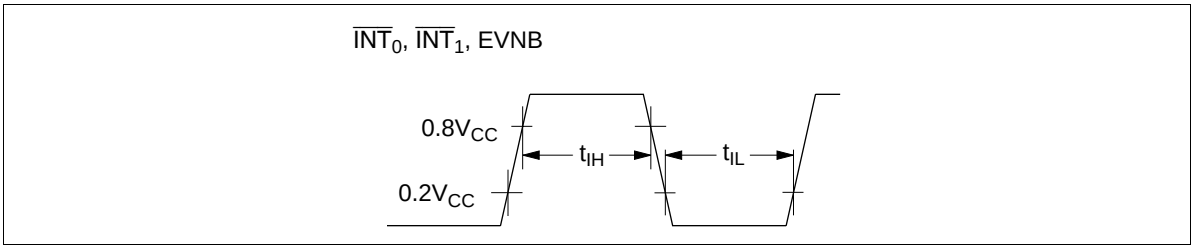



**Figure 57 Interrupt Timing**

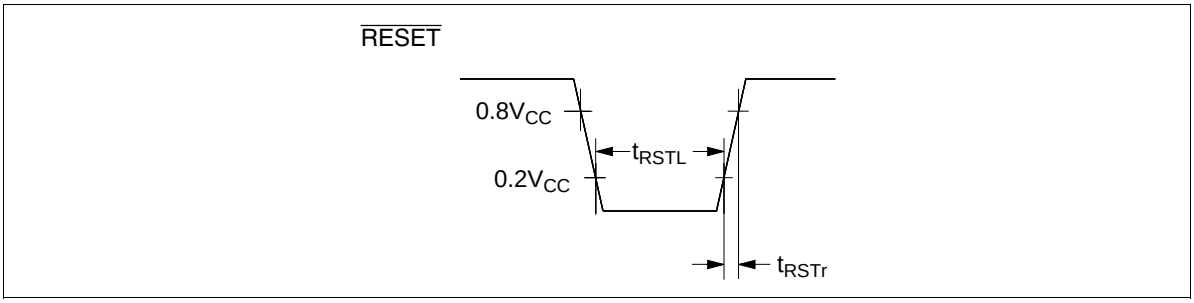



**Figure 58 $\overline{\text{RESET}}$ Timing**

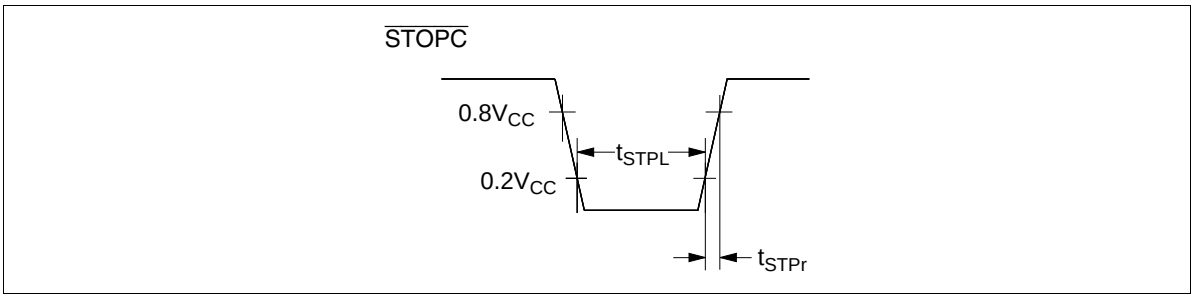
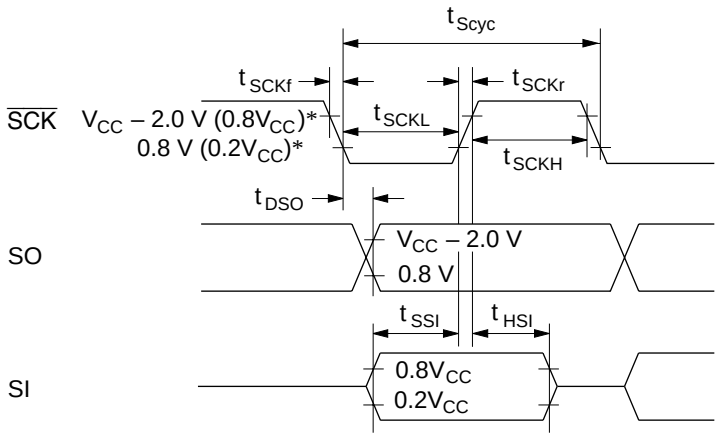



**Figure 59 $\overline{\text{STOPC}}$ Timing**




Note: * $V_{CC}$ – 2.0 V and 0.8 V are the threshold voltages for transmit clock output, and $0.8V_{CC}$ and $0.2V_{CC}$ are the threshold voltages for transmit clock input.

**Figure 60 Serial Interface Timing**

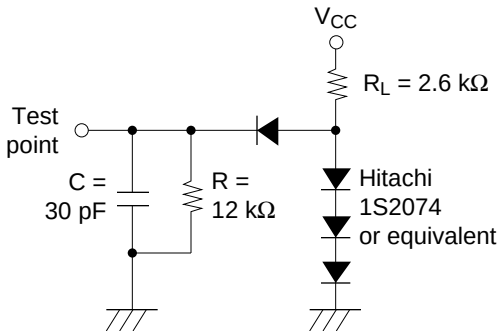



**Figure 61 Timing Load Circuit**

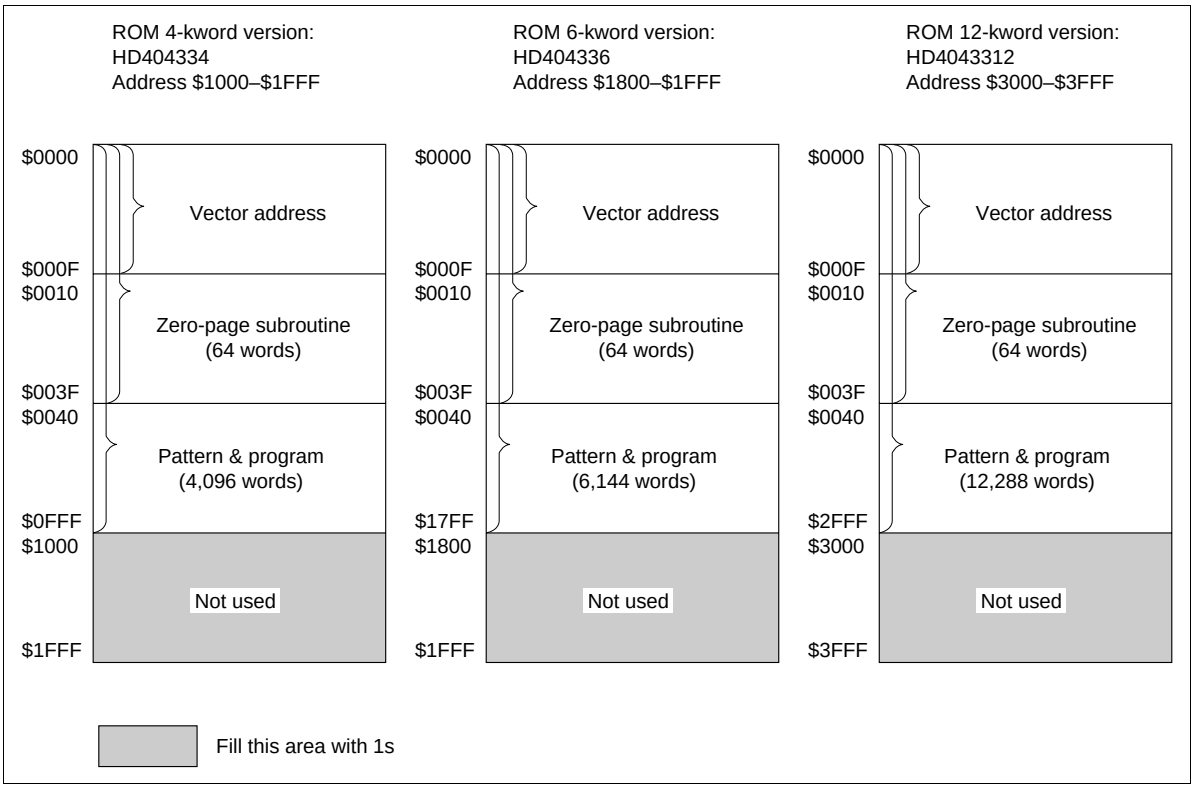
## Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404334 and HD404336 as an 8-kword version (HD404338), and to create the same data size for the HD4043312 as a 16-kword version (HD404339).

The 8-kword and 16-kword data sizes are required to change ROM data to mask manufacturing data since the program used is for an 8-k or 16-kword version.

This limitation applies when using an EPROM or a data base.



## HD404334/HD404336/HD404338/HD4043312/HD404339 Option List

Please check off the appropriate applications and enter the necessary information.

| | |
|---|---|
| Date of order | |
| Customer | |
| Department | |
| Name | |
| ROM code name | |
| LSI number | |

1. ROM Size

| | |
|---|---|
| ☐ HD404334 | 4-kword |
| ☐ HD404336 | 6-kword |
| ☐ HD404338 | 8-kword |
| ☐ HD4043312 | 12-kword |
| ☐ HD404339 | 16-kword |

2. Optional Functions

| |
|---|
| *☐ With 32-kHz CPU operation, with time base for clock |
| *☐ Without 32-kHz CPU operation, with time base for clock |
| ☐ Without 32-kHz CPU operation, without time base |

Note: *Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. I/O Options

D: Without pull-down resistance E: With pull-down resistance

| Pin name | I/O | I/O option | |
|---|---|---|---|
| | | D | E |
| D0/$\overline{INT_0}$ | I/O | | |
| D1/$\overline{INT_1}$ | I/O | | |
| D2/EVNB | I/O | | |
| D3/BUZZ | I/O | | |
| D4/$\overline{STOPC}$ | I/O | | |
| D5 | I/O | | |
| D6 | I/O | | |
| D7 | I/O | | |
| D8 | I/O | | |
| D9 | I/O | | |
| D10 | I/O | | |
| D11 | I/O | | |
| D12 | I/O | | |
| D13 | I/O | | |

| Pin name | | I/O | I/O option | |
|---|---|---|---|---|
| | | | D | E |
| R1 | R10 | I/O | | |
| | R11 | I/O | | |
| | R12 | I/O | | |
| | R13 | I/O | | |
| R2 | R20 | I/O | | |
| | R21 | I/O | | |
| | R22 | I/O | | |
| | R23 | I/O | | |
| R8 | R80 | I/O | | |
| | R81 | I/O | | |
| | R82 | I/O | | |
| | R83 | I/O | | |
| R9 | R90 | I/O | | |
| | R91 | I/O | | |
| | R92 | I/O | | |
| | R93 | I/O | | |

4. RA1/Vdisp

| |
|---|
| ☐ RA1 without pull-down resistance |
| ☐ Vdisp |

Note: If even only one pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

5. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

| |
|---|
| ☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| ☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS. |

6. System Oscillator (OSC1, OSC2)

| | | |
|---|---|---|
| ☐ Ceramic oscillator | f = | MHz |
| ☐ Crystal oscillator | f = | MHz |
| ☐ External clock | f = | MHz |

7. Stop Mode

| |
|---|
| ☐ Used |
| ☐ Not used |

8. Package

| |
|---|
| ☐ FP-64B |
| ☐ DP-64S |

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

**Hitachi, Ltd.**
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

**For further information write to:**

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright © Hitachi, Ltd., 1998. All rights reserved. Printed in Japan.