

- 2-V to 5.5-V V_{CC} Operation
- Supports Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

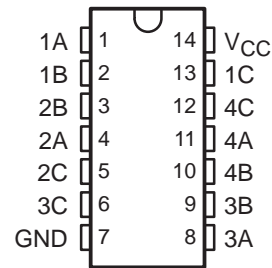
This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V V_{CC} operation.

This switch is designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

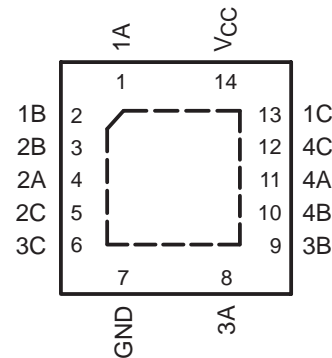
Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

**D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)**



**RGY PACKAGE
(TOP VIEW)**



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC4066N	SN74AHC4066N
	QFN – RGY	Tape and reel	SN74AHC4066RGYR	HA4066
	SOIC – D	Tube	SN74AHC4066D	AHC4066
		Tape and reel	SN74AHC4066DR	
	SOP – NS	Tube	SN74AHC4066NS	AHC4066
		Tape and reel	SN74AHC4066NSR	
	SSOP – DB	Tube	SN74AHC4066DB	HA4066
		Tape and reel	SN74AHC4066DBR	
	TSSOP – PW	Tube	SN74AHC4066PW	HA4066
		Tape and reel	SN74AHC4066PWR	
	TVSOP – DGV	Tape and reel	SN74AHC4066DGV	HA4066

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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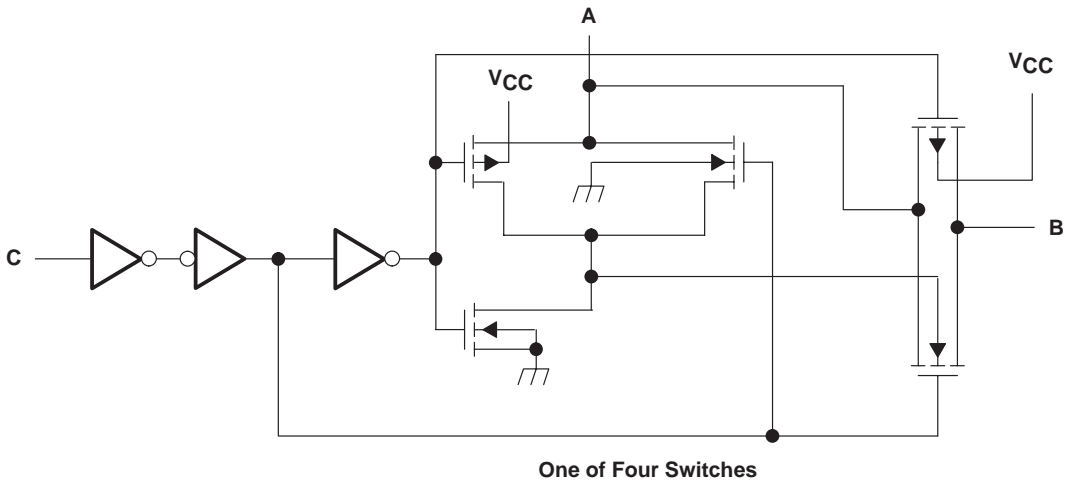
SN74AHC4066
QUADRUPLE BILATERAL ANALOG SWITCH

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FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Control-input clamp current, I_{IK} ($V_I < 0$)	-20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	± 50 mA
On-state switch current, I_T ($V_{IO} = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): N package	80°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 5.5 V maximum.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2†	5.5	V
V _{IH}	High-level input voltage, control inputs	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage, control inputs	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Control input voltage	0	5.5	V
V _{IO}	Input/output voltage	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	
T _A	Operating free-air temperature	–40	85	°C

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AHC4066

QUADRUPLE BILATERAL ANALOG SWITCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
r _{on} On-state switch resistance	I _T = -1 mA, V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1)	2.3 V		38	180		225	Ω
		3 V		29	150		190	
		4.5 V		21	75		100	
r _{on(p)} Peak on-state resistance	I _T = -1 mA, V _I = V _{CC} to GND, V _C = V _{IH}	2.3 V		143	500		600	Ω
		3 V		57	180		225	
		4.5 V		31	100		125	
Δr _{on} Difference in on-state resistance between switches	I _T = -1 mA, V _I = V _{CC} to GND, V _C = V _{IH}	2.3 V		6	30		40	Ω
		3 V		3	20		30	
		4.5 V		2	15		20	
I _I Control input current	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1	μA
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 2)	5.5 V			±0.1		±1	μA
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 3)	5.5 V			±0.1		±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V					20	μA
C _{ic} Control input capacitance				1.5				pF
C _{io} Switch input/output capacitance				5.5				pF
C _F Feed-through capacitance				0.5				pF

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH} t _{PHL} Propagation delay time	A or B	B or A	C _L = 15 pF, (see Figure 4)		1.2	10		16	ns
t _{PZH} t _{PZL} Switch turn-on time	C	A or B	C _L = 15 pF, R _L = 1 k Ω (see Figure 5)		3.3	15		20	ns
t _{PLZ} t _{PHZ} Switch turn-off time	C	A or B	C _L = 15 pF, R _L = 1 k Ω (see Figure 5)		6	15		23	ns
t _{PLH} t _{PHL} Propagation delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)		2.6	12		18	ns
t _{PZH} t _{PZL} Switch turn-on time	C	A or B	C _L = 50 pF, R _L = 1 k Ω (see Figure 5)		4.2	25		32	ns
t _{PLZ} t _{PHZ} Switch turn-off time	C	A or B	C _L = 50 pF, R _L = 1 k Ω (see Figure 5)		9.6	25		32	ns

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH} t _{PHL} Propagation delay time	A or B	B or A	C _L = 15 pF, (see Figure 4)		0.8	6		10	ns
t _{PZH} t _{PZL} Switch turn-on time	C	A or B	C _L = 15 pF, R _L = 1 k Ω (see Figure 5)		2.3	11		15	ns
t _{PLZ} t _{PHZ} Switch turn-off time	C	A or B	C _L = 15 pF, R _L = 1 k Ω (see Figure 5)		4.5	11		15	ns
t _{PLH} t _{PHL} Propagation delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)		1.5	9		12	ns
t _{PZH} t _{PZL} Switch turn-on time	C	A or B	C _L = 50 pF, R _L = 1 k Ω (see Figure 5)		3	18		22	ns
t _{PLZ} t _{PHZ} Switch turn-off time	C	A or B	C _L = 50 pF, R _L = 1 k Ω (see Figure 5)		7.2	18		22	ns

SN74AHC4066

QUADRUPLE BILATERAL ANALOG SWITCH

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH} t _{PHL}	Propagation delay time	A or B	B or A	C _L = 15 pF, (see Figure 4)	0.3	4		7	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)	1.6	7		10	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)	3.2	7		10	ns
t _{PLH} t _{PHL}	Propagation delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)	0.6	6		8	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)	2.1	12		16	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)	5.1	12		16	ns

analog switch characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) 20log ₁₀ (V _O /V _I) = -3 dB (see Figure 6)	2.3 V		30		MHz
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Figure 7)	2.3 V		-45		dB
				3 V		-45		
				4.5 V		-45		
Crosstalk (control input to signal output)	C	A or B	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8)	2.3 V		15		mV
				3 V		20		
				4.5 V		50		
Feed-through attenuation (switch off)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (see Figure 9)	2.3 V		-40		dB
				3 V		-40		
				4.5 V		-40		
Sine-wave distortion	A or B	B or A	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10)	V _I = 2 V _{p-p}	2.3 V	0.1		%
				V _I = 2.5 V _{p-p}	3 V	0.1		
				V _I = 4 V _{p-p}	4.5 V	0.1		

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	4.5	pF



PARAMETER MEASUREMENT INFORMATION

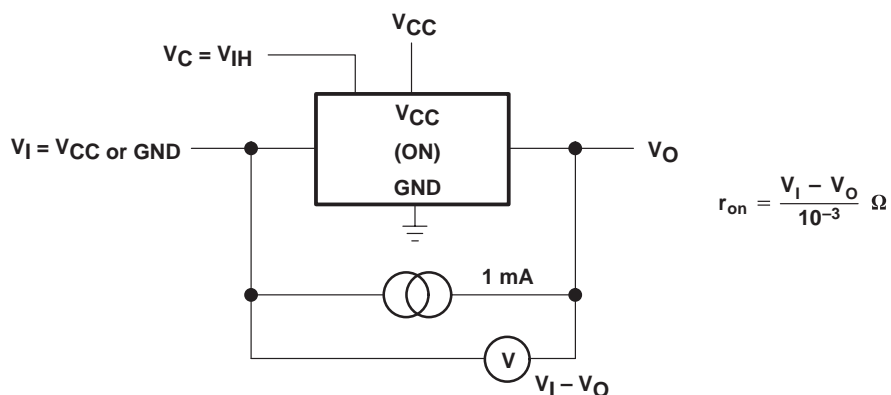


Figure 1. On-State Resistance Test Circuit

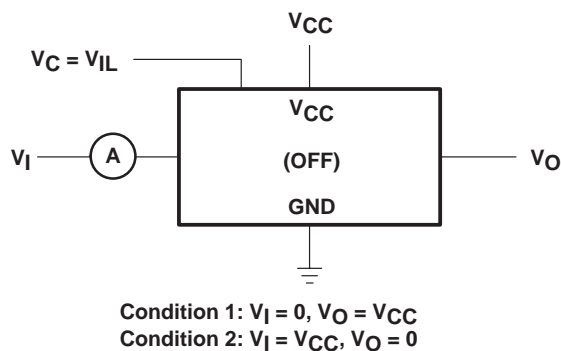


Figure 2. Off-State Switch Leakage-Current Test Circuit

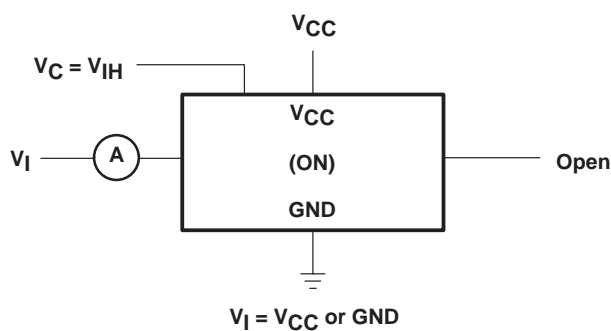


Figure 3. On-State Leakage-Current Test Circuit

SN74AHC4066
QUADRUPLE BILATERAL ANALOG SWITCH

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PARAMETER MEASUREMENT INFORMATION

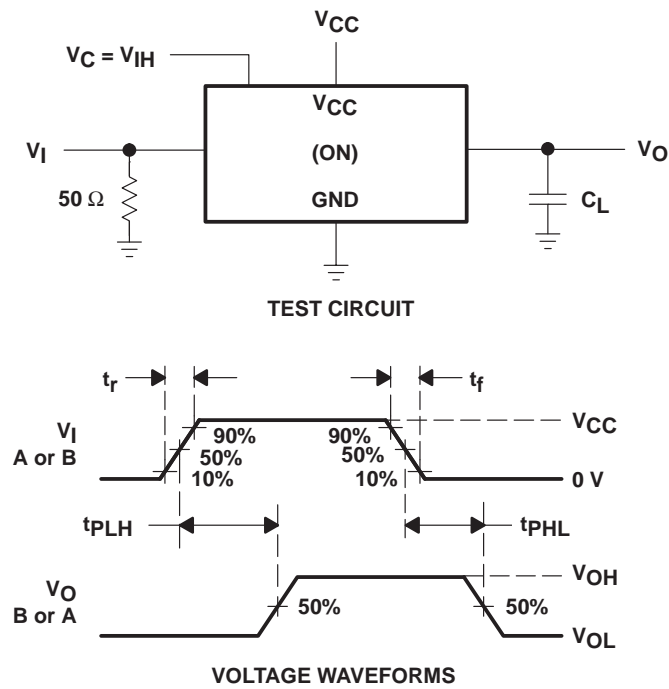
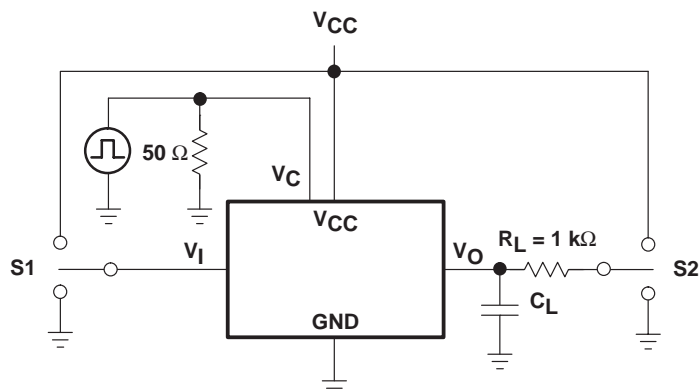


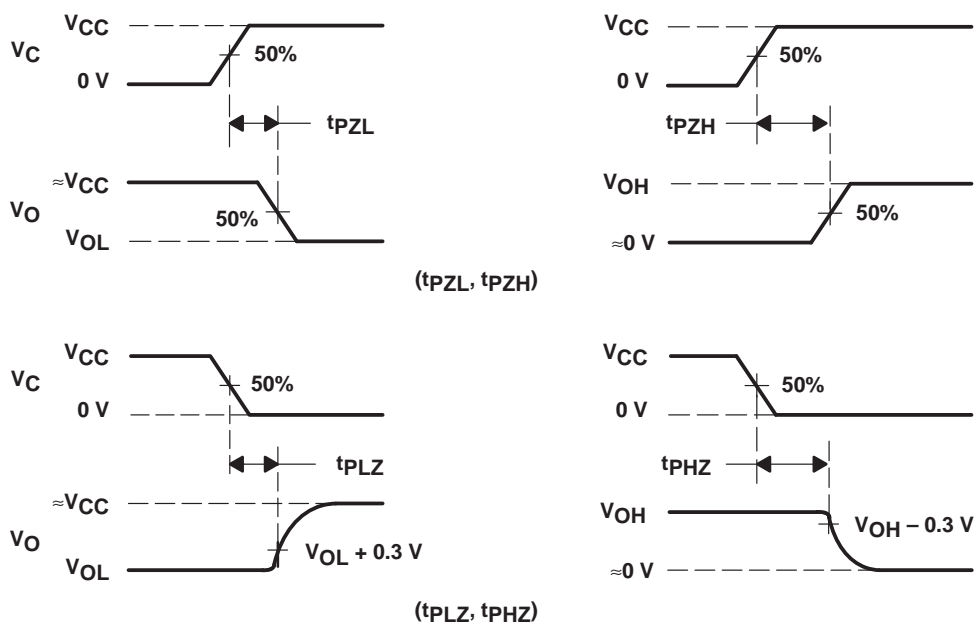
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST	S1	S2
tPZL	GND	VCC
tPZH	VCC	GND
tPLZ	GND	VCC
tPHZ	VCC	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (tPZL, tPLZ, tPZH, tPHZ), Control to Signal Output

The diagram shows a CMOS inverter circuit. The input signal f_{in} is connected to the inverter's input through a $50\ \Omega$ resistor. A $0.1\ \mu\text{F}$ capacitor is connected between the input and the inverter's input node, which is labeled V_I . The inverter is represented by a box with V_{CC} (ON) and GND labels. The output of the inverter is connected to a load resistor $R_L = 600\ \Omega$ and a load capacitor $C_L = 50\ \text{pF}$. The output node is labeled V_O . The inverter's supply voltage is V_{CC} , and its ground is GND. A note $V_{CC}/2$ is shown near the load resistor, indicating the initial output voltage.

The top circuit diagram shows a CMOS inverter with its control input $V_C = V_{CC}$. The input signal f_{in} is a square wave with a period of $0.1 \mu F$ and a frequency of 600Ω . The input signal is connected to the inverter's input V_I through a 600Ω resistor. The inverter's output V_{O1} is connected to a load resistor $R_L = 600 \Omega$ and a load capacitor $C_L = 50 pF$. The output signal V_{O1} is a square wave with a period of $0.1 \mu F$ and a frequency of 600Ω . The bottom circuit diagram shows a CMOS inverter with its control input $V_C = GND$. The input signal f_{in} is a square wave with a period of $0.1 \mu F$ and a frequency of 600Ω . The input signal is connected to the inverter's input V_I through a 600Ω resistor. The inverter's output V_{O2} is connected to a load resistor $R_L = 600 \Omega$ and a load capacitor $C_L = 50 pF$. The output signal V_{O2} is a square wave with a period of $0.1 \mu F$ and a frequency of 600Ω . A graph of the input signal v_i is shown on the right, which is a square wave.

The diagram shows a CMOS inverter circuit. The input is connected to a voltage divider consisting of a 50 Ω resistor and a 600 Ω resistor, both connected to ground. The input node is also connected to a square wave voltage source. The inverter's output is connected to a load resistor $R_L = 600\ \Omega$ and a load capacitor $C_L = 50\ \text{pF}$, both connected to ground. The output node is labeled V_O . The inverter's supply voltage is V_{CC} and its ground is GND . The input node is labeled V_C . The output node is labeled V_O . The load resistor and capacitor are labeled $R_L = 600\ \Omega$ and $C_L = 50\ \text{pF}$ respectively. The input node is labeled $V_{CC}/2$ and the output node is labeled $V_{CC}/2$.



PARAMETER MEASUREMENT INFORMATION

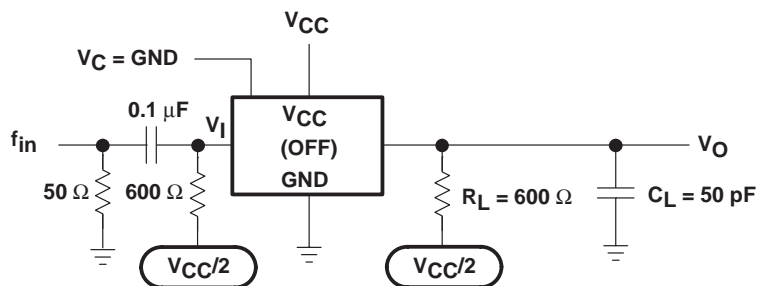


Figure 9. Feed-Through Attenuation (Switch Off)

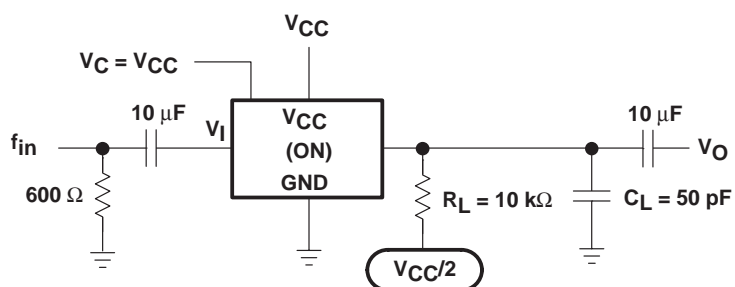


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC4066D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066DGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHC4066NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

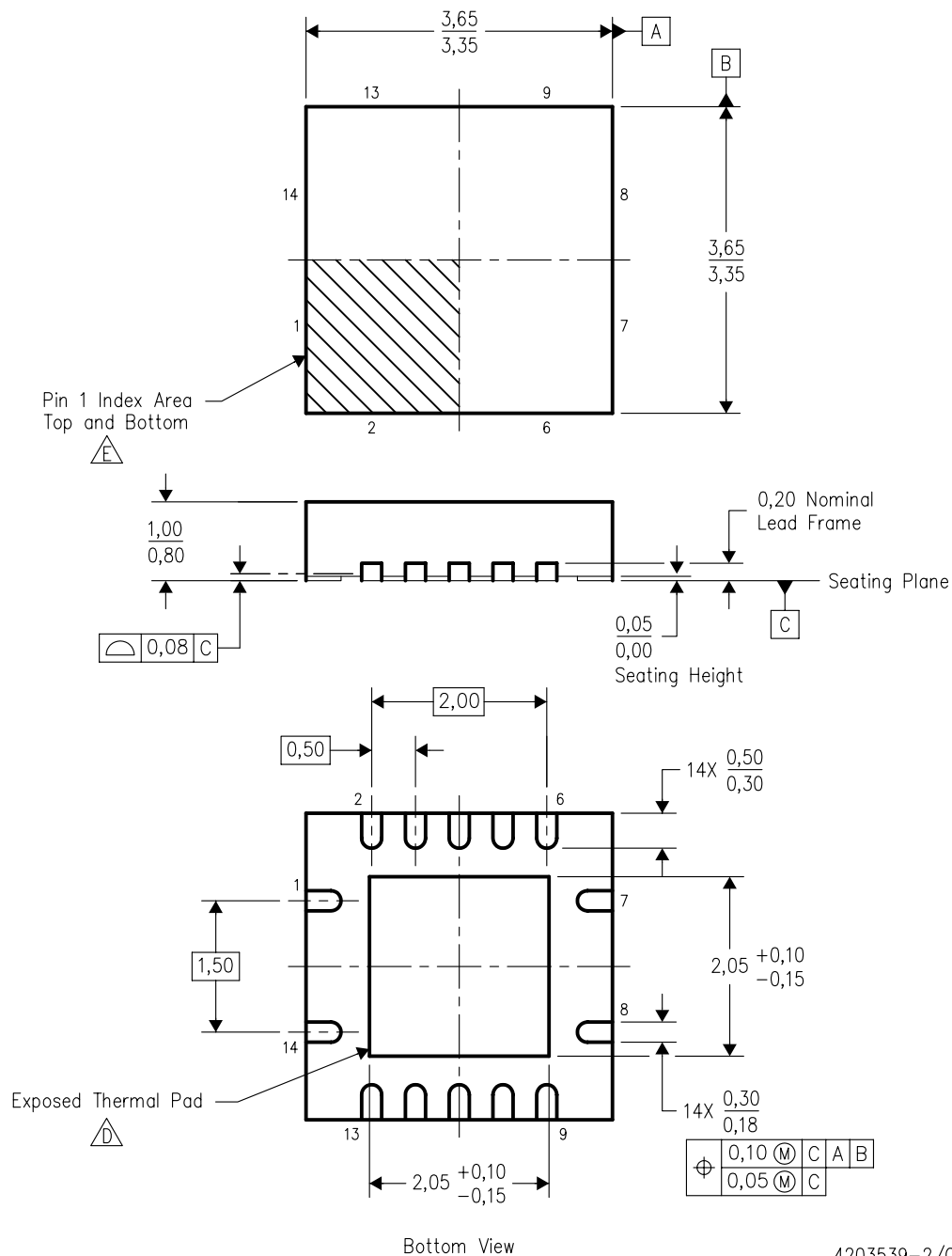


NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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