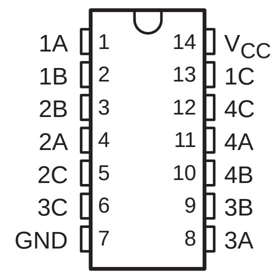
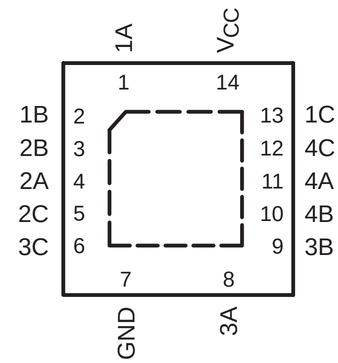
- **2-V to 5.5-V V_{CC} Operation**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V V_{CC} operation.

This switch is designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC4066N	SN74AHC4066N
	QFN – RGY	Tape and reel	SN74AHC4066RGYR	HA4066
	SOIC – D	Tube	SN74AHC4066D	AHC4066
		Tape and reel	SN74AHC4066DR	
	SOP – NS	Tube	SN74AHC4066NS	AHC4066
		Tape and reel	SN74AHC4066NSR	
	SSOP – DB	Tube	SN74AHC4066DB	HA4066
		Tape and reel	SN74AHC4066DBR	
	TSSOP – PW	Tube	SN74AHC4066PW	HA4066
		Tape and reel	SN74AHC4066PWR	
	TVSOP – DGV	Tape and reel	SN74AHC4066DGVR	HA4066

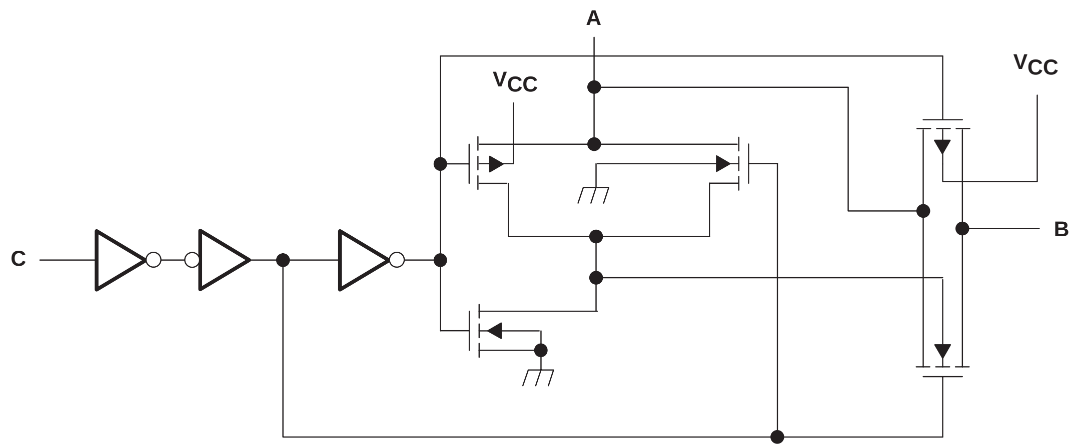
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



One of Four Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Control-input clamp current, I_{IK} ($V_I < 0$) . . . . . –20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$) . . . . . ±50 mA
On-state switch current, I_T (V_{IO} = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 86°C/W
(see Note 3): DB package . . . . . 96°C/W
(see Note 3): DGV package . . . . . 127°C/W
(see Note 3): N package . . . . . 80°C/W
(see Note 3): NS package . . . . . 76°C/W
(see Note 3): PW package . . . . . 113°C/W
(see Note 4): RGY package . . . . . 47°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2†	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
r_{on}	On-state switch resistance	I_T = –1 mA, V_I = V_{CC} or GND, V_C = V_{IH} (see Figure 1)	2.3 V		38	180		225	Ω
			3 V		29	150		190	
			4.5 V		21	75		100	
$r_{on(p)}$	Peak on-state resistance	I_T = –1 mA, V_I = V_{CC} to GND, V_C = V_{IH}	2.3 V		143	500		600	Ω
			3 V		57	180		225	
			4.5 V		31	100		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = –1 mA, V_I = V_{CC} to GND, V_C = V_{IH}	2.3 V		6	30		40	Ω
			3 V		3	20		30	
			4.5 V		2	15		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1	µA
$I_{S(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_C = V_{IL} (see Figure 2)	5.5 V			±0.1		±1	µA
$I_{S(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_C = V_{IH} (see Figure 3)	5.5 V			±0.1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5 V					20	µA
C_{ic}	Control input capacitance				1.5				pF
C_{io}	Switch input/output capacitance				5.5				pF
C_F	Feed-through capacitance				0.5				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C MIN	TYP	MAX	MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		1.2	10		16	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.3	15		20	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		6	15		23	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		2.6	12		18	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		4.2	25		32	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		9.6	25		32	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C MIN	TYP	MAX	MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.8	6		10	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		2.3	11		15	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		4.5	11		15	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		1.5	9		12	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		3	18		22	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		7.2	18		22	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.3	4		7	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		1.6	7		10	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.2	7		10	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		0.6	6		8	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		2.1	12		16	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		5.1	12		16	ns

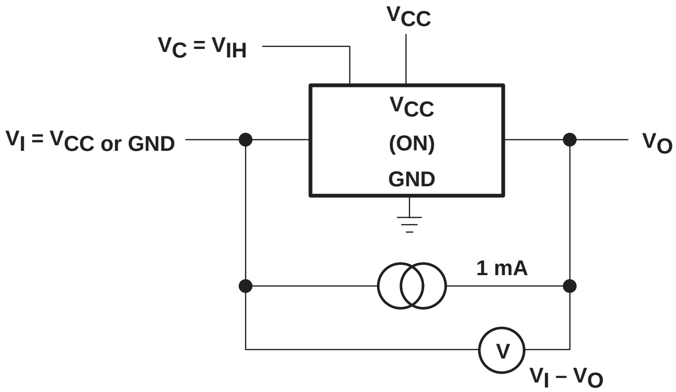
analog switch characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	UNIT
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) $20\log_{10}(V_O/V_I)$ = –3 dB (see Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		15		mV
					3 V		20		
					4.5 V		50		
Feed-through attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Figure 9)		2.3 V		–40		dB
					3 V		–40		
					4.5 V		–40		
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V		0.1		%
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

operating characteristics, T_A = 25°C

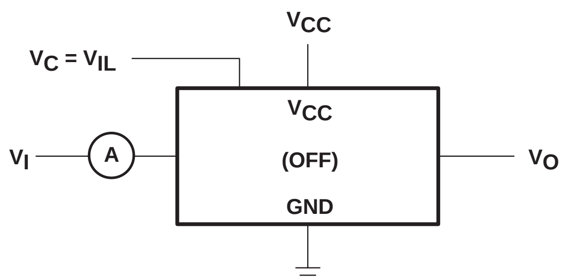
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	4.5	pF

PARAMETER MEASUREMENT INFORMATION



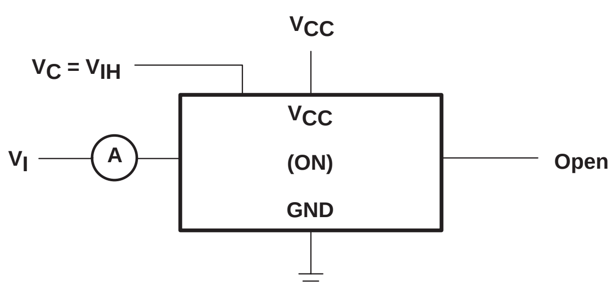
$$r_{on} = \frac{V_I - V_O}{10^{-3}}\ \Omega$$

Figure 1. On-State Resistance Test Circuit



Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit



$V_I = V_{CC}$ or GND

Figure 3. On-State Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

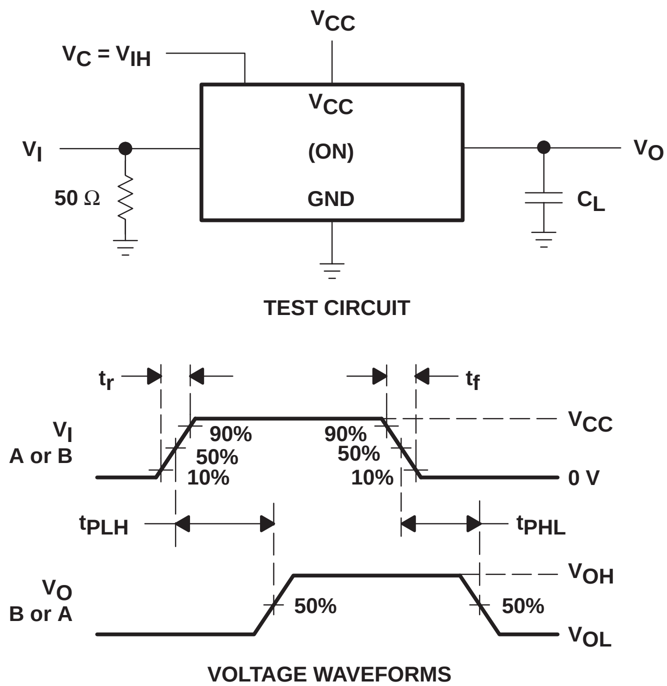
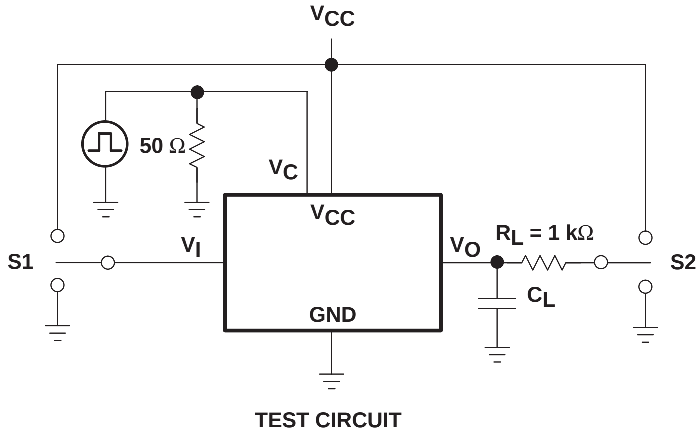


Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

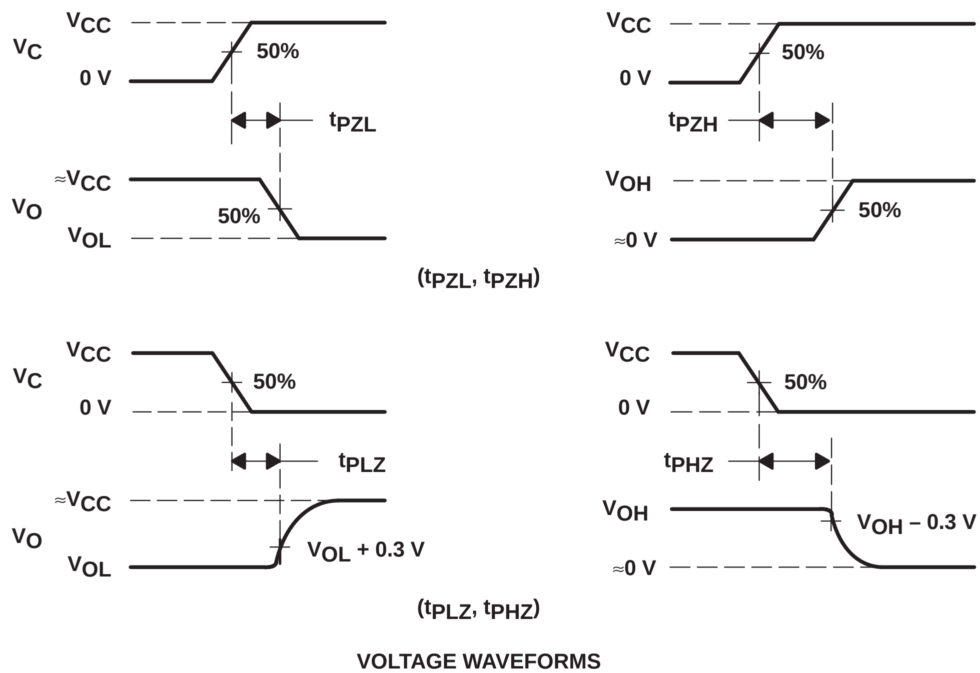


Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION

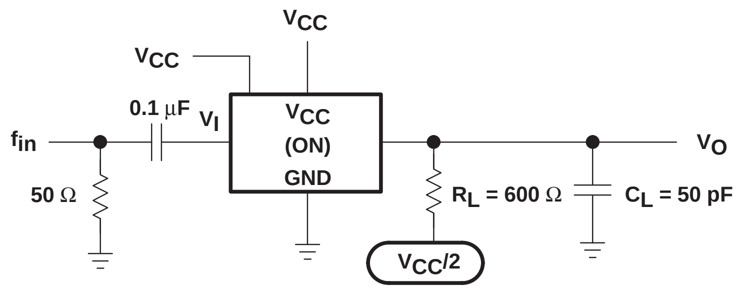


Figure 6. Frequency Response (Switch On)

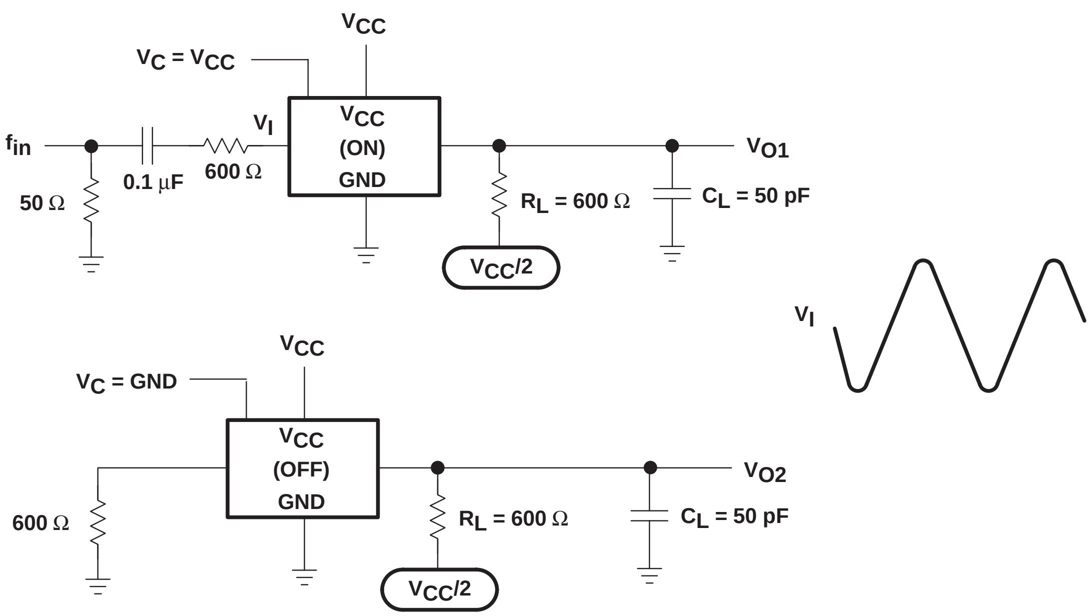


Figure 7. Crosstalk Between Any Two Switches

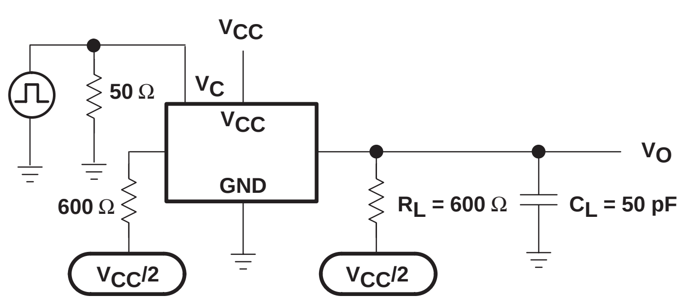


Figure 8. Crosstalk (Control Input – Switch Output)

PARAMETER MEASUREMENT INFORMATION

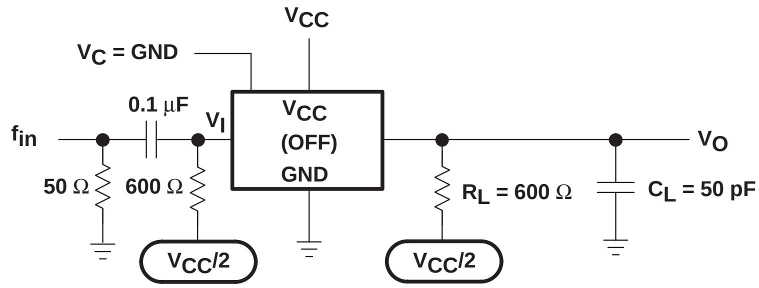


Figure 9. Feed-Through Attenuation (Switch Off)

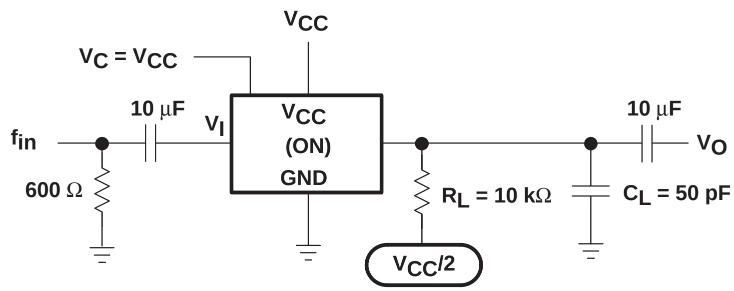


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AHC4066D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066DGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHC4066NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC4066PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC4066RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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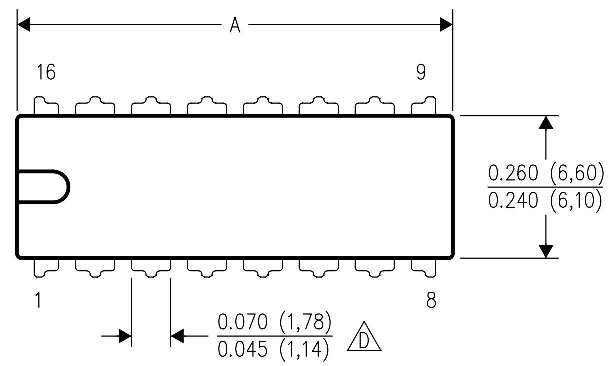
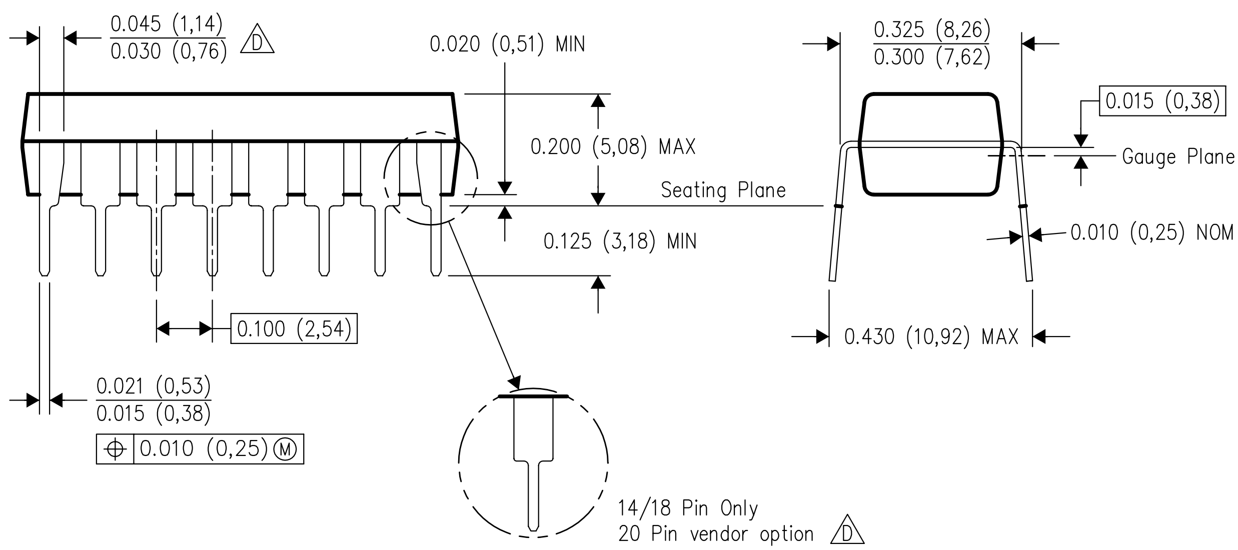
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

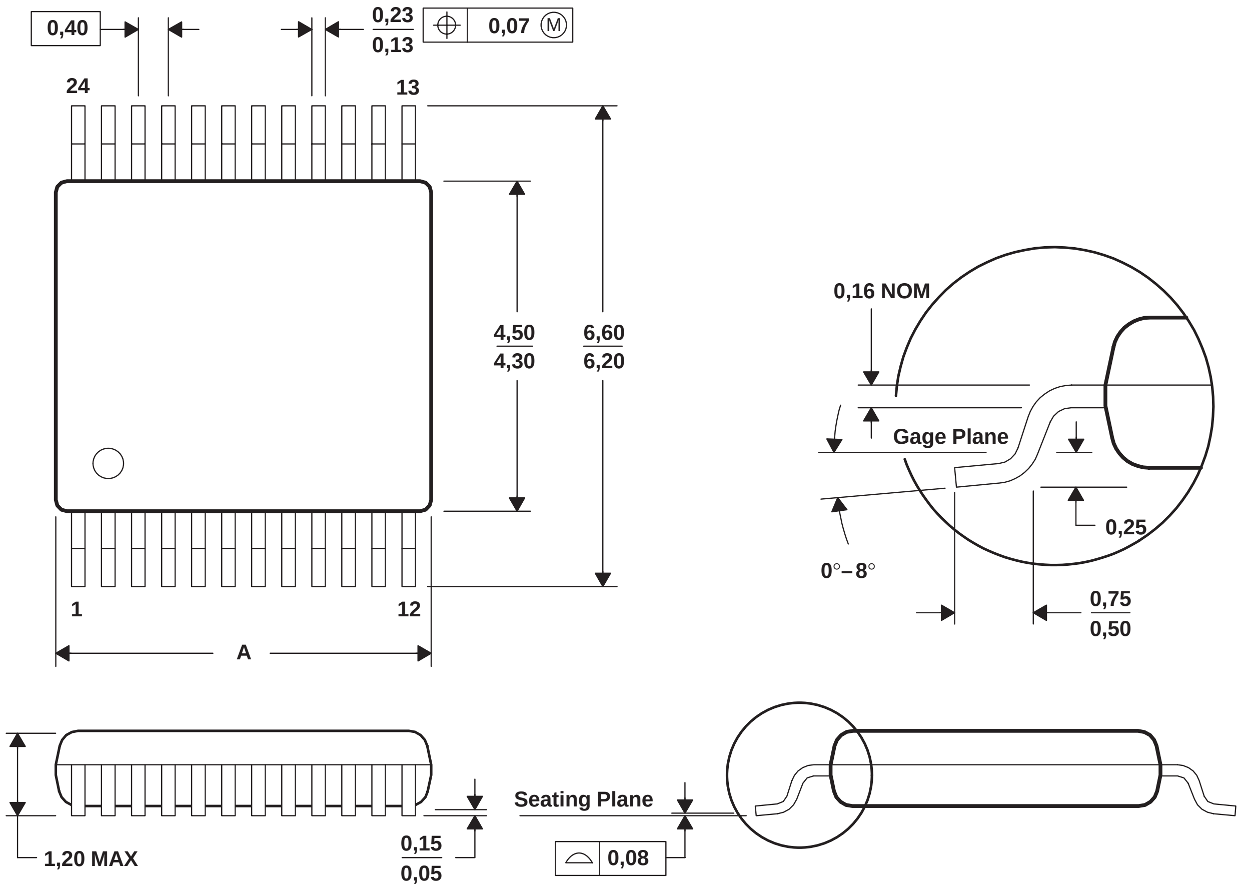


4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

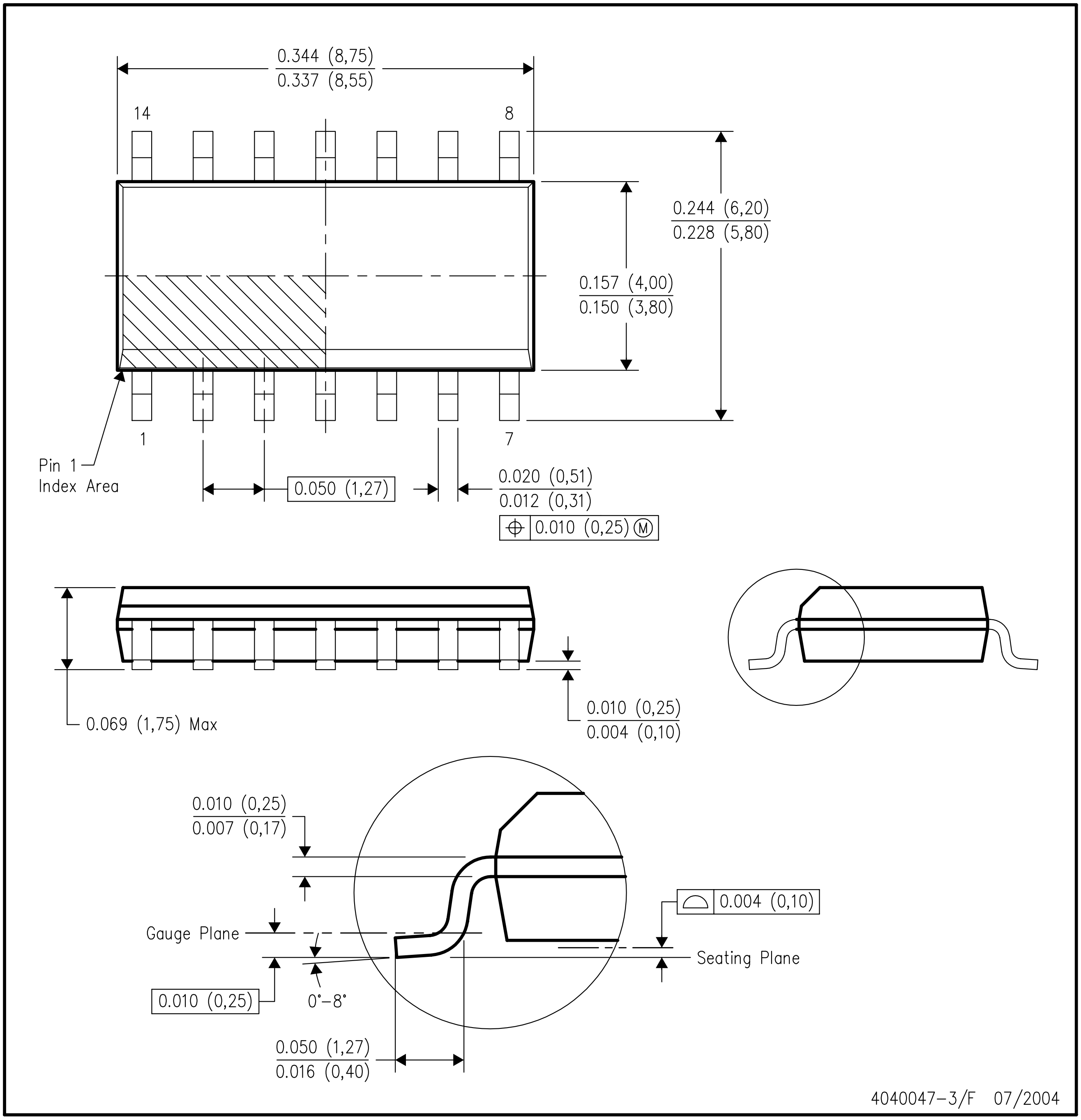


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

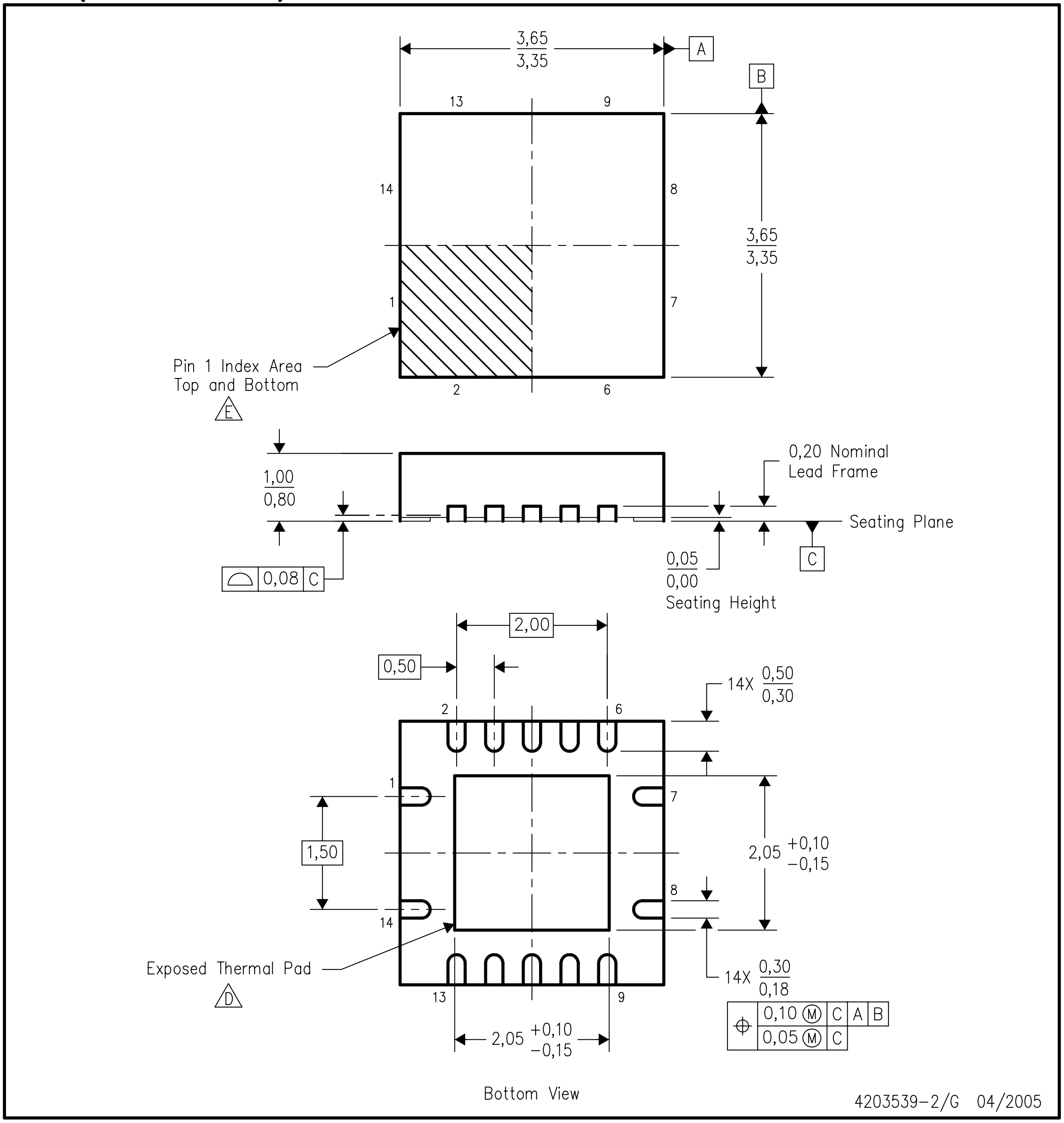
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

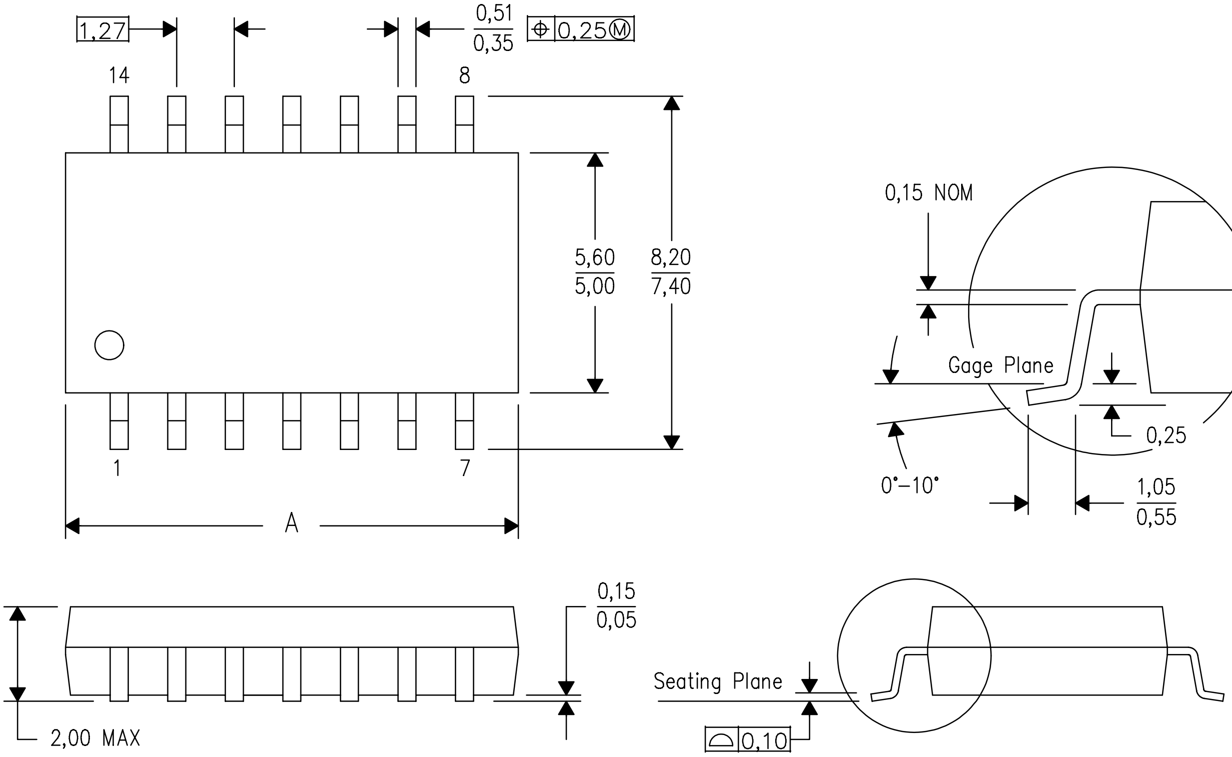
RGY (S–PQFP–N14) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- F. Package complies to JEDEC MO–241 variation BA.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



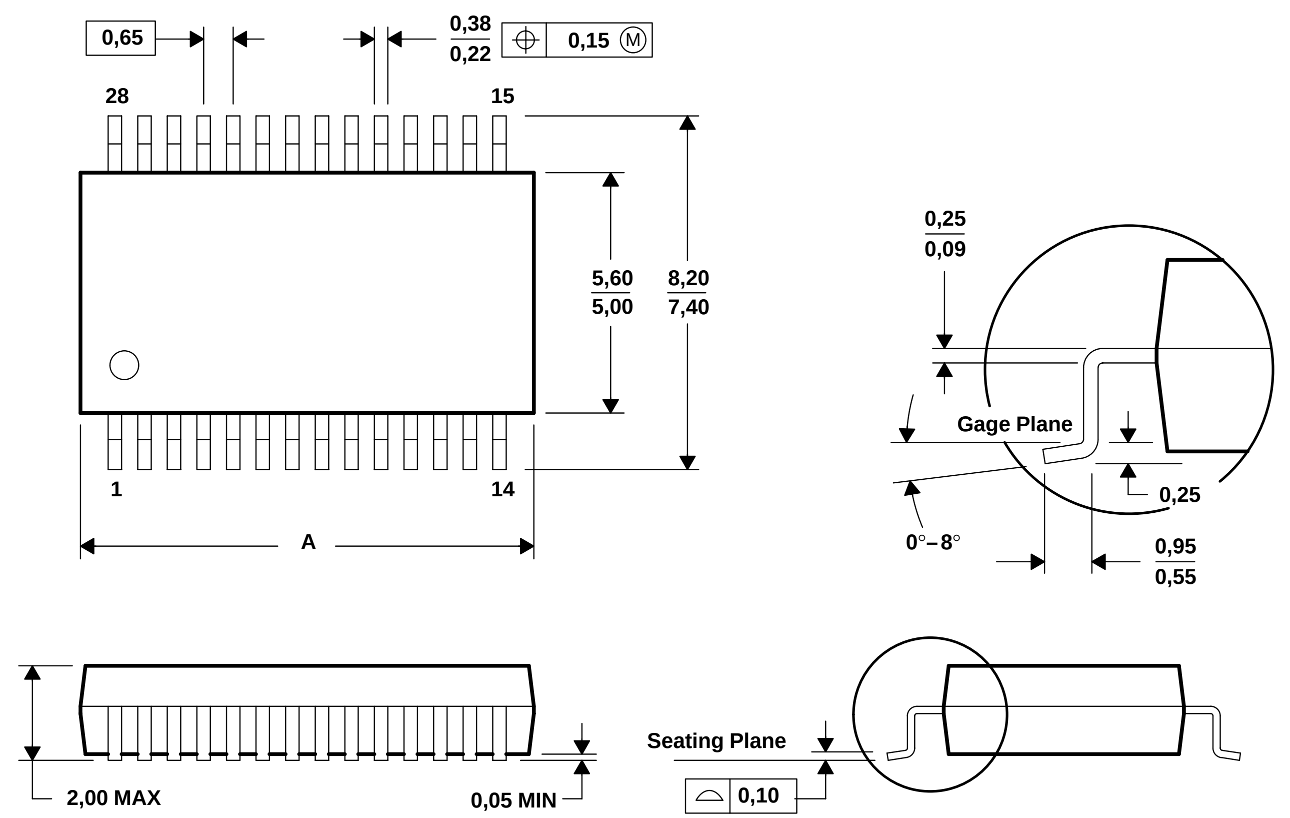
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



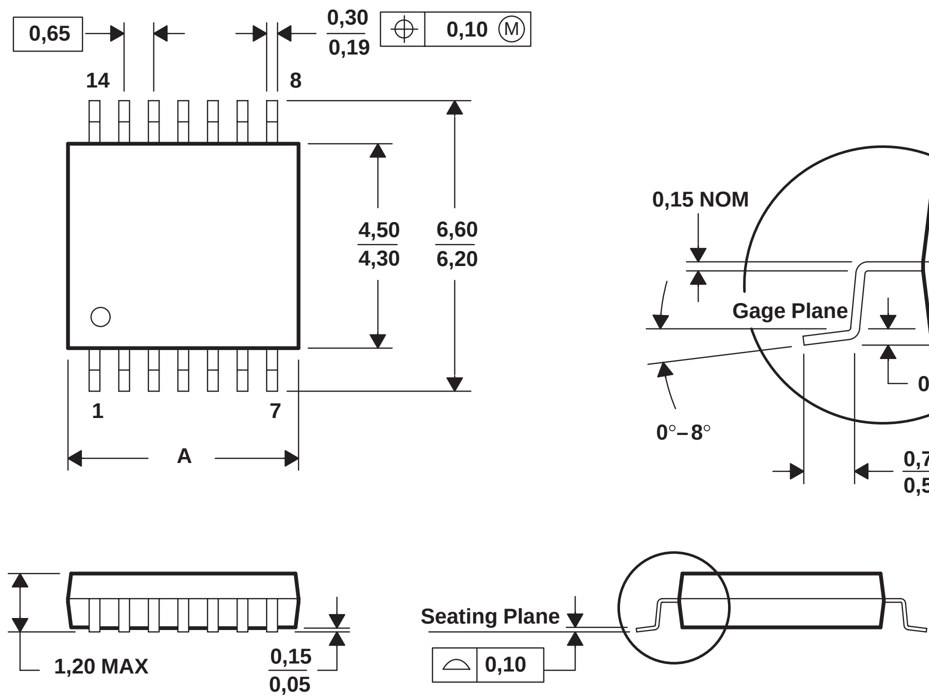
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
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