BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

FEATURES

- **Supply Current of 40 µA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Precision 5-V Supply Voltage Monitor, Other Voltage Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Watchdog Timer With 800-ms Time-Out**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Voltage Monitor for Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal (TPS3617 Only)**
- **8-Pin MSOP Package**
- **Temperature Range: -40°C to 85°C**

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

DESCRIPTION

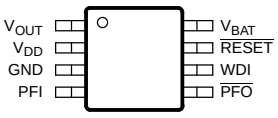
The TPS3617 and TPS3618 are battery-backup supervisors that monitor 5 V supplies. They provide a battery-backup function ideal for applications that require data retention of CMOS RAM during fault conditions. When the voltage at V_{DD} drops below a preset threshold (V_{IT}), the active low push-pull $\overline{\text{RESET}}$ output asserts, and V_{OUT} switches from V_{DD} to V_{BAT}. When V_{DD} rises above the trip threshold, V_{OUT} switches immediately from V_{BAT} to V_{DD}. The $\overline{\text{RESET}}$ output remains low until the delay time (t_d) expires. During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) goes higher than 1.1 V.

The PFI and $\overline{\text{PFO}}$ pins are provided if additional voltage monitoring is needed. If the voltage at PFI is less than 1.15 V, the push-pull $\overline{\text{PFO}}$ pin will assert low. When the voltage at PFI exceeds the threshold voltage, $\overline{\text{PFO}}$ will go high.

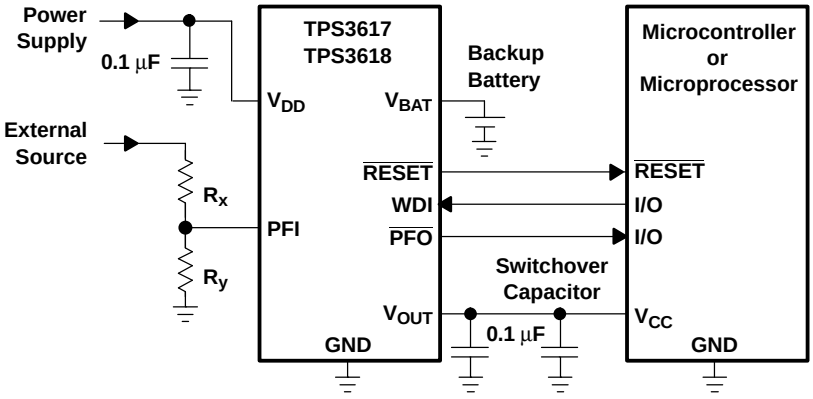
These devices also feature a watchdog timer pin (WDI) that monitors processor activity and asserts $\overline{\text{RESET}}$ if the processor is inactive longer than the watchdog timeout period. If the watchdog timer is not used, the WDI pin should be left floating.

The TPS3617 and TPS3618 are available in an 8-pin MSOP package and are characterized for operation over a temperature range of -40°C to 85°C.

MSOP (DGK) Package
(TOP VIEW)



ACTUAL SIZE
3,05 mm x 4,98 mm



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})(2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS3617-50	5V	4.55V	-40°C to +125°C	ASD	TPS3617-50DGK	Tube, 80
					TPS3617-50DGKR	Tape and Reel, 2500
TPS3618-50				ANK	TPS3618-50DGKT	Tape and Reel, 250
					TPS3618-50DGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com.
(2) For other threshold votages, contact the local TI sales office for availability and lead time.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

	TPS3617, TPS3618	UNIT
Input voltage range, V_{DD}	-0.3 to 7	V
Input voltage range, PFI pin	-0.3 to (V_{DD} + 0.3)	V
Continuous output current at V_{OUT}, I_O	400	mA
All other pins, I_O	±10	mA
Operating junction temperature range, T_J(2)	-40 to +85	°C
Storage temperature range, T_{STG}	-65 to +150	°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	+260	°C
Continuous total power dissipation	See Dissipation Rating Table	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

ELECTRICAL CHARACTERISTICS

1.65 V ≤ V_{DD} ≤ 5.5 V, R_{LRESET} = 1 MΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = -40°C to +85°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.65		5.5	V
I_{DD}	V_{DD} supply current	V_{OUT} = V_{DD}				40	µA
		V_{OUT} = V_{BAT}				40	
V_{BAT}	Battery supply range			1.5		5.5	V
I_{BAT}	V_{BAT} supply current	V_{OUT} = V_{DD}		-0.1		0.1	µ A
		V_{OUT} = V_{BAT}				0.5	
	Slew rate at V_{DD} or V_{BAT}					1	V/µs
V_I	Input volrage, any input			0		V_{DD} + 0.3	V
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V, I_{OH} = -400 µA	V_{DD} - 0.2			V
			V_{DD} = 3.3 V, I_{OH} = -2 mA, V_{DD} = 5 V, I_{OH} = -3 mA	V_{DD} - 0.4			
		$\overline{PFO}$	V_{DD} = 1.8 V, I_{OH} = -20 µA	V_{DD} - 0.3			
			V_{DD} = 3.3 V, I_{OH} = -80 µA, V_{DD} = 5 V, I_{OH} = -120 µA	V_{DD} - 0.4			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{DD} = 1.8 V, I_{OL} = 400 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA, V_{DD} = 5 V, I_{OL} = 3 mA			0.4	
V_{RES}	Power-up reset voltage (1)		V_{BAT} > 1.1 V, or V_{DD} > 1.1 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_O = 8.5 mA, V_{DD} = 1.8 V, V_{BAT} = 0 V	V_{DD} - 0.050			V
			I_O = 125 mA, V_{DD} = 3.3 V, V_{BAT} = 0 V	V_{DD} - 0.150			
			I_O = 200 mA, V_{DD} = 5 V, V_{BAT} = 0 V	V_{DD} - 0.200			
	Battery-backup mode		I_O = 0.5 mA, V_{BAT} = 1.5 V, V_{DD} = 0 V	V_{BAT} - 0.200			
			I_O = 7.5 mA, V_{BAT} = 3.3 V, V_{DD} = 0 V	V_{BAT} - 0.113			
$R_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V		0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		8	15	
I_O	Continuous output current at V_{OUT}					300	mA
V_{IT}	Negative-going input threshold voltage (2)	TPS3617-50	T_A = -40°C to 85°C	4.46	4.55		V
V_{PFI}		PFI		1.13	1.15	1.17	V
V_{HYS}	V_{IT} hysteresis		1.65 V < V_{IT} < 2.5 V		20		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5.5 V		60		
	PFI hysteresis				12		
	V_{BSW} hysteresis (3)		V_{DD} = 1.8 V		55		
V_{IH}	WDI high-level input voltage			0.7 x V_{DD}			
V_{IL}	WDI low-level input voltage					0.3 x V_{DD}	
I_{IH}	WDI high-level input current (4)		WDI = V_{DD} = 5 V			150	µA
I_{IL}	WDI low-level input current (4)		WDI = 0 V, V_{DD} = 5 V			-150	µA
	WDI input transition rise and fall rate, Δt/ΔV					100	ns/V
I_I	PFI input current		PFI voltage < V_{DD}	-25		25	nA
I_{OS}	$\overline{PFO}$ short-circuit current		$\overline{PFO}$ = 0 V, V_{DD} = 1.8 V			-0.3	mA
			$\overline{PFO}$ = 0 V, V_{DD} = 3.3 V			-1.1	
			$\overline{PFO}$ = 0 V, V_{DD} = 5 V			-2.4	

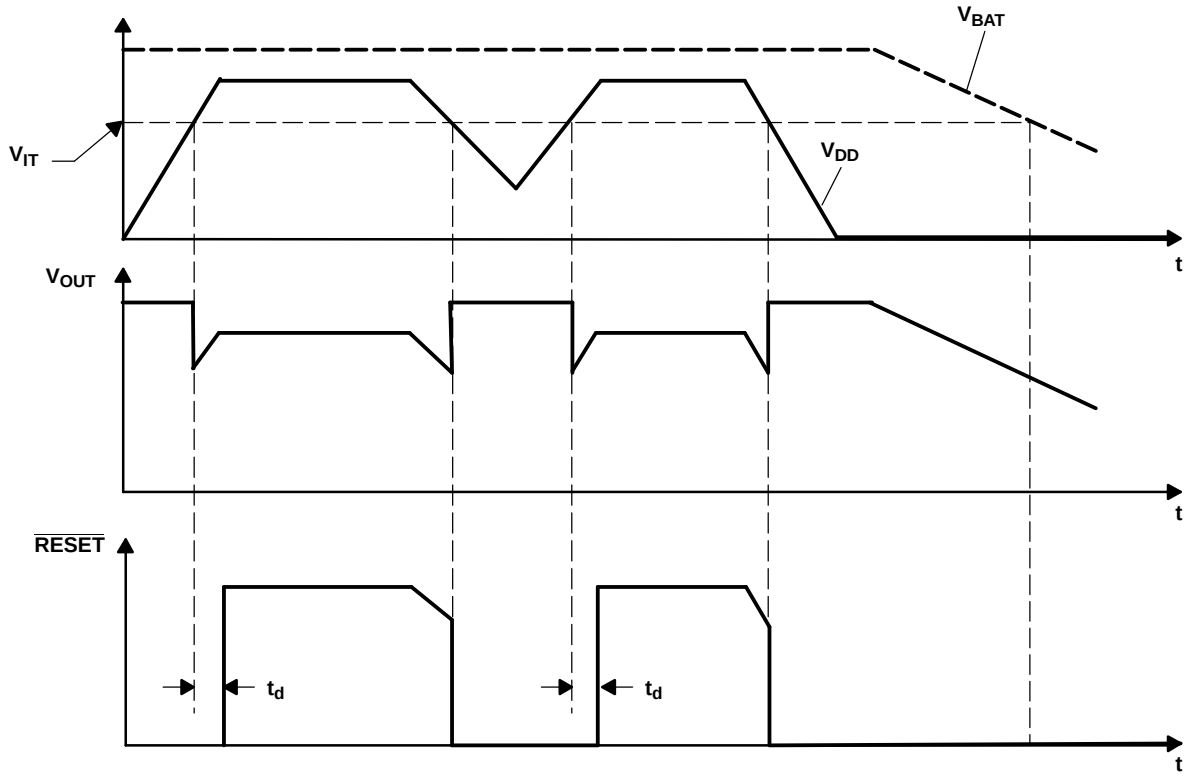
(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.
(3) For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}.
(4) For details on how to optimize current consumption when using WDI, refer to the *Watchdog* section of this data sheet.

ELECTRICAL CHARACTERISTICS (continued)

1.65 V ≤ V_{DD} ≤ 5.5 V, R_{LRESET} = 1 MΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = -40°C to +85°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance, any input		V_I = 0 V to 5 V		5		pF
t_w	Pulse Width	V_{DD}	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ - 0.2 V	6			µs
		WDI	$V_{DD} > V_{IT}$ + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns
t_d	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V, See timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog time-out		$V_{DD} > V_{IT}$ + 0.2 V, See timing diagram	0.48	0.8	1.12	s
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT}$ - 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V		2	5	µs
		PFI to $\overline{PFO}$	$V_{IL} = V_{PFI}$ - 0.2 V, $V_{IH} = V_{PFI}$ + 0.2 V		3	5	
Transition time		V_{DD} to V_{BAT}				3	µs

TIMING DIAGRAM



FUNCTION TABLE

$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	V_{OUT}	$\overline{RESET}$
0	0	V_{BAT}	0
0	1	V_{DD}	0
1	0	V_{DD}	1
1	1	V_{DD}	1

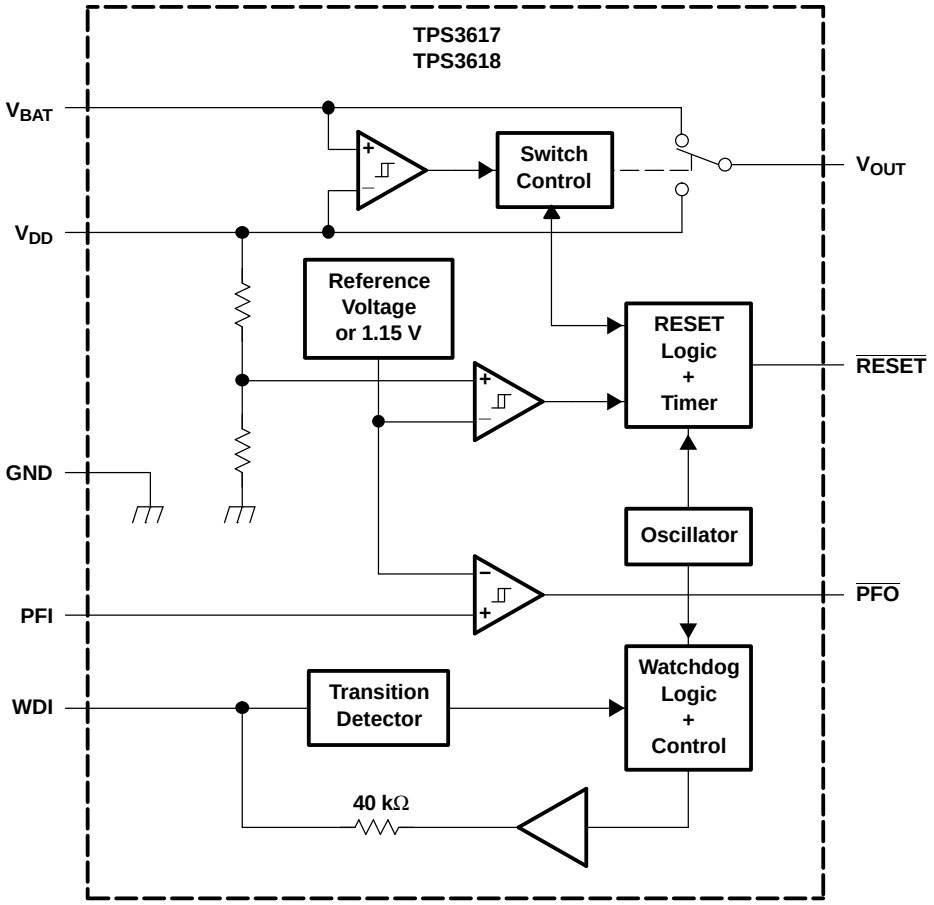
$\overline{\text{PFO}}$ FUNCTION TABLE

PFI > V_{PFI}	$\overline{\text{PFO}}$
0	0
1	1
CONDITION: $V_{DD} > V_{DD(MIN)}$	

TERMINAL FUNCTIONS

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	3	I	Ground
PFI	4	I	Power-fail comparator input
$\overline{\text{PFO}}$	5	O	Power-fail comparator output; asserts low when PFI < 1.15 V
$\overline{\text{RESET}}$	7	O	Active-low push-pull reset output
V_{BAT}	8	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output
WDI	6	I	Watchdog input. Should be left floating if not used.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	3
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})	vs Output current	4
I_{DD}	Supply current	vs Supply voltage	5
V_{IT}	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	6
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{PFO}$		9, 10
V_{OL}	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	11, 12
	Minimum pulse duration at V_{DD}	vs Threshold voltage overdrive at V_{DD}	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

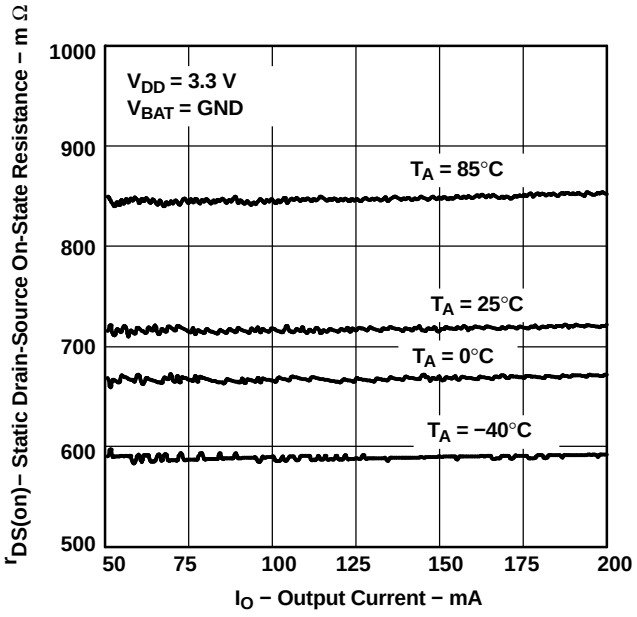


Figure 1.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

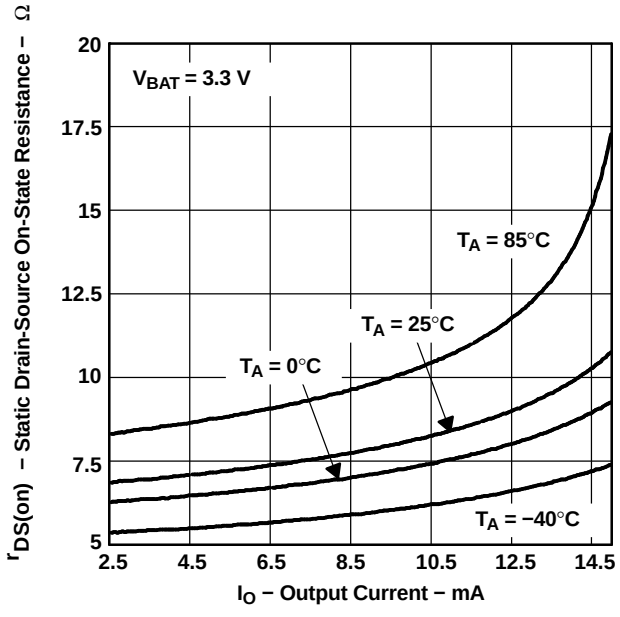


Figure 2.

SUPPLY CURRENT
vs
SUPPLE VOLTAGE

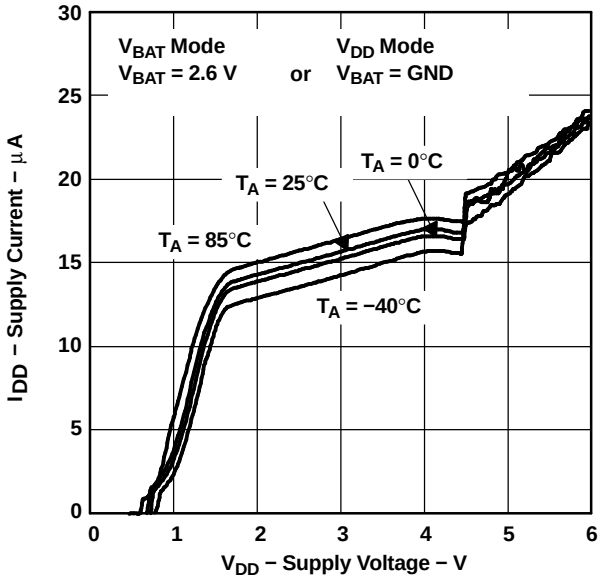


Figure 3.

INPUT THRESHOLD VOLTAGE AT $\overline{\text{RESET}}$
vs
FREE-AIR TEMPERATURE

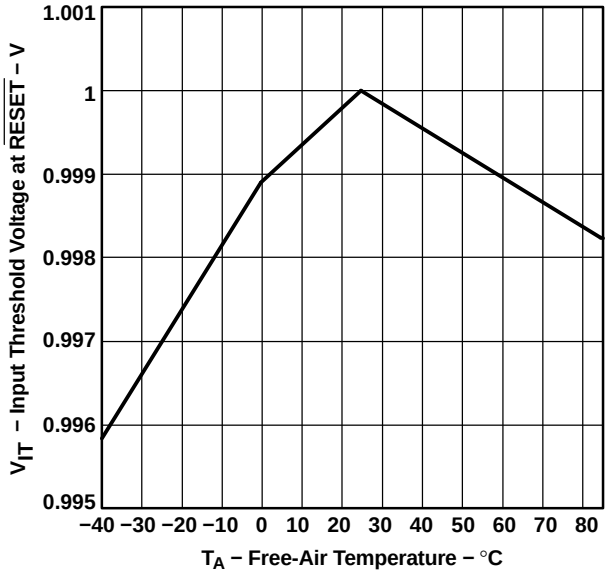


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

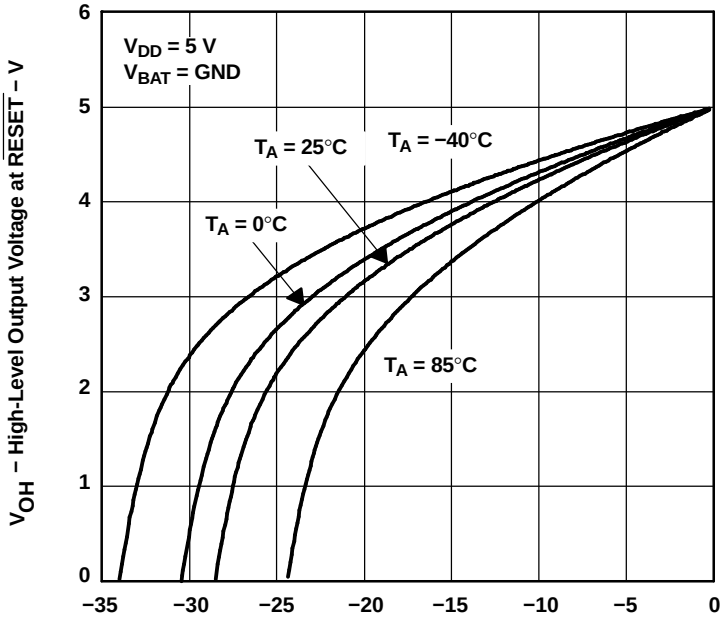


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

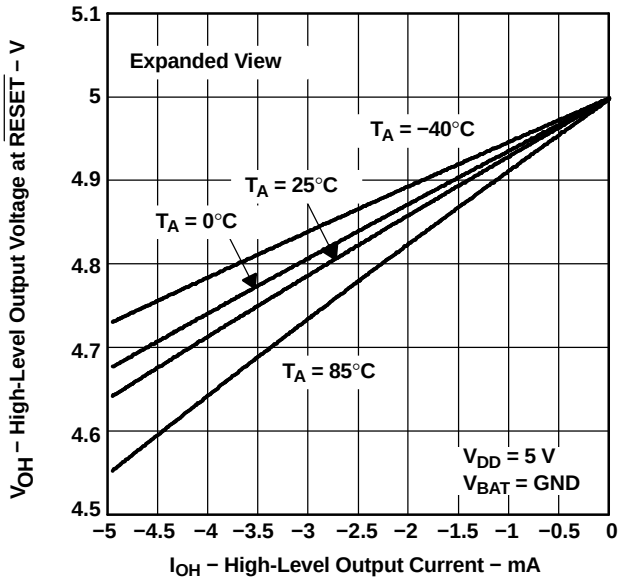


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$
vs
HIGH-LEVEL OUTPUT CURRENT

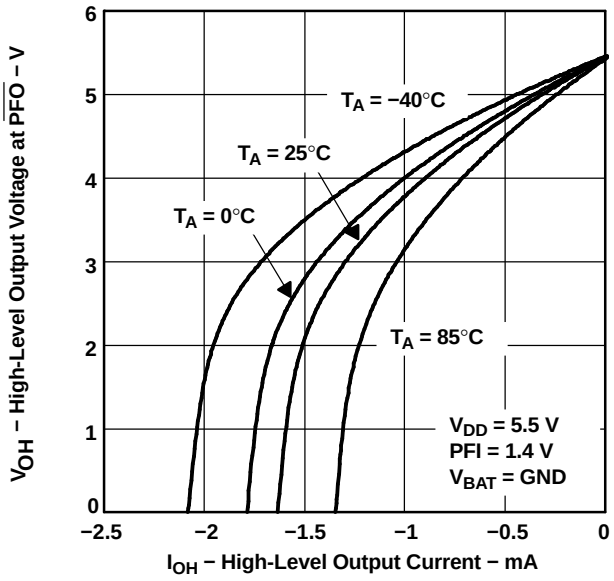


Figure 7.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{PFO}}$
vs
HIGH-LEVEL OUTPUT CURRENT

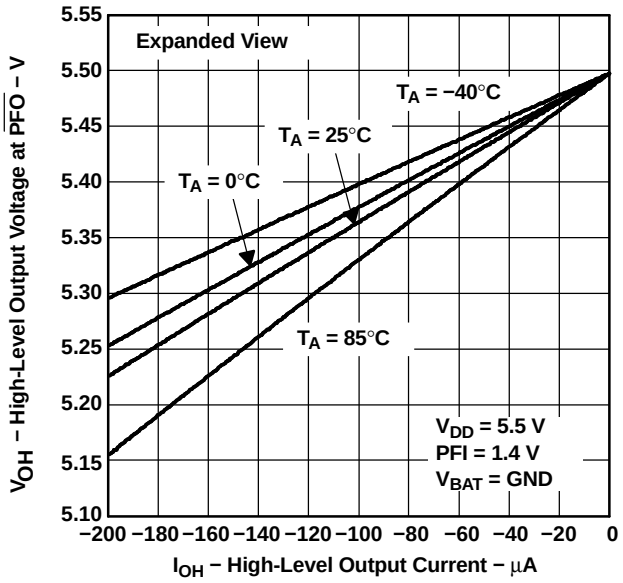


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

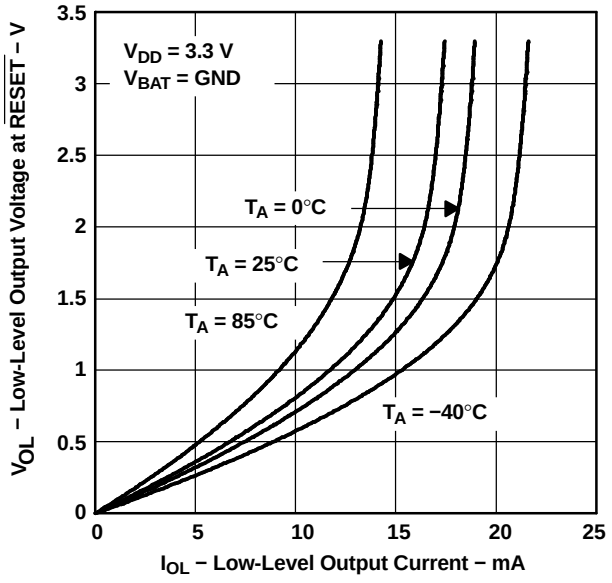


Figure 9.

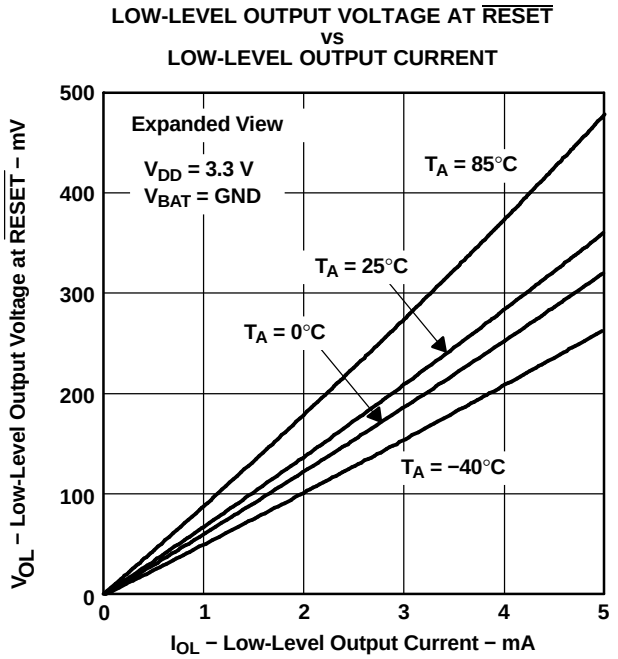


Figure 10.

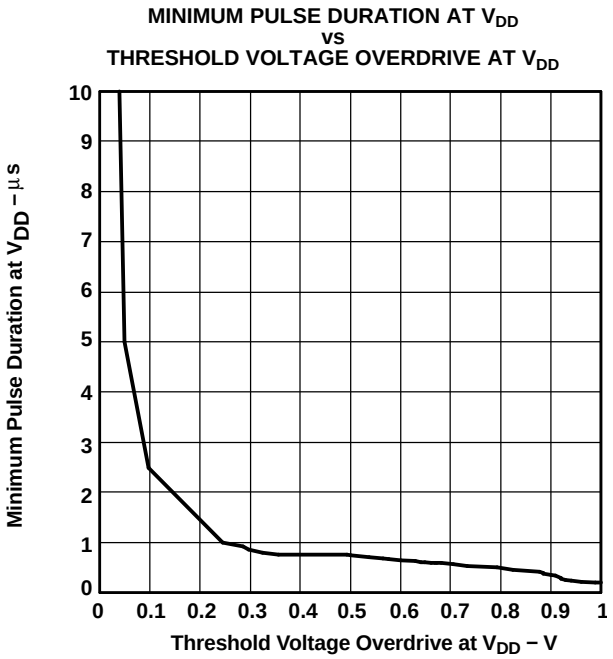


Figure 11.

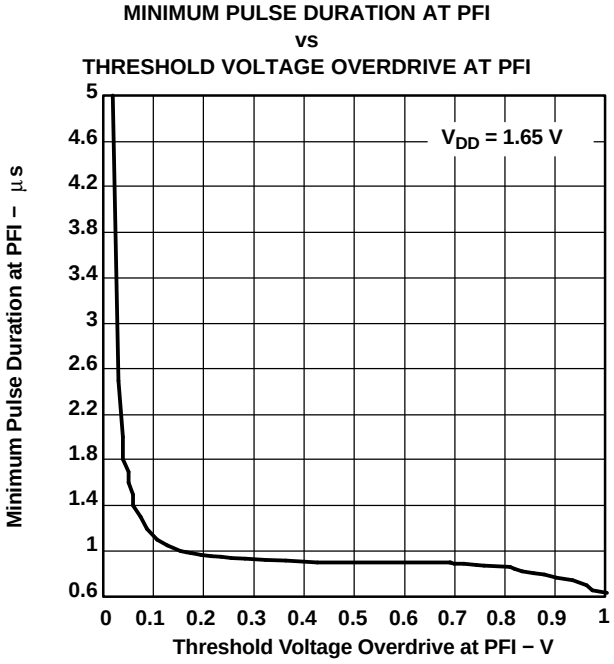


Figure 12.

DETAILED DESCRIPTION

BATTERY FRESHNESS SEAL (TPS3617 Only)

The battery freshness seal of the TPS3617 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V_{BAT} should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT(min)}$).
2. Ground $\overline{PFO}$.
3. Connect PFI to V_{DD} (PFI = V_{DD}).
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and keep connected for 5 ms < t < 35 ms.

The battery freshness seal mode is disabled by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

POWER-FAIL COMPARATOR (PFI AND $\overline{PFO}$)

An additional comparator monitors voltages other than the nominal supply voltage. The power-fail-input (PFI) can be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ($V_{(PFI)}$) of 1.15 V typical, the power-fail output ($\overline{PFO}$) goes low. If it goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of the sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave the $\overline{PFO}$ unconnected.

WATCHDOG

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to toggle the watchdog input within 0.8 s typically, to avoid a timeout from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and should be retriggered internally. See Figure 13 for the watchdog timing diagram.

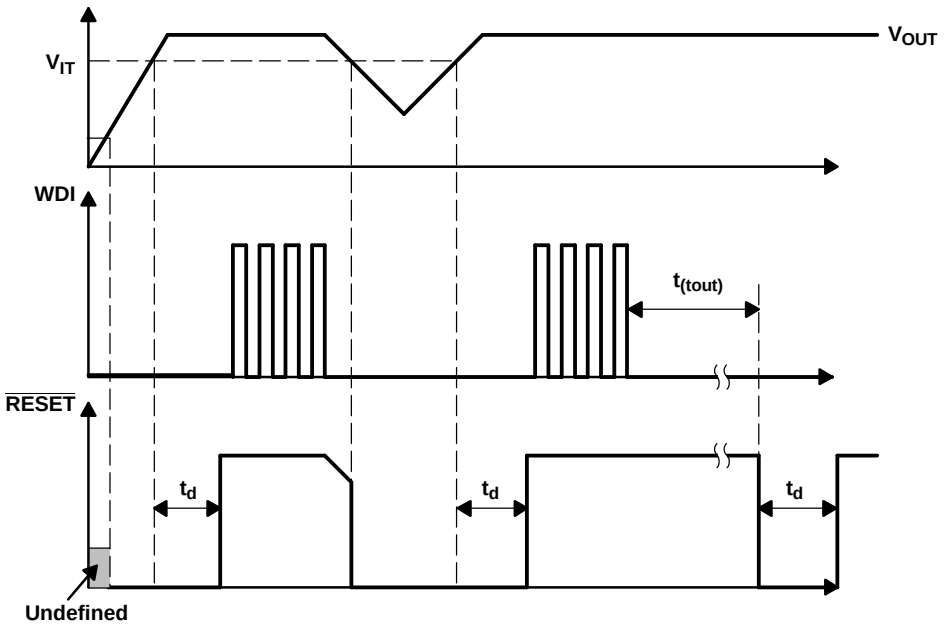


Figure 13. Watchdog Timing

DETAILED DESCRIPTION (continued)

SAVING CURRENT WHILE USING THE WATCHDOG

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5.0 V/40 kΩ ≈ 125 µA can flow into WDI.

BACKUP-BATTERY SWITCHOVER

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors should not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE		
$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

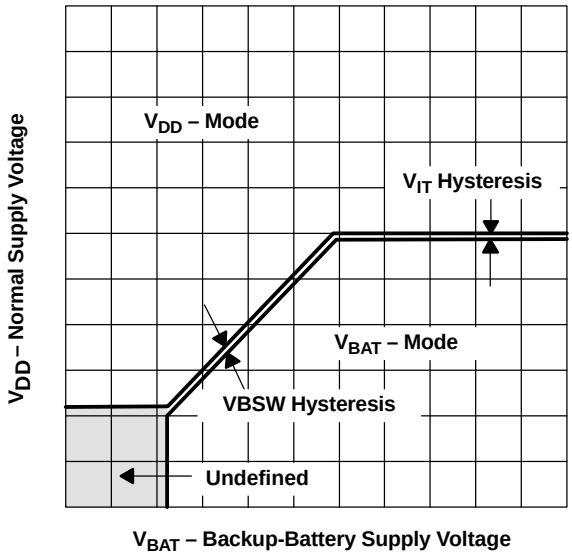


Figure 14. V_{DD} - V_{BAT} Switchover

PACKAGING INFORMATION

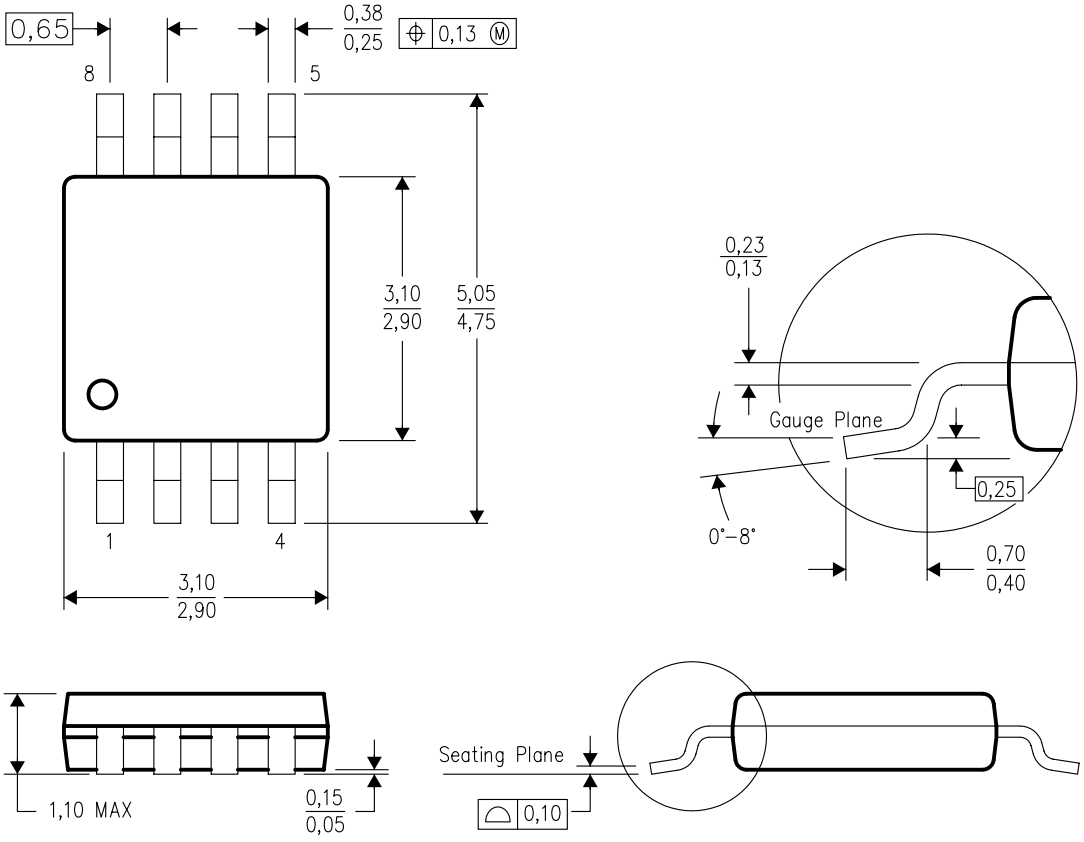
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3617-50DGK	ACTIVE	MSOP	DGK	8	80	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3617-50DGKR	ACTIVE	MSOP	DGK	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3618-50DGKR	ACTIVE	MSOP	DGK	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3618-50DGKT	ACTIVE	MSOP	DGK	8	250	None	CU NIPDAU	Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265