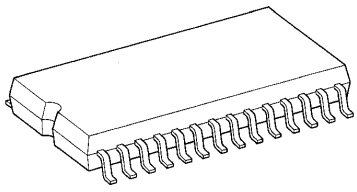
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9270F, TC9270N

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH A BUILT-IN DIGITAL ATTENUATOR DIGITAL FILTER

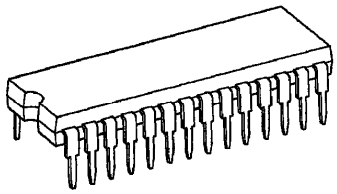
TC9270F, TC9270N are a 2'nd order Σ-Δ modulation system 1-bit DA converter with a built-in 8 times over sampling FIR type digital filter developed for digital audio equipment.
As the de-empahsis filter has been incorporation, it is possible to construct small the digital filter ~ the analog output unit at a low price.

TC9270F



SOP28-P-450-1.27

TC9270N



SDIP28-P-400-1.78

Weight
SOP28-P-450-1.27 : 0.8g (Typ.)
SDIP28-P-400-1.78 : 2.2g (Typ.)

FEATURES

- Built-in 8 times over-sampling FIR type digital filter.
- Over sampling ratio (OSR) of Σ-Δ modulation circuit is 384fs or 256fs.
- Built-in digital de-emphasis filter.
- Permits microcontrollers to attenuate output levels (128 steps) during serial mode.
- Simultaneous outputs L-ch and R-ch.
- Compatible with double speed operation.
- Built-in Digital 0 Detection.
- Pin of OSCE can be stopped system clock.
- Characteristics of the digital filter and DA converter are as follows.

DIGITAL FILTER

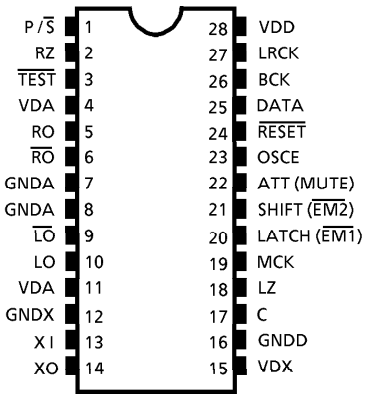
	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard Operation	8fs	±0.003dB	20k~24.1kHz	−68dB
Double Speed Operation	4fs	±0.05dB	20k~24.1kHz	−40dB

DA CONVERTER

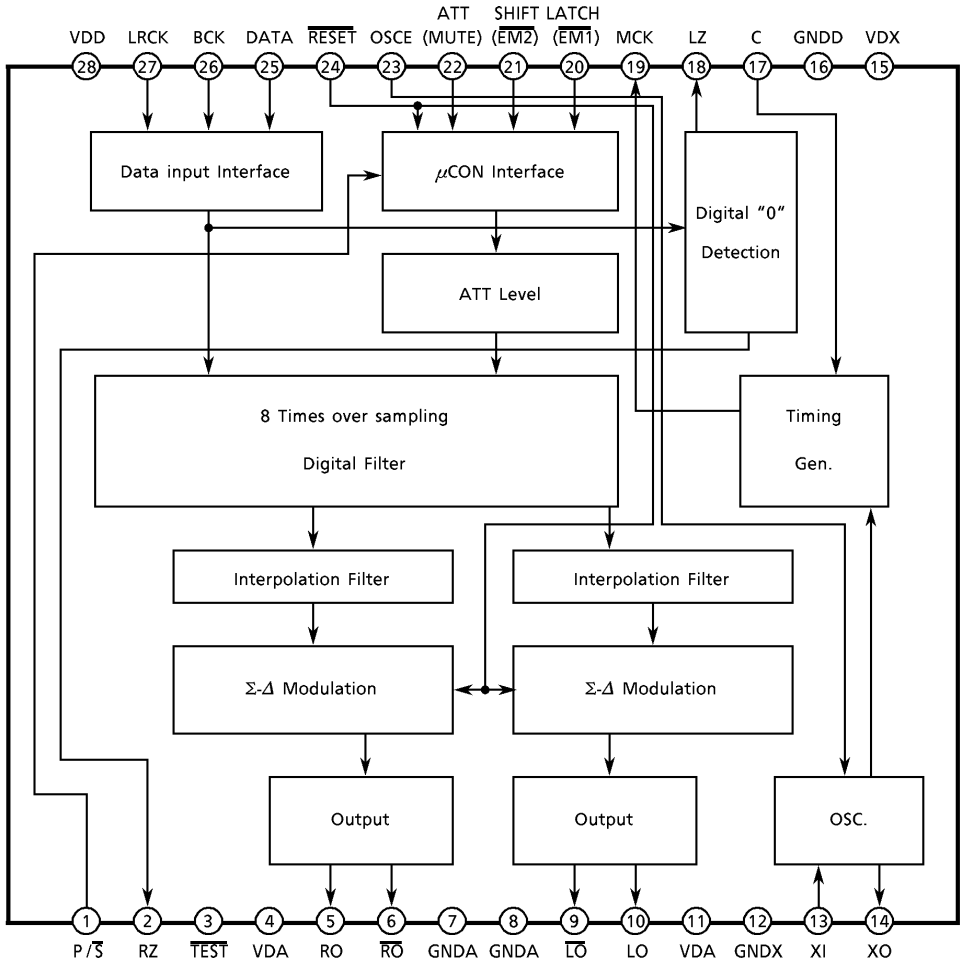
	OSR	NOISE DISTORATION	S/N RATIO
Standard Operation	384fs	−90dB (TYP)	100dB (TYP)
Double Speed Operation	192fs	−87dB (TYP)	98dB (TYP)

- 2 kinds of package, Pin 28 flat package and Pin 28 DIP shrunk package.

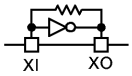
PIN CONNECION



BLOCK DIAGRAM



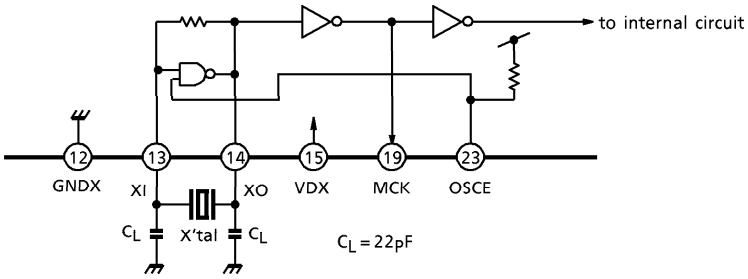
DESCRIPTION OF PIN FUNCTIONS

No.	SYMBOL	I / O	FUNCTION & OPERATION	REMARKS
1	P / $\overline{S}$	I	Parallel control, serial control, switching pin.	Pull-up resistance
2	RZ	O	R-ch digital "0" detection output pin.	
3	$\overline{TEST}$	I	Test pin. Normally, use at "H".	Pull-up resistance
4	VDA	—	Analog power supply pin.	
5	RO	O	R-ch data forward output pin.	
6	$\overline{RO}$	O	R-ch data reverse output pin.	
7	GNDA	—	Analog ground pin.	
8	GNDA	—	Analog ground pin.	
9	$\overline{LO}$	O	L-ch data reverse output pin.	
10	LO	O	L-ch data forward output pin.	
11	VDA	—	Analog power supply pin.	
12	GNDX	—	Crystal oscillator ground Pin.	
13	XI	I	Crystal oscillator connection pin. Connect to a crystal oscillator, generates needed frequency for the system.	
14	XO	O		
15	VDX	—	Crystal oscillator power supply pin.	
16	GNDD	—	Digtal ground pin.	
17	C	I	Clock Select pin. "L" ; 256fs, "H" ; 384fs.	Pull-up resistance
18	LZ	O	L-ch digital "0" detection output pin.	
19	MCK	O	System clock output pin.	
20	LATCH ($\overline{EM1}$)	I	Serial mode : Data latch signal input pin. Parallel mode : De-emphasis filter mode select pin.	Pull-up resistance
21	SHIFT ($\overline{EM2}$)	I	Serial mode : Shift clock input pin. Parallel mode : De-emphasis filter mode select pin.	Pull-up resistance
22	ATT (MUTE)	I	Serial mode : Data input pin. Parallel mode : Soft mute cantrol pin. ("H" Soft mute ON)	Pull-up resistance
23	OSCE	I	System clock control pin. "L" : System clock stop	Pull-up resistance
24	$\overline{RESET}$	I	Reset pin. "L" : Reset Σ-Δ circuit and ATT data 00 (HEX)	Pull-up resistance
25	DATA	I	Audio data input pin.	
26	BCK	I	Bit clock input pin.	
27	LRCK	I	LR clock input pin.	
28	VDD	—	Digital power supply pin.	

OPERATION DESCRIPTION FOR EACH BLOCK

1. CRYSTAL OSCILLATION CIRCUIT AND TIMING GENERATOR

Clock required for internal operation can be generated when crystal and capacitors are connected as shown in FIG.1 So external system clock signal may be applied to the X1 terminal at Pin 13. However are must be taken in using system clock since the S / N ratio and noise distortion performance can be greatly affected by Jitter, rise and fall characteristics··· etc. of system clock.



Use crystal with Low CI value and quick response.

FIG.1 Configuration of crystal oscillation circuit

The timing generator generates the timing signal for digital filter, digital attennator, de-emphasis filter Σ-Δ demodulator circuit.

C (Pin 17)	XI INPUT CLOCK
L	256fs
H	384fs

Internal system clock can be stopped by OSCE pin but output of DAC will become unstable.

OSCE (Pin 23)	SYSTEM CLOCK
L	Stop
H	Normal operation

2. DATA INPUT CIRCUIT

Data and LRCK are taken into the shift register at the leading edge of BCK.
As shown in the following timing example, it is necessary to input data and LRCK synchronized with the falling edge of BCK.
In parallel mode ($P/\overline{S}$ = "H"), input data length is fixed to 16 bits.
In serial mode ($P/\overline{S}$ = "L"), input data length can be selected to 16, 18, or 20bits.

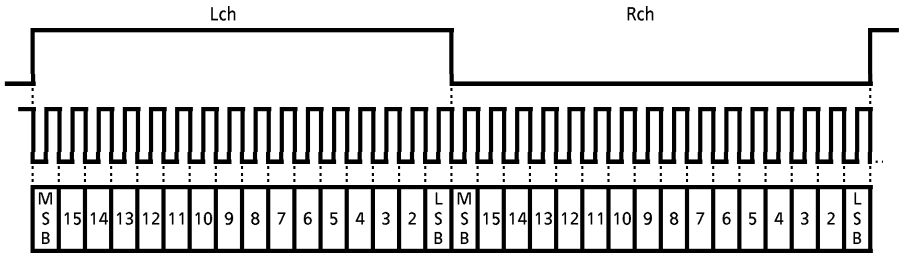


FIG.2a Example of input timing diagram (16 bit Input)

If BCK is 48fs or 64fs, please input DATA as follows.

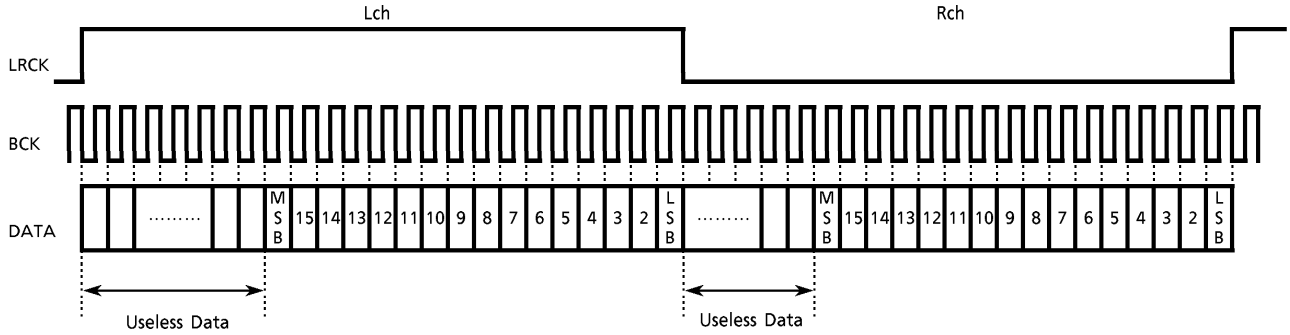
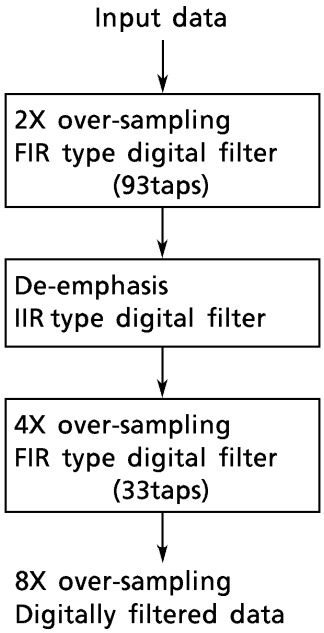


FIG.2b Example of input timing diagram (16 bit input)
When BCK = 48fs or 64fs.

3. DIGITAL FILTER, DE-EMPHASIS FILTER

Foldover noise component outside the band is removed by the 8 times over-sampling FIR type digital filter. The construction and basic characteristic of the digital filter are changed by the standard and double speed operations.

● Standard operation



● Double speed operation

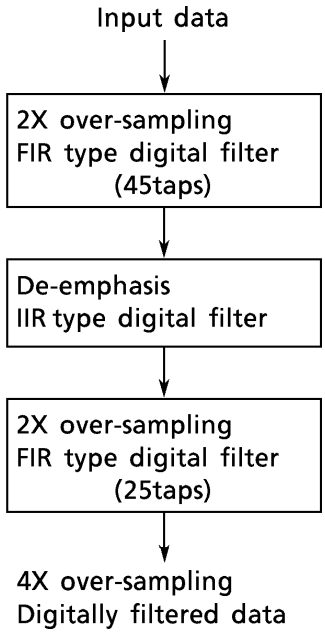


FIG.3 Construction of digital filter

Table-1 Basic characteristics of digital filter (fs = 44.1kHz)

MODE	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard operation	±0.003dB	20.0k~24.1kHz	−68dB
Double speed operation	±0.05dB	20.0k~24.1kHz	−40dB

Digital filter frequency characteristics

- Standard operation

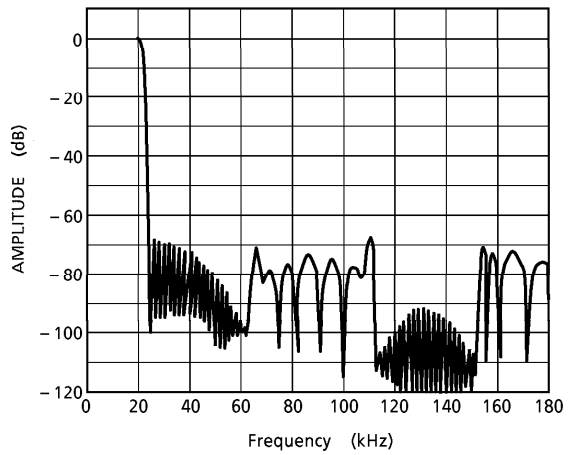


FIG4. Frequency characteristics (stop band)

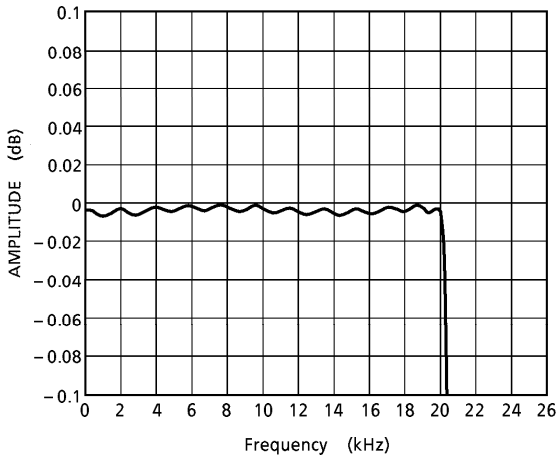


FIG5. Frequency characteristics (pass band)

- Double speed operation

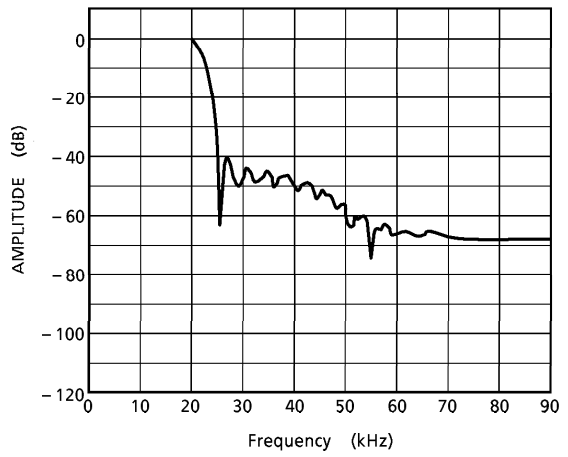


FIG6. Frequency characteristics (stop band)

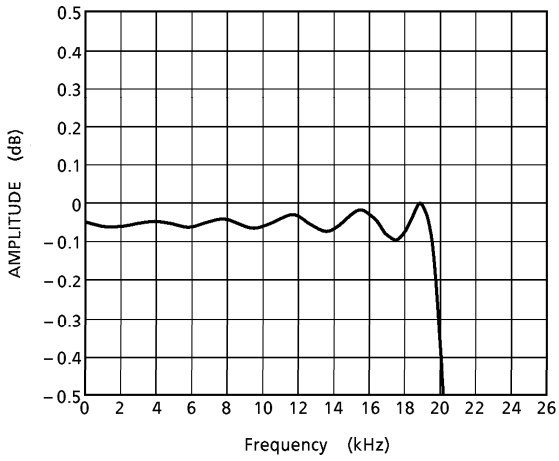


FIG7. Frequency characteristics (pass band)

The built-in digital de-emphasis circuit can be set to coup with sampling frequency of 32kHz, 44.1kHz, and 48kHz. The selection is done as shown in the following table.

Table.2 Truth table for de-emphasis filter selection

LATCH ($\overline{EM1}$)	H	H	L	L	
SHIFT ($\overline{EM2}$)	H	L	H	L	
MODE (fs SELECT)	44.1	OFF	48	32	(kHz)

Since the de-emphasis filter is a digital circuit, resistors, capacitors, and analog switches are not requided. Filter construction is shown below.

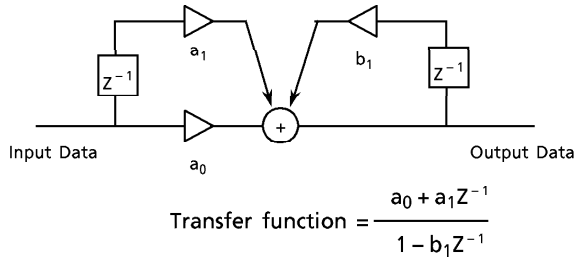


FIG.8 Digital De-emphasis filter construction

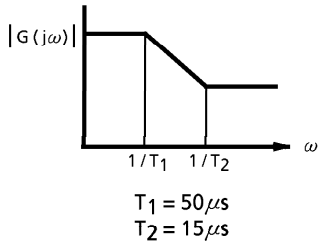


FIG.9 Filter Characteristics

4. INTERPOLATION FILTER AND DITHER CIRCUIT

The interpolation filter linearly interpolates 8 fs after the digital filter and over to 16fs in the dither circuit, DC offset and dither have been added to Data in order to areven noise by the idling pattern peculiar to Σ-Δ Modulation DAC. After adding the dither 384fs is over sampled in sample and hold circuit.

5. DA CONVERSION CIRCUIT

2 times Σ-Δ modulation DA converter for 2 channels (simultaneous output type) is incorporated in the TC9270F / N. The internal circuit construction is as shown in fig.10.
The conversion time for the bitstream output is 1 / 384fs. (in 384fs mode)
In case if CD application, fs = 44.1kHz
conversion time

Tset = (1 / 384 × 44.1kHz) = 59.05ns

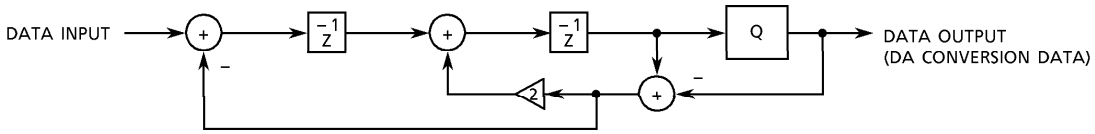


FIG.10 Σ-Δ Modulation circuit

6. The Σ-Δ modulation section is designed to operate at same frequency as the master clock in both standard and double speed operation.

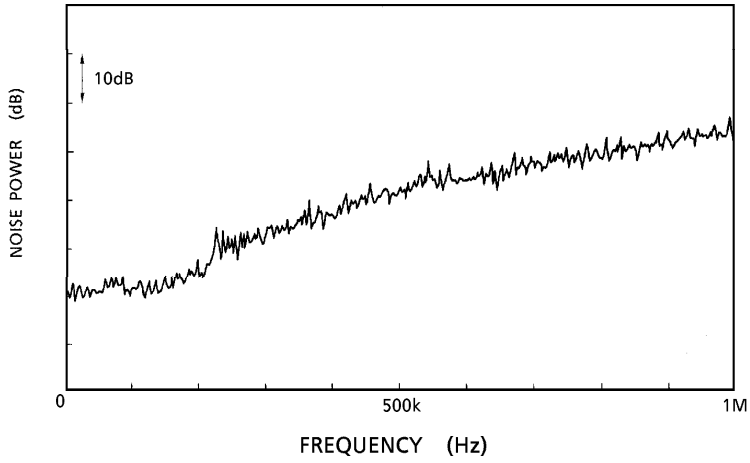


FIG.11 Noise shaping characteristics

7. DATA OUTPUT CIRCUIT

In the data output circuit, the 384fs or 256fs data are added to the data shift by rising and falling edge of clock. By differentiating these forward signal and the reverse signal in the external analog circuit, DA conversion of Low distortion factor high S/N ratio be obtained.

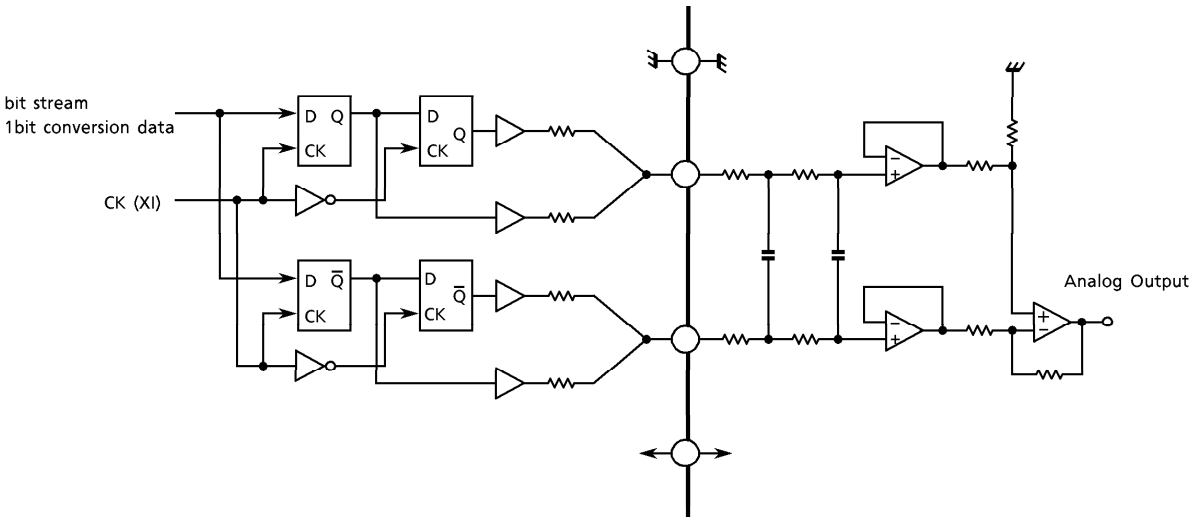


FIG.12 Data output circuit

8. INTERNAL CONTROL SIGNAL EXPLANATION

Parallel and serial control mode can be selected by the P/$\overline{S}$ terminal. The controll functions are example as follow.

8-1 PARALLEL CONTROL MODE (P/$\overline{S}$ PIN = H)

In parallel control mode, Pin 20, 21, 22 are set as follow.

Table-3 Terminal name at parallel mode

PIN No.	PIN NAME	FUNCTION
20	$\overline{EM1}$	De-emphasis control signal 1
21	$\overline{EM2}$	De-emphasis control signal 2
22	MUTE	If set to "H", digital mute for output is ON.

8-2 SERIAL CONTROL MODE (P/$\overline{S}$ = L : FOR MICRO PROCESSOR CONTROL USE)

In serial control mode, the TC9270F/N can be controlled by micro processor. The control function of Pin 20, 21, 22 are as

Table-4 Terminal name at serial mode

PIN No.	PIN NAME	FUNCTION
20	LATCH	Data latch for input signal.
21	SHIFT	Shift clock signal input terminal
22	ATT	Att data input terminal

Latch and att signal are entered to the shift register of the LSI at the rising edge of the shift signal.
Also, the latch signal should rise after a minimum of 1.5μs of the last data is shifted to the register.
If the shift pulse is changed while catch is Low, Mis-operation may occur. Latch should be keep at Low until after D7 is shifted into the register.

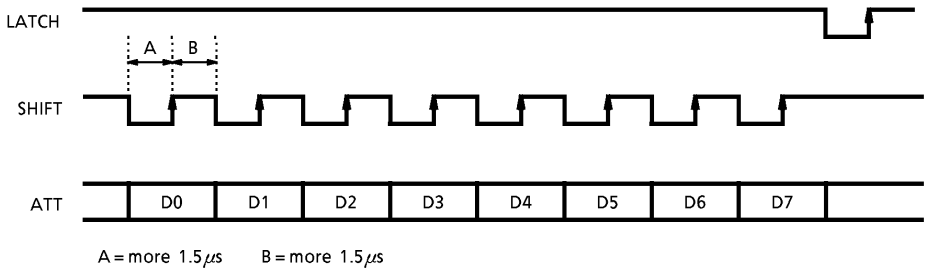


FIG.13 Example for serial control mode data

In serial control mode, the control features are as follow.

Table-5 Serial mode control

SERIAL INPUT DATA	CONTROL SIGNAL		
D7	0	1	
D6	AT6	0	1
D5	AT5	EMP	—
D4	AT4	CHS	MODE
D3	AT3	MONO	—
D2	AT2	HS	—
D1	AT1	μEM2	BIT2
D0	AT0	μEM1	BIT1

AT0~6 : Attenuation level setting
μEM1、2 : De-emphasis option set
HS : Double speed mode setting
BIT1、2 : Input data bit select
MONO : Stereo / Mono setting
CHS : Mono mode L / R mode
EMP : De-emphasis ON / OF
MODE : Digital filter fs selection

① Digital attenuator

D7 = L is the command for digital attenuator. If can be set to 28 levels as show below.

Table-6 Audio output of attenuation DATA

ATTENUATION CONTROL DATA D6~D0	AUDIO OUTPUT
7F (HEX)	0dB
7E (HEX)	– 0.069dB
⋮	⋮
01 (HEX)	– 42.076dB
00 (HEX)	– ∞

The attenuation value can be calculated from input data as follow :

ATT = 20ℓog (input data / 127)dB

Example : In case of attenuator = 7A

ATT = 20ℓog (122 / 127)dB = – 0.349dB

Digital attention change from 0dB to – ∞ with a slope of 1024s / f

② MONO, CHS

1) MONO is the commend for switching bit stereo and mono mode.
"H"- MONO "L"- STEREO

2) CHS selects the left or right channel in MONO mode.
"H"- R channel "L"- Left channel

(Note) : In parallel mode, both MONO and CHS are set to "L" an correspond to stereo mode.

Table-7 Mono, CHS control feature

MONO	CHS	CONTROL FEATURE
L	L	Stereo mode
L	H	
H	L	mono Left channel
H	H	mono Right channel

③ MODE、EMP、μEM1、μEM2

These control the fs selection and coefficient selection for De-emphasis filter.

Table-8 De-emphasis filter and digital filter coefficient setting

MODE	EMP	μEM1	μEM2	DIG. FILTER COEFFICIENT	DE-EMPHASIS COEFFICIENT
0	—	0	0	44.1 kHz	44.1 kHz
		0	1	44.1 kHz	OFF
		1	0	44.1 kHz	48 kHz
		1	1	44.1 kHz	32 kHz
1	0	0	0	44.1 kHz	OFF
		0	1	44.1 kHz	OFF
		1	0	48 kHz	OFF
		1	1	32 kHz	OFF
1	1	0	0	44.1 kHz	44.1 kHz
		0	1	44.1 kHz	OFF
		1	0	48 kHz	48 kHz
		1	1	32 kHz	32 kHz

④ HS

HS is for selecting normal speed mode and double speed mode.
"H" Double speed mode "L" - Normal In parallel mode it is fixed to "L" normal speed mode.

⑤ BIT1、BIT2

These are for selecting input data length.

Table-9 Input data length settings

BIT1	BIT2	INPUT DATA LENGTH
L	—	16
H	L	18
	H	20

9. ZERO DETECT FUNCTION

This device has a built-in input data digital zero detection function. If zero data is continued for over $(2^{15}/fs)_{sec}$ "LZ" and "RZ" Pin become "H".

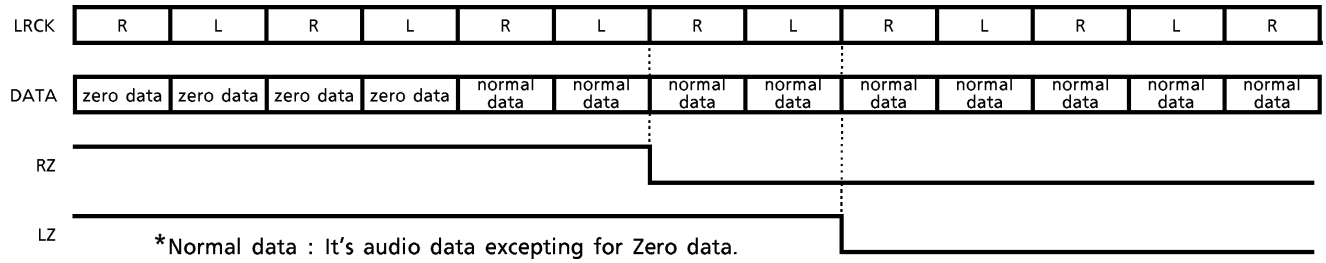


FIG.14 Zero detect cancel timing

10. RESET FUNCTION

The internal circuit can be reset by setting reset bit to "L".
In reset mode, outputs are as follow.
LO, $\overline{LO}$ both fixed at "L"
RO, $\overline{RO}$ both fixed at "H"
Output timing at reset is as follows.

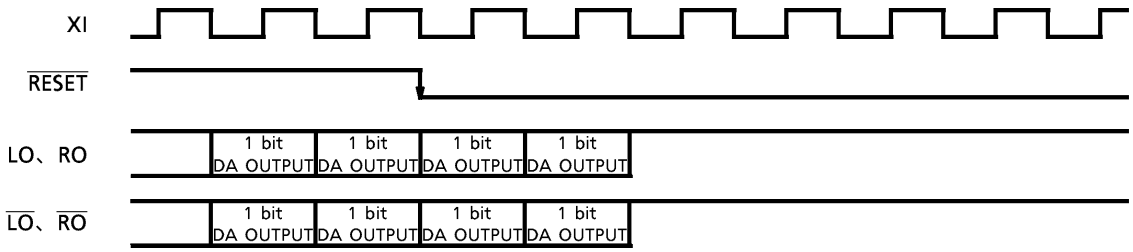


FIG.15 Reset and output relationship

The clock signal (XI input) is required for resetting internal circuit and output when setting reset to L.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~6.0	V
	V_{DA}	−0.3~6.0	V
	V_{DX}	−0.3~6.0	V
Input Voltage	V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	TC9270F : 600	mW
		TC9270N : 800	
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DA} = 5V$)

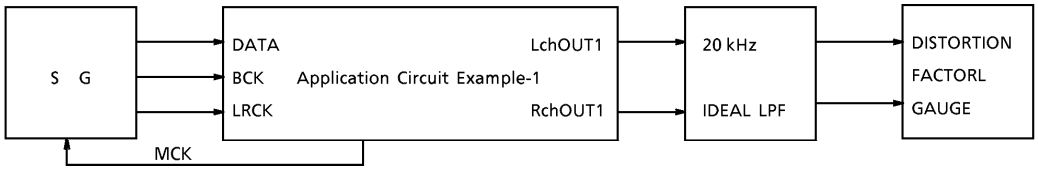
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Power Dissipation		I_{DD}	—	XI = 16.9MHz	—	30	40	mA
Input Voltage	"H"Level	V_{IH}	—		$V_{DD} \times 0.7$	—	V_{DD}	V
	"L"Level	V_{IL}			0.0	—	$V_{DD} \times 0.3$	
Input Current	"H"Level	I_{IH}	—		−1.0	—	1.0	μA
	"L"Level	I_{IL}						
Pull-up Resiso		RUP	—	1, 3, 17, 20, 21, 22, 23, Pin 24 Ta = 25°C, at 0V force measure current.	100	150	300	kΩ

AC CHARACTERISTICS (*) : Ta = 25°C

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Noise Distortion	(*)	THD + N	1	1kHz Sine wave, full-scale input	—	−90	−85	dB
S/N Ratio	(*)	S/N	1		95	100	—	dB
Dynamic Range	(*)	DR	1	1kHz Sine wave, −60 Input Conversion	90	95	—	dB
Cross-talk	(*)	CT	1	1kHz Sine wave, full-scale input	—	−95	−90	dB
Operating Frequency		f_{opr}	—		10	16.9344	19.2	MHz
Input Frequency		f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
		f_{BCK}		BCK duty cycle = 50%	0.96	1.4112	6.2	MHz
Rise Time		t_r	—	LRCK, BCK (10%~90%)	—	—	15	ns
Fall Time		t_f			—	—	15	ns
Delay Time		t_d	—	BCK ↓ Edge → LRCK, DATA	−50	—	50	ns

- **TEST CIRCUIT – 1** ; Application Circuit Example 1 is used.

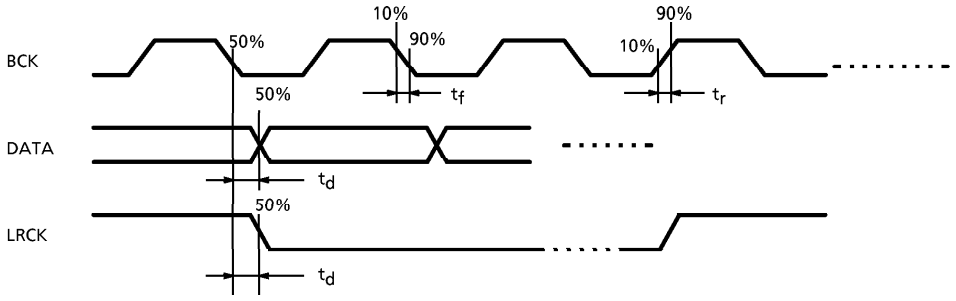


SG : ANRITSU MG-22A or equivalent
LPF : SHIBASOKU 725C Biult-In Filter
Distortion Factor Gauge : SHIBASOKU 725C or equivalent

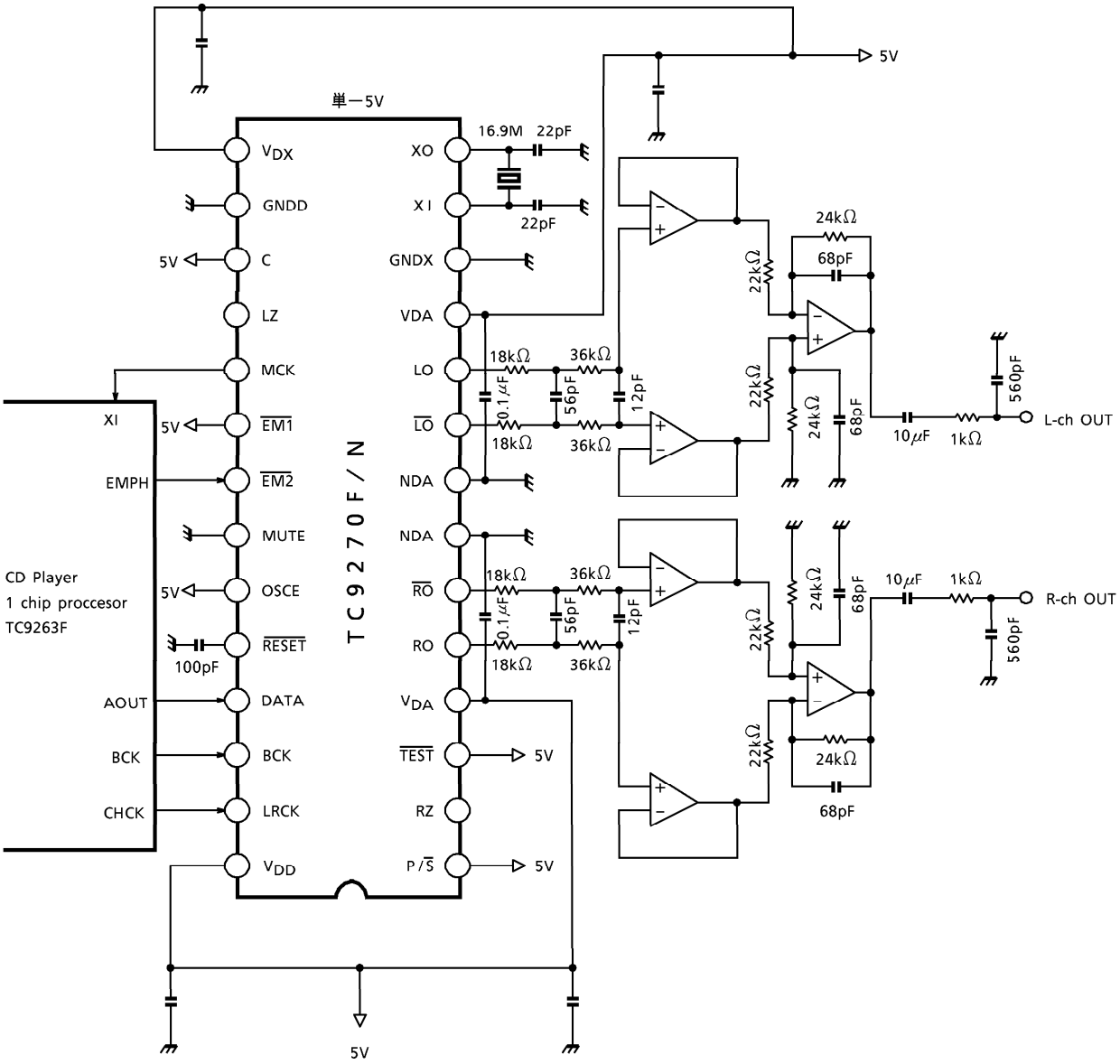
Measuring Item	Distortion factor gauge filter setting A weight
THD + N, CT	OFF
S / N, DR	ON

A weight : IEC - A or equivalent

- **AC CHARACTERISTIC POINT** ; (Input signal ; LRCK、BCK、DATA)

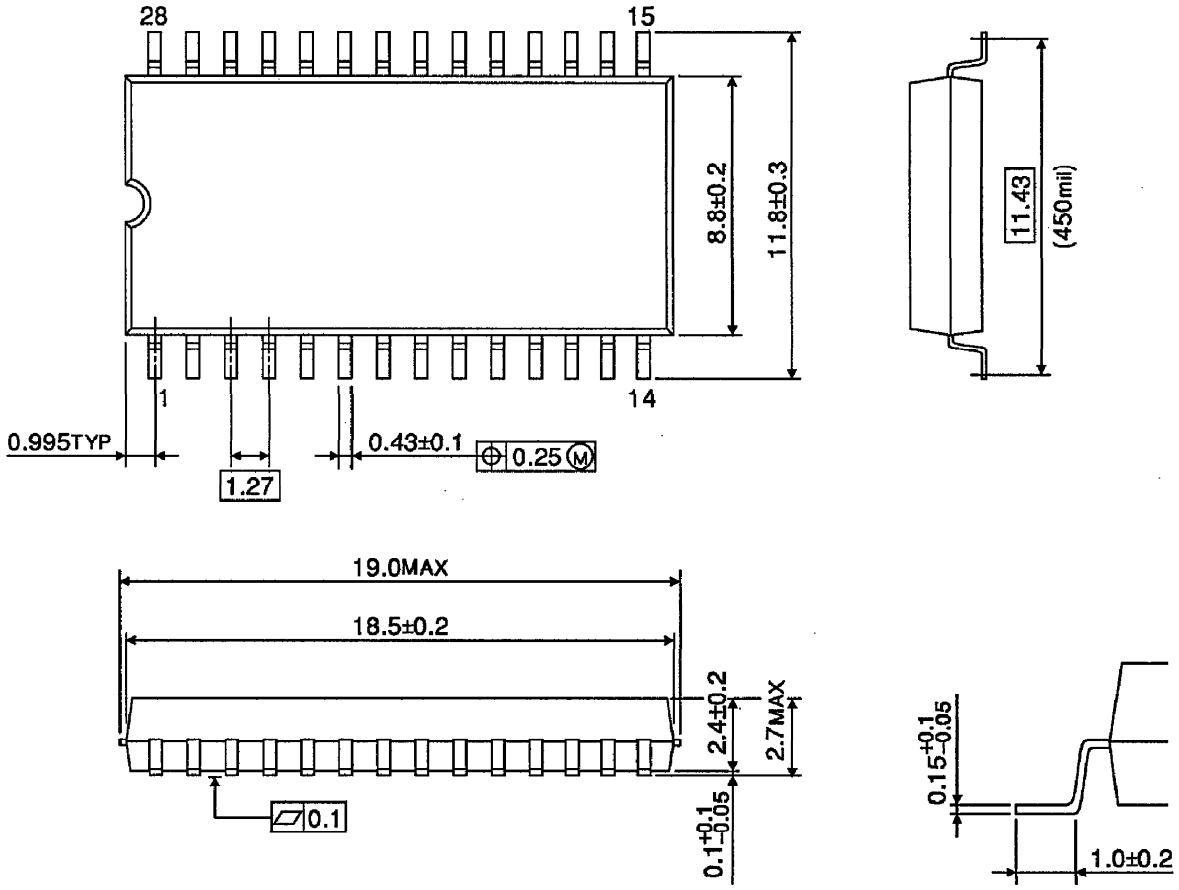


APPLICATION CIRCUIT



PACKAGE DIMENSIONS

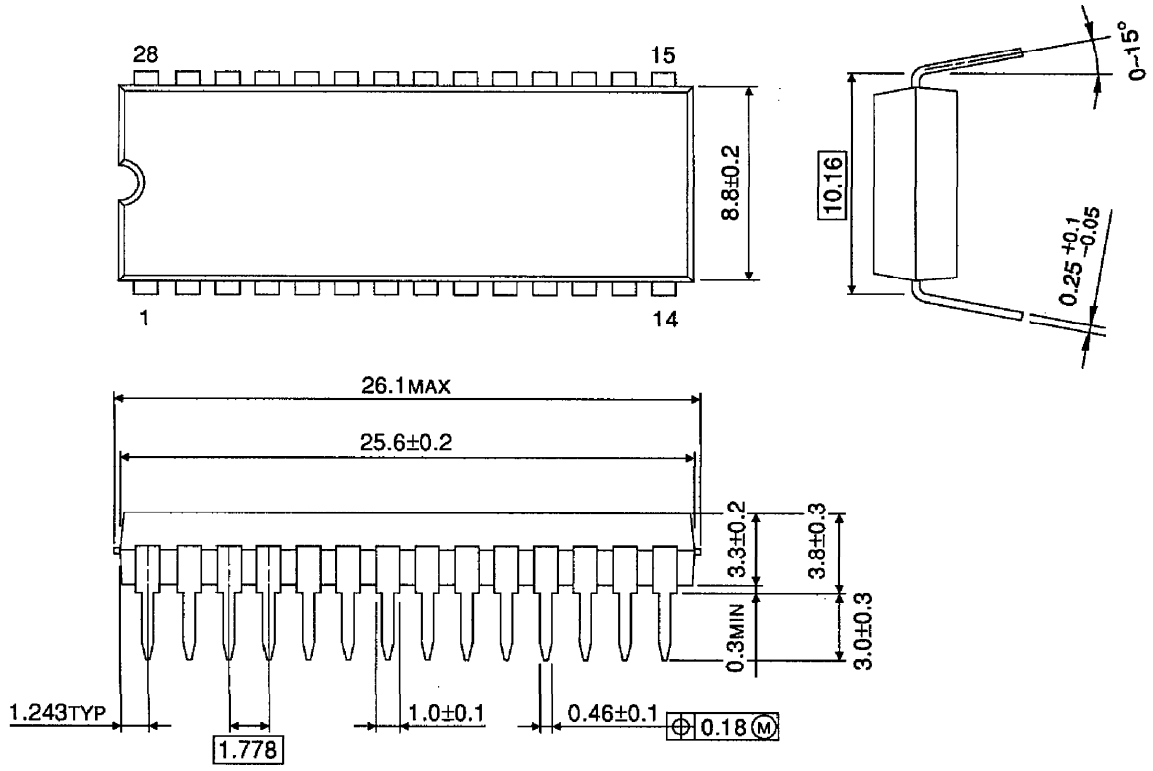
SOP28-P-450-1.27 Unit : mm



Weight : 0.8g (Typ.)

PACKAGE DIMENSIONS

SDIP28-P-400-1.78 Unit : mm



Weight : 2.2g (Typ.)

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000707EBA

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