

1:8 LVTTTL TO M-LVDS REPEATER DUAL 1:4 LVTTTL TO M-LVDS REPEATER

FEATURES

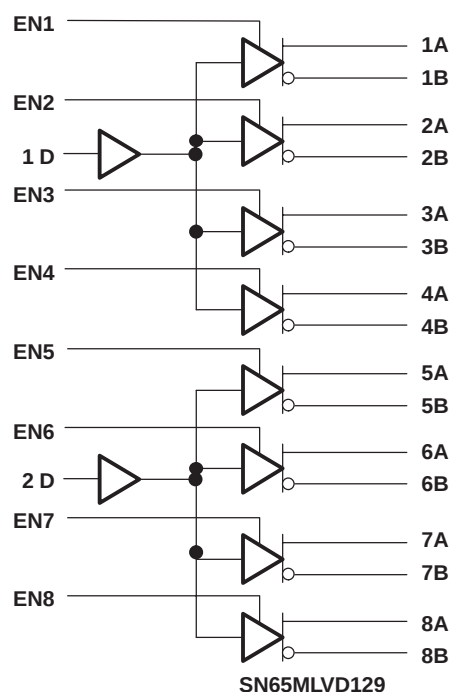
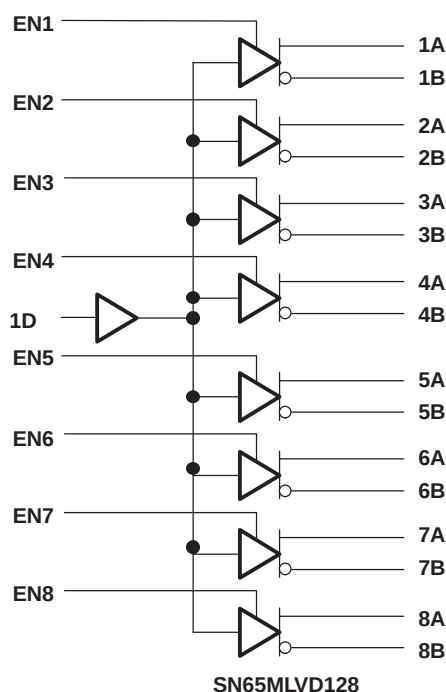
- LVTTTL Receiver and Eight Line Drivers Configured as an 8-Port M-LVDS Repeater – SN65MLVD128
- 2 LVTTTL Receivers and Eight Line Drivers Configured as Dual 4-Port M-LVDS Repeaters – SN65MLVD129
- Drivers Meet or Exceed the M-LVDS Standard (TIA/EIA-899)
- Low-Voltage Differential 30-Ω to 55-Ω Line Drivers for Data Rates⁽¹⁾ Up to 250 Mbps or Clock Frequencies Up to 125 MHz
- Power Up/Down Glitch Free
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5\text{ V}$

- Independent Enables for each Driver
- Output-to-Output Skew $t_{sk(o)} \leq 160\text{ ps}$
Part-to-Part Skew $t_{sk(pp)} \leq 800\text{ ps}$
- Single 3.3-V Voltage Supply
- Bus Pin ESD Protection Exceeds 9 kV
- Packaged in 48-Pin TSSOP (DGG)

APPLICATIONS

- AdvancedTCA™ (ATCA™) Clock Bus Driver
- Clock Distribution
- Data and Clock Repeating Over Backplanes and Cables
- Cellular Base Stations
- Central Office Switches
- Network Switches and Routers

LOGIC DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

⁽¹⁾The data rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The SN65MLVD128 and SN65MLVD129 are LVTTTL-to-M-LVDS translators/repeaters. Outputs comply with the M-LVDS standard (TIA/EIA-899) and are optimized for data rates up to 250 Mbps, and clock frequencies up to 125 MHz. The driver outputs have been designed to support multipoint buses presenting loads as low as 30 Ω and incorporates controlled transition times for backbone operation.

M-LVDS compliant devices allow for 32 nodes on a common bus, providing a high-speed replacement for RS-485 devices when lower common-mode voltage range and lower output signaling levels are acceptable. The SN65MLVD128 and SN65MLVD129 provide separate driver enables, allowing for independent control of each output signal.

Intended applications for these devices include transmission of clock signals from a central clock module, as well as translation and buffering of data or control signals for transmission through a controlled impedance backplane or cable.

ORDERING INFORMATION

PART NUMBER	INPUT:OUTPUT CHANNEL	PART MARKING	PACKAGE/CARRIER
SN65MLVD128DGG	1:8	MLVD128	48-Pin TSSOP/Tube
SM65MLVD128DGGR	1:8	MLVD128	48-Pin TSSOP/Tape and Reeled
SN65MLVD129DGG	Dual 1:4	MLVD129	48-Pin TSSOP/Tube
SM65MLVD129DGGR	Dual 1:4	MLVD129	48-Pin TSSOP/Tape and Reeled

PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
48-DGG	Low-K ⁽²⁾	1114.6 mW	9.7 mW/ $^\circ\text{C}$	533.1 mW
48-DGG	High-K ⁽³⁾	1824.5 mW	15.9 mW/ $^\circ\text{C}$	872.6 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			SN65MLVD128, 129
Supply voltage range ⁽²⁾ , V_{CC}			-0.5 V to 4 V
Input voltage range, V_I	D, EN		-0.5 V to 4 V
Output voltage range, V_O	A or B		-1.8 V to 4 V
Electrostatic discharge	Human Body Model ⁽³⁾	A, B	± 9 kV
		All pins	± 4 kV
	Charged-Device Model ⁽⁴⁾	All pins	± 1500 V
	Machine Model ⁽⁵⁾	All pins	200 V
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.

(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.8	V
Voltage at any bus terminal (separate or common mode) V_A or V_B	-1.4		3.8	V
Differential load resistance, R_L	30		55	Ω
Signaling rate, $1/t_{UI}$			250	Mbps
Clock frequency			125	MHz
Ambient temperature, T_A	-40		85	$^{\circ}\text{C}$

(1) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT	
I _{CC}	Supply current	Driver enabled	EN = V _{CC} , Input = V _{CC} or GND, R _L = 50 Ω		112	140	mA
			EN = V _{CC} , Input = V _{CC} or GND, R _L = No load			45	mA
	Driver disabled	EN = V _{CC} , Input = V _{CC} or GND, R _L = 50 Ω			7	mA	
		EN = V _{CC} , Input = V _{CC} or GND, R _L = No load			7	mA	
Device power dissipation, P _D		V _{CC} = 3.6 V, EN = V _{CC} , C _L = 15 pF, R _L = 50 Ω, Input 125 MHz 50 % duty cycle square wave, T _A = 85°C				529	mW

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
LVTTL (D, EN) INPUT SPECIFICATIONS						
$ I_{IH} $	High-level input current	$V_{IH} = 2\text{ V or }V_{CC}$			10	μA
$ I_{IL} $	Low-level input current	$V_{IL} = \text{GND or }0.8\text{ V}$			10	μA
C_i	Input capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5\text{ V}^{(3)}$		5		pF
M-LVDS (A, B) OUTPUT SPECIFICATIONS						
$ V_{AB} $	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta V_{AB} $	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		$-0.2V_{SS}$			V
$ I_{OS} $	Differential short-circuit output current magnitude	See Figure 4			24	mA
I_{OZ}	High-impedance state output current	$-1.4\text{ V} \leq (V_A \text{ or } V_B) \leq 3.8\text{ V}$, Other output = 1.2 V	-20		20	μA
$I_{O(OFF)}$	Power-off output current	$-1.4\text{ V} \leq (V_A \text{ or } V_B) \leq 3.8\text{ V}$, Other output = 1.2 V, $0 \leq V_{CC} \leq 1.5\text{ V}$	-20		20	μA
$C_A \text{ or } C_B$	Output capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5\text{ V}$, ⁽³⁾ Other input at 1.2 V, driver disabled		3		pF
C_{AB}	Differential output capacitance	$V_I = 0.4 \sin(30E6\pi t)\text{ V}$, ⁽³⁾ Driver disabled			2.5	pF
$C_{A/B}$	Output capacitance balance, (C_A/C_B)		0.99		1.01	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	See Figure 5	1		3	ns
t_{pHL}	Propagation delay time, high-to-low-level output		1		3	ns
t_r	Differential output signal rise time		1		2	ns
t_f	Differential output signal fall time		1		2	ns
$t_{sk(p)}$	Pulse skew ($ t_{pHL} - t_{pLH} $)				100	ps
$t_{sk(o)}$	Output skew				160	ps
$t_{sk(bb)}$	Bank-to-bank skew(2)				100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				800	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	100 MHz clock input, All channels enabled		1	3	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter(4)	100 MHz clock input, All channels enabled			20	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	200 Mbps 2 ¹⁵ -1 PRBS input, All channels enabled		46	110	ps
t_{pZH}	Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
t_{pZL}	Enable time, high-impedance-to-low-level output				7	ns
t_{pHZ}	Disable time, high-level-to-high-impedance output	See Figure 6			7	ns
t_{pLZ}	Disable time, low-level-to-high-impedance output				7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) $t_{sk(bb)}$, which only applies to the SN65MLVD129, is the magnitude of the difference between the t_{pLH} and t_{pHL} of two outputs of any bank.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Stimulus jitter has been subtracted from the numbers.

PARAMETER MEASUREMENT INFORMATION

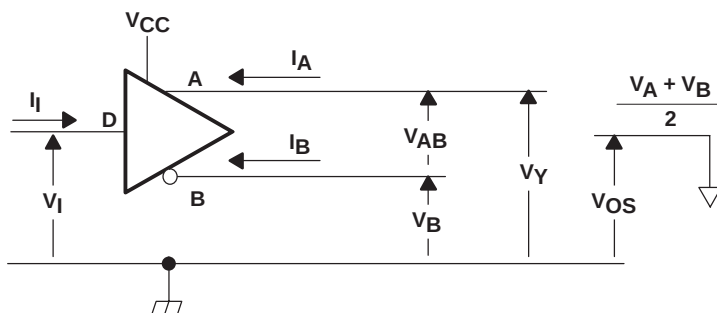
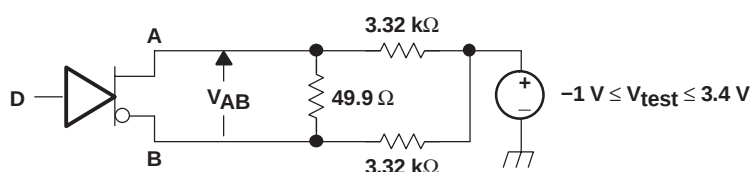
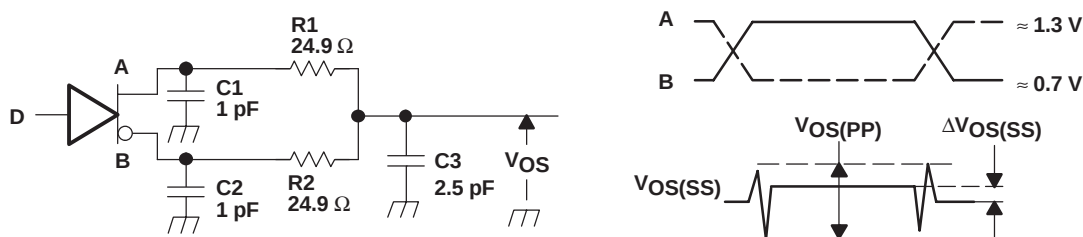


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.

B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.

C. R1 and R2 are metal film, surface mount, $\pm 1\%$, and located within 2 cm of the D.U.T.

D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

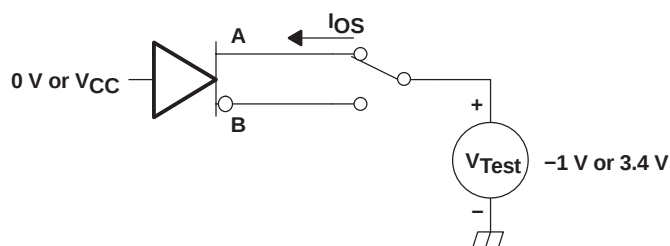
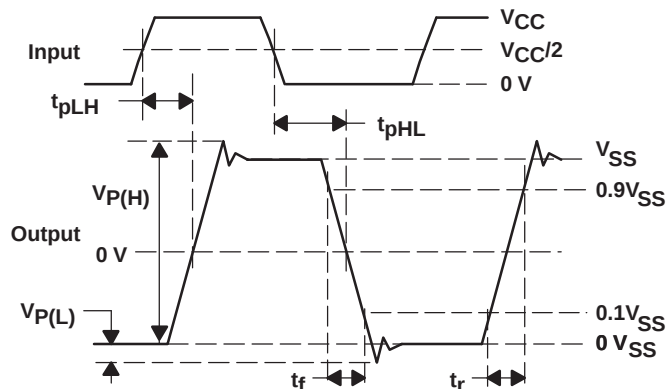
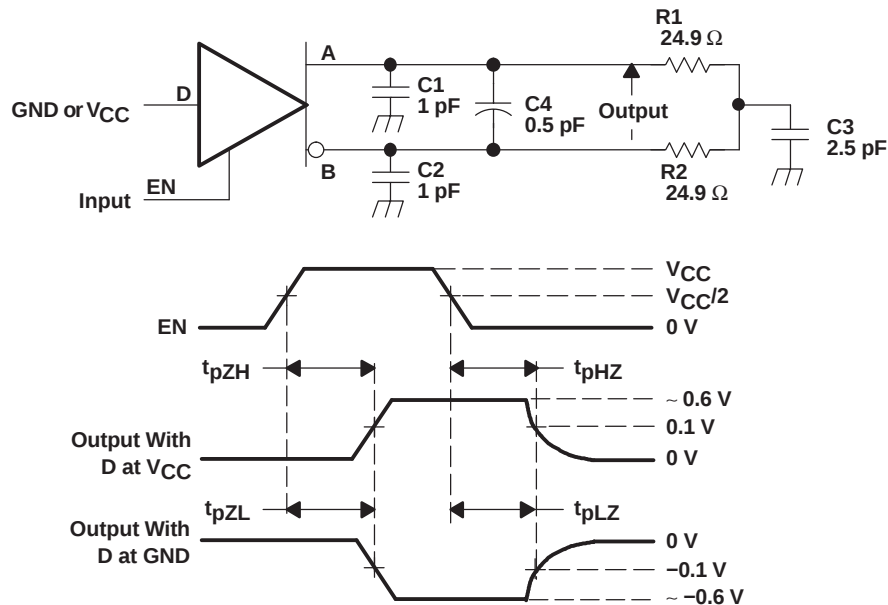


Figure 4. Driver Short-Circuit Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.

B. C1, C2, C3, and C4 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are $\pm 20\%$.

C. R1 and R2 are metal film, surface mount, $\pm 1\%$, and located within 2 cm of the D.U.T.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

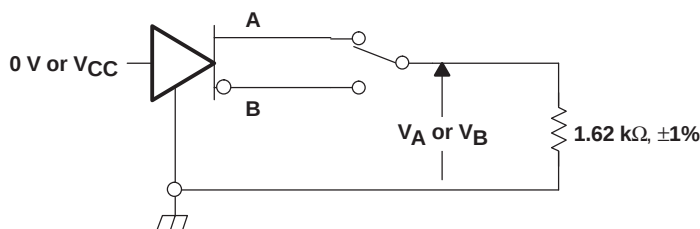
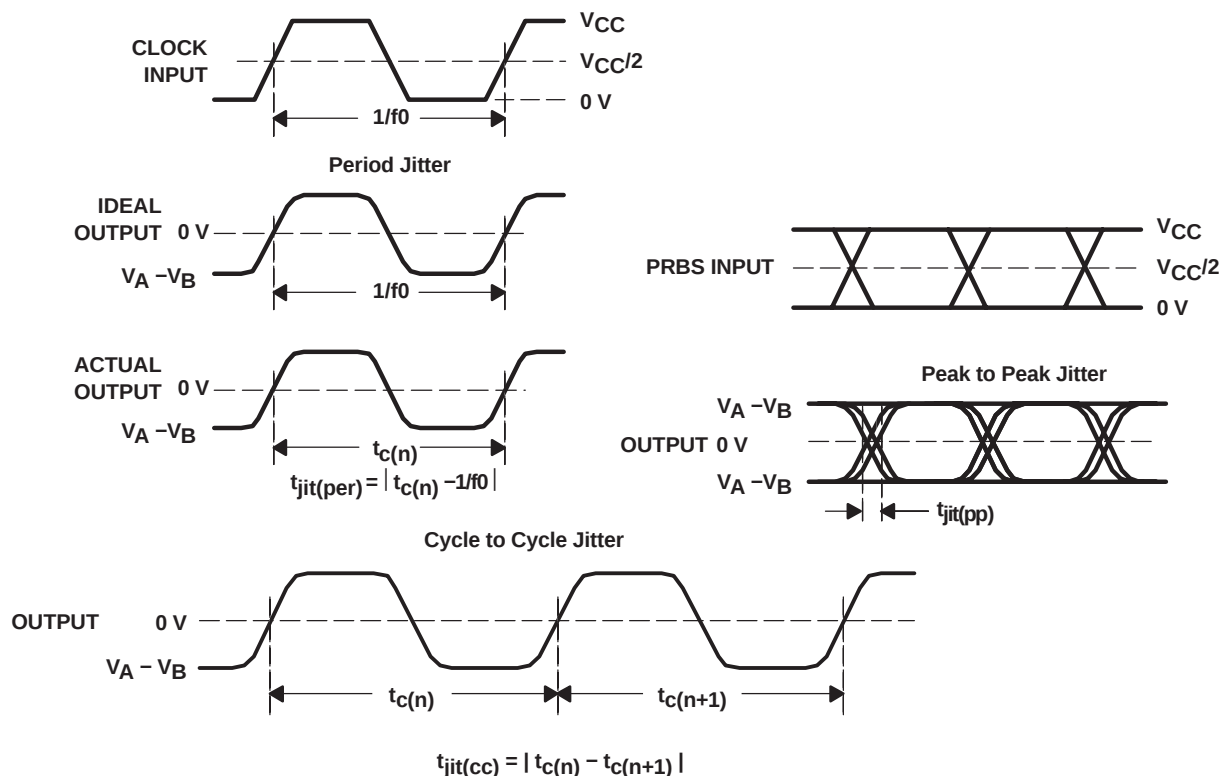


Figure 7. Driver Maximum Steady State Output Voltage



NOTES:D. All input pulses are supplied by an Agilent 8304A Stimulus System.

E. The measurement is made on a TEK TDS6604 running TDSJIT3 application software

F. Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 $\pm$ 1% duty cycle clock input.

G. Peak-to-peak jitter is measured using a 200 Mbps 2¹⁵-1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

Terminal Functions – SN65MLVD128

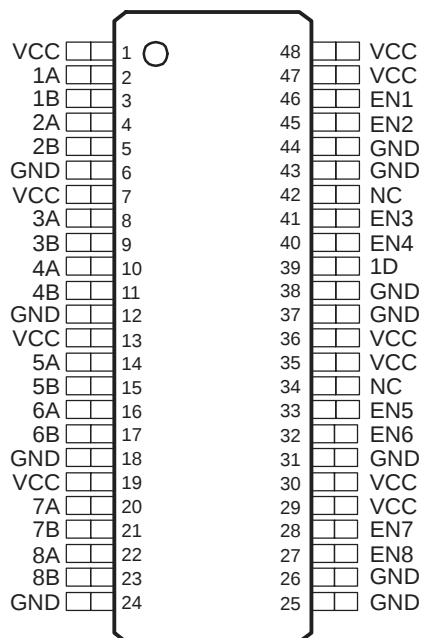
PIN		TYPE	DESCRIPTION
NAME	NO.		
1D	39	Input	Data inputs for drivers
EN1 – EN8	27, 28, 32, 33, 40, 41, 45, 46	Input	Driver enable, active high, individual enables
1A – 8A	2, 4, 8, 10, 14, 16, 20, 22	Output	M-LVDS bus noninverting output
1B – 8B	3, 5, 9, 11, 15, 17, 21, 23	Output	M-LVDS bus inverting output
GND	6, 12, 18, 24, 25, 26, 31, 37, 38, 43, 44	Power	Circuit ground
VCC	1, 7, 13, 19, 29, 30, 35, 36, 47, 48	Power	Supply voltage
NC	34, 42	N/A	Not connected

Terminal Functions – SN65MLVD129

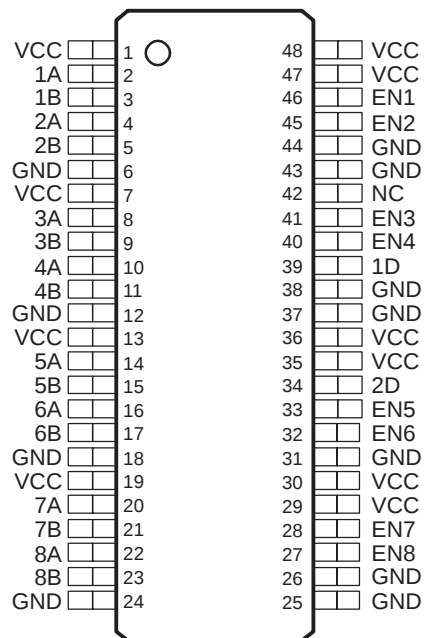
PIN		TYPE	DESCRIPTION
NAME	NO.		
1D, 2D	39, 34	Input	Data inputs for drivers
EN1 – EN8	27, 28, 32, 33, 40, 41, 45, 46	Input	Driver enable, active high, individual enables
1A – 8A	2, 4, 8, 10, 14, 16, 20, 22	Output	M-LVDS bus noninverting output
1B – 8B	3, 5, 9, 11, 15, 17, 21, 23	Output	M-LVDS bus inverting output
GND	6, 12, 18, 24, 25, 26, 31, 37, 38, 43, 44	Power	Circuit ground
V _{CC}	1, 7, 13, 19, 29, 30, 35, 36, 47, 48	Power	Supply voltage
NC	42	N/A	Not connected

PIN ASSIGNMENTS

MLVD128DGG
48-TSSOP PACKAGE
(TOP VIEW)



MLVD129DGG
48-TSSOP PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

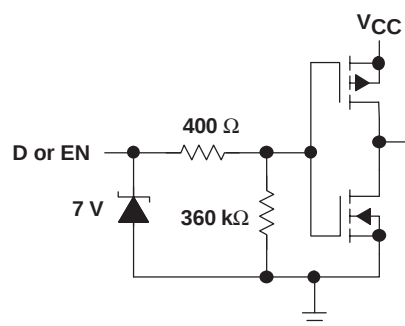
MLVD128/MLVD129

INPUT	ENABLE	OUTPUTS	
		A	B
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

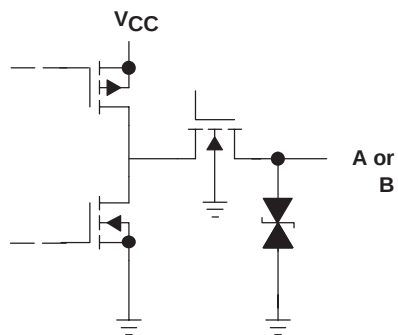
H = high level, L = low level, Z = high impedance, X = Don't care, OPEN = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

DRIVER INPUT AND DRIVER ENABLE



DRIVER OUTPUT



TYPICAL CHARACTERISTICS

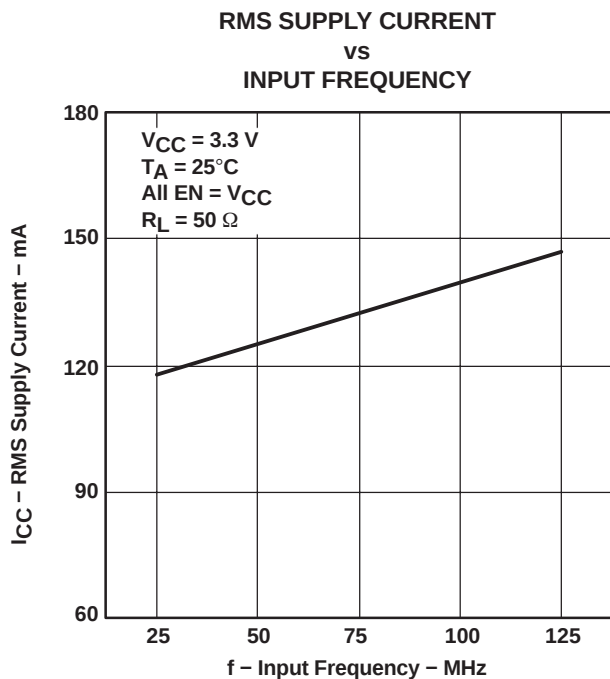


Figure 9

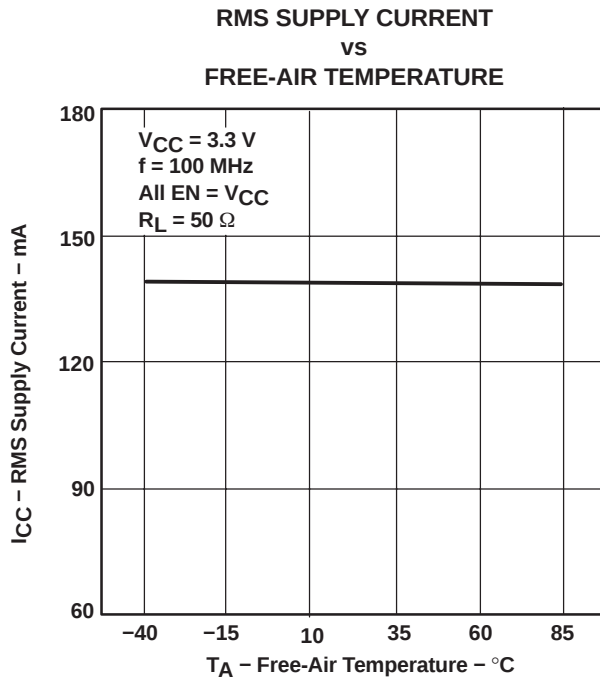


Figure 10

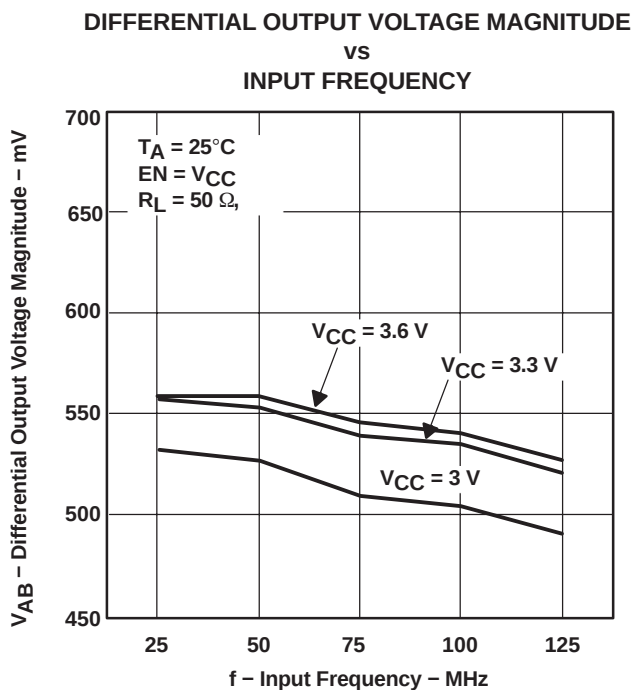


Figure 11

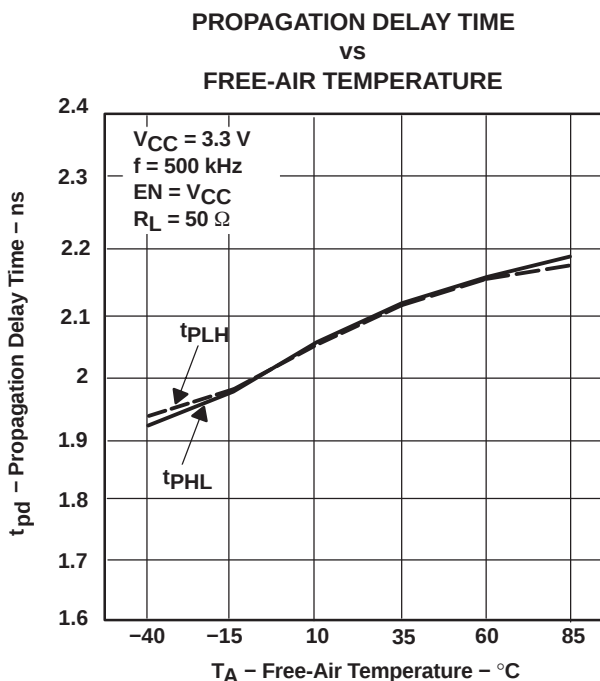


Figure 12

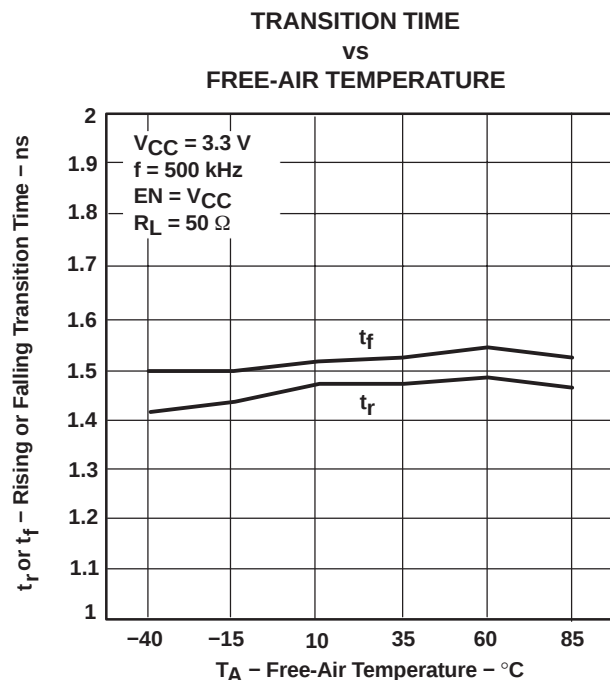


Figure 13

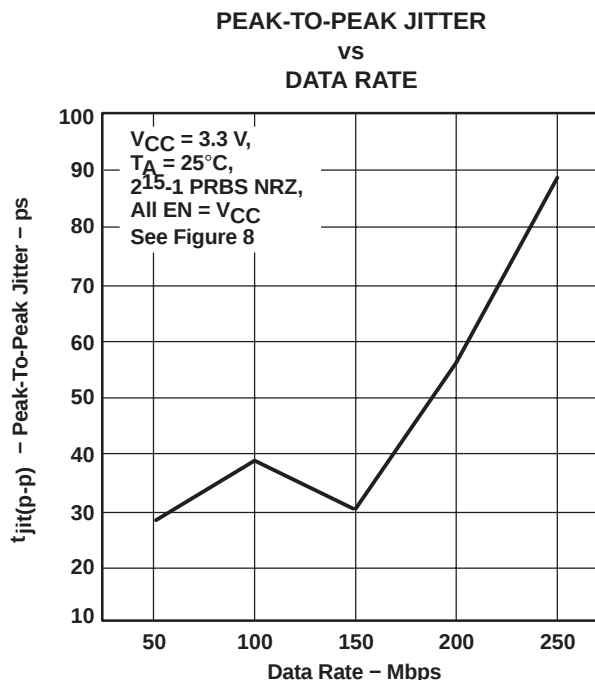


Figure 14

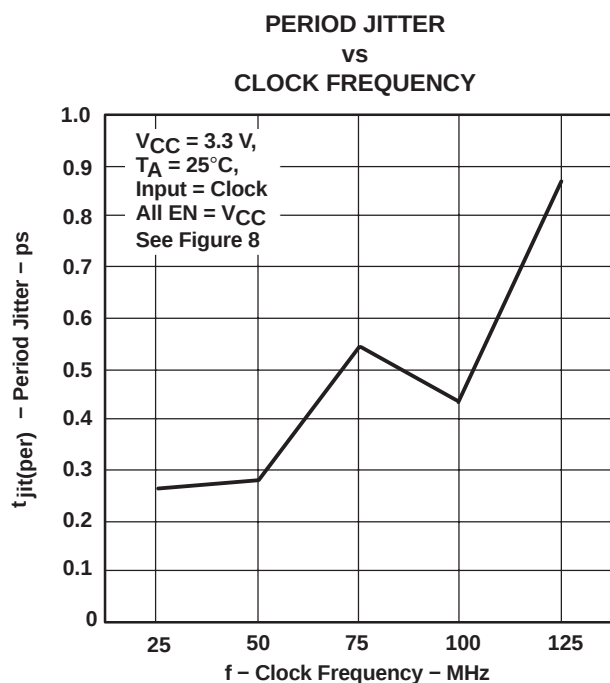


Figure 15

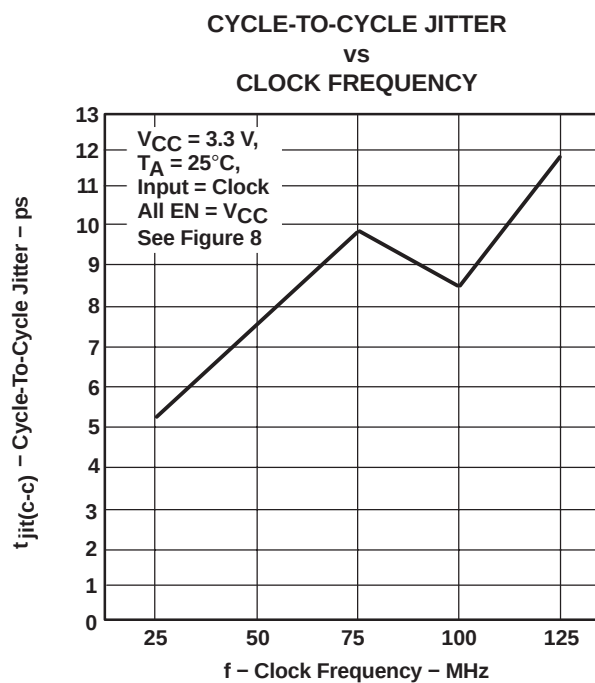
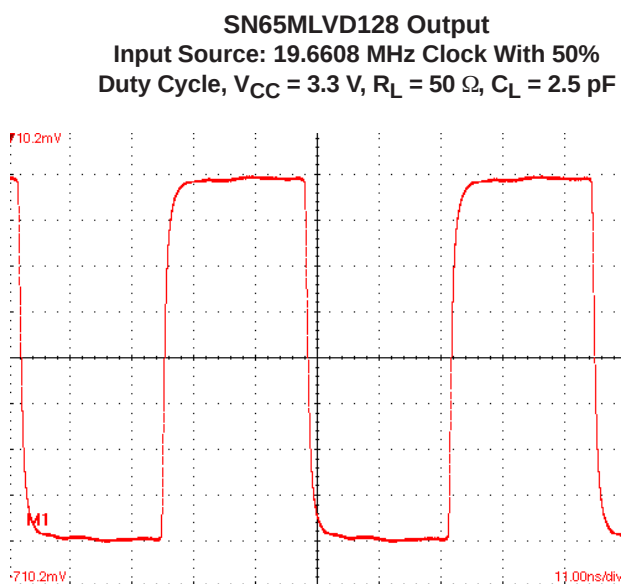


Figure 16

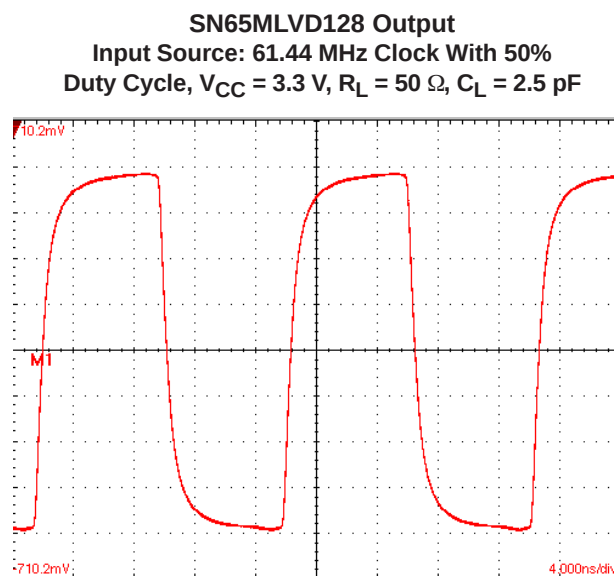
APPLICATION INFORMATION

CLOCK DISTRIBUTION



Output Duty cycle = 49.97%.
Vertical scale = 142 mV/div
Horizontal scale = 11 ns/div

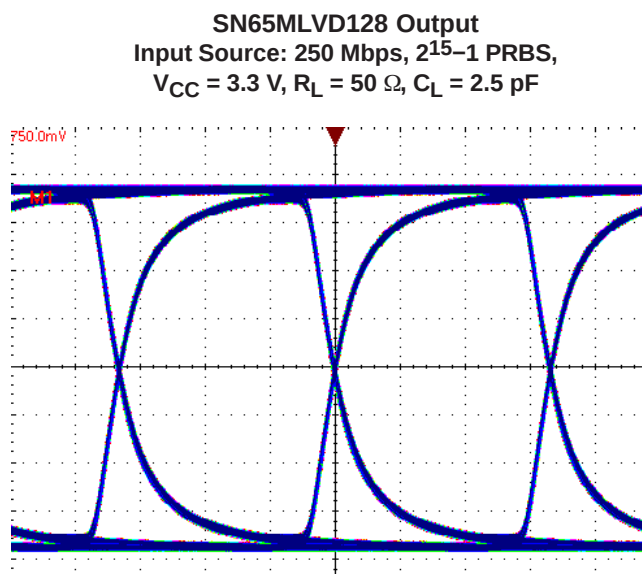
Figure 17



Output duty cycle = 50.01%.
Vertical scale = 142 mV/div
Horizontal scale = 4 ns/div

Figure 18

DATA DISTRIBUTION



Vertical scale = 150 mV/div
Horizontal scale = 1.21 ns/div

Figure 19

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65MLVD128DGG	ACTIVE	TSSOP	DGG	48	40	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65MLVD128DGGR	ACTIVE	TSSOP	DGG	48	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65MLVD129DGG	ACTIVE	TSSOP	DGG	48	40	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65MLVD129DGGR	ACTIVE	TSSOP	DGG	48	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

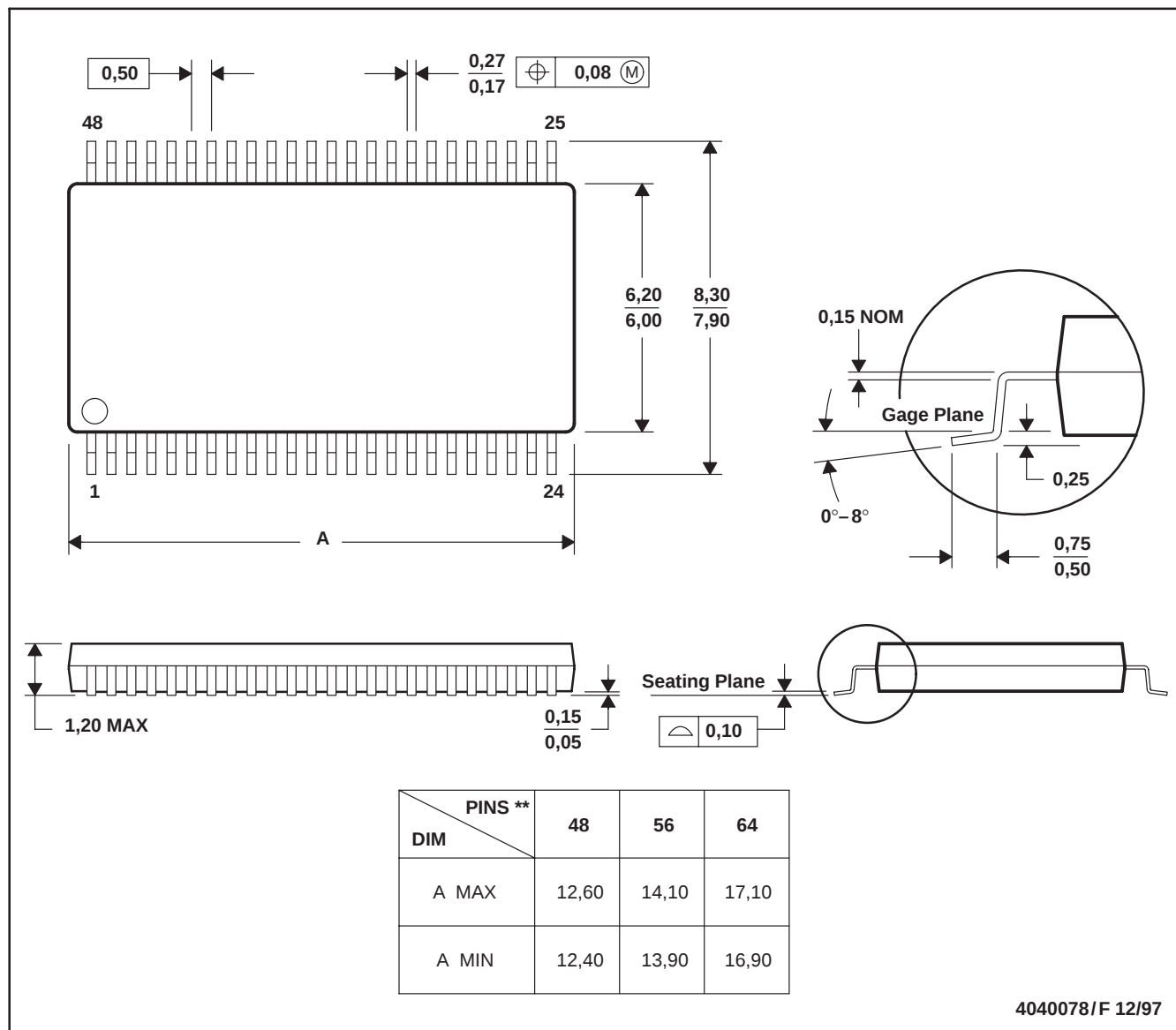
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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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