

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74AC161P, TC74AC161F, TC74AC161FN, TC74AC161FT

TC74AC163P, TC74AC163F, TC74AC163FN, TC74AC163FT

SYNCHRONOUS PRESETTABLE 4 – BIT BINARY COUNTER

TC74AC161P/F/FN/FT ASYNCHRONOUS CLEAR

TC74AC163P/F/FN/FT SYNCHRONOUS CLEAR

The TC74AC161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate and double - layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ inputs are active on low logic level.

Presetting of these IC's is synchronous to the rising edge of CK.

The clear function of the TC74AC163 is synchronous to CK, while the TC74AC161 are cleared asynchronously.

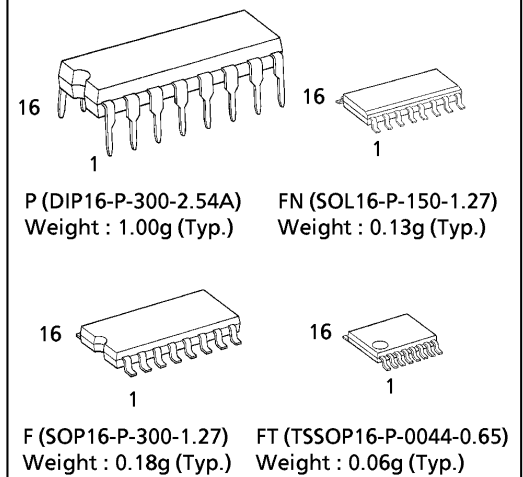
Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n - bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

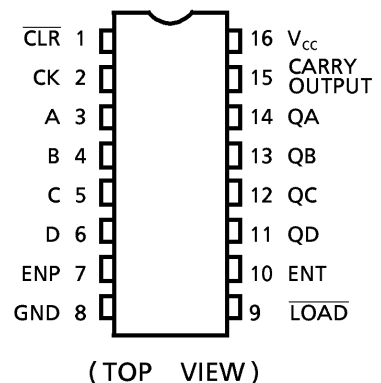
FEATURES:

- High Speed..... $f_{\text{MAX}} = 170\text{MHz}(\text{typ.})$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{\text{OH}}| = |I_{\text{OL}}| = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F161/163

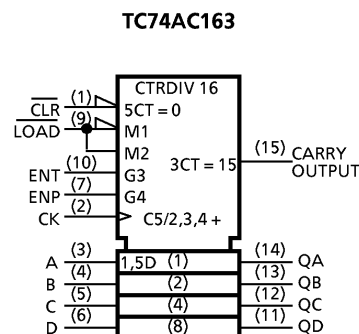
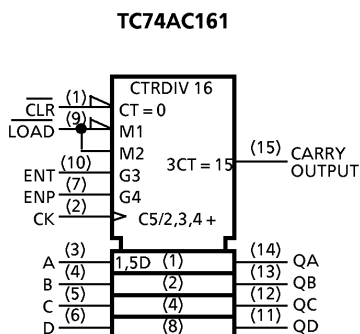
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL

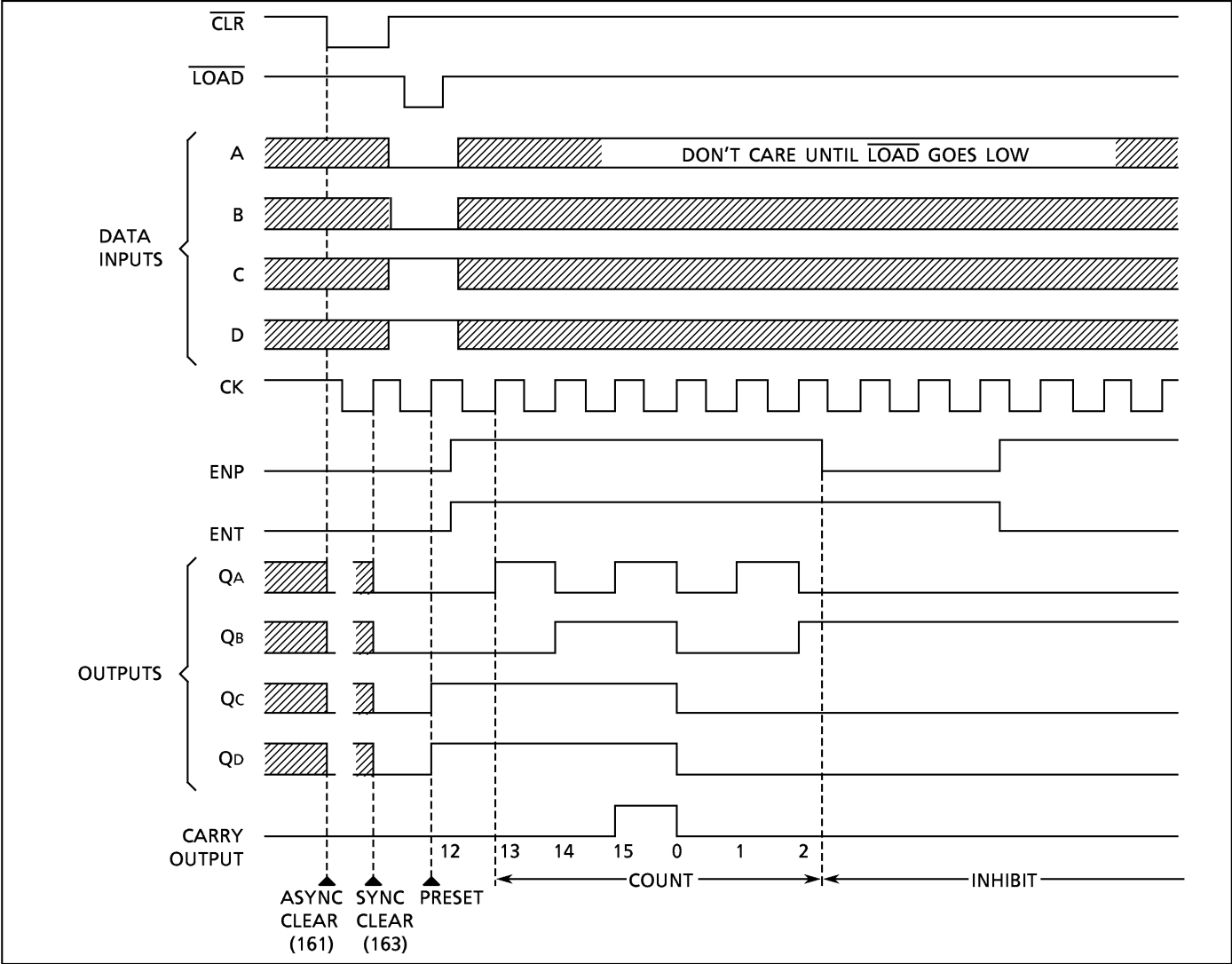


TRUTH TABLE

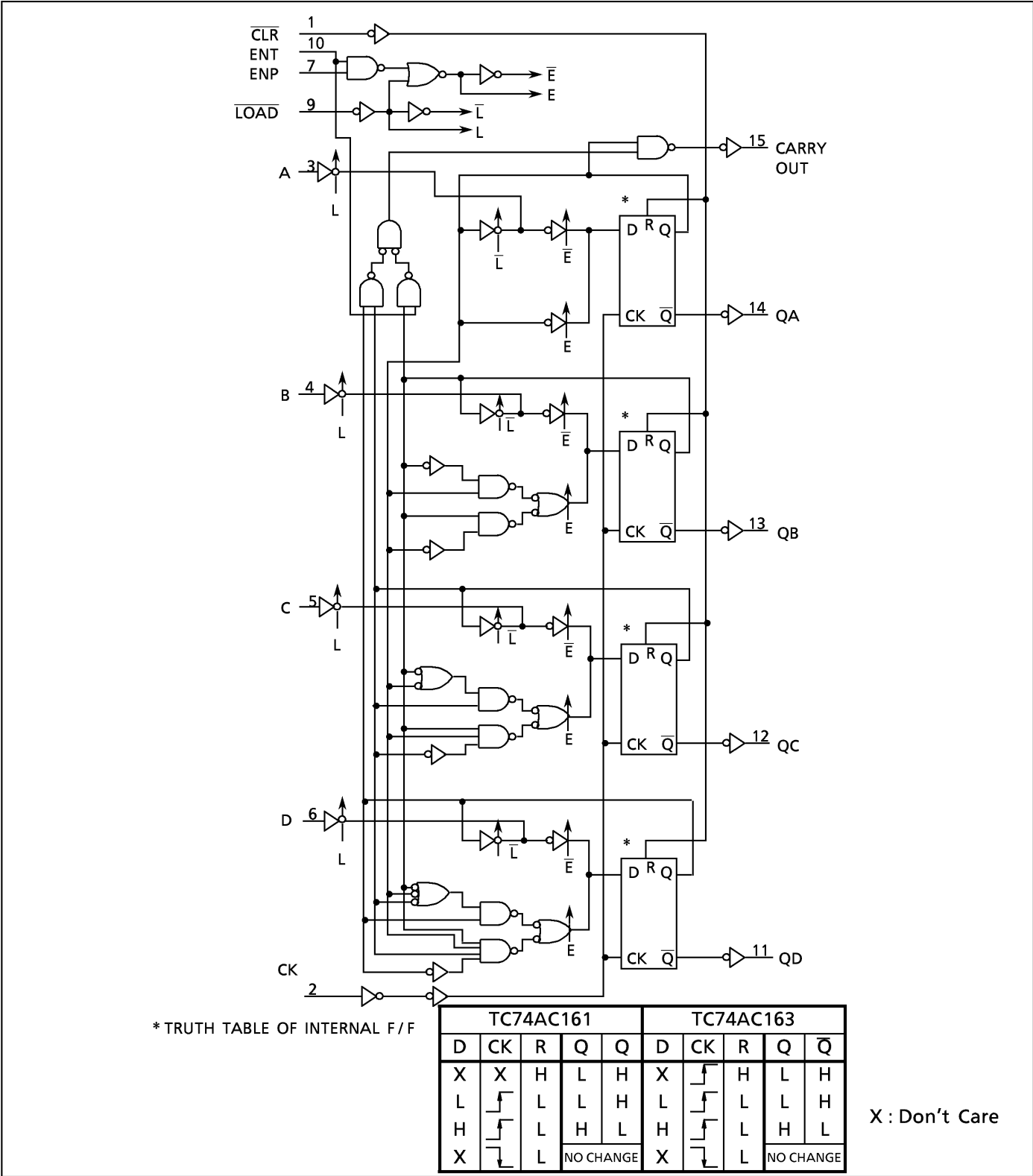
INPUTS							OUTPUTS				FUNCTION
CLR (161)	CLR (163)	LOAD	ENP	ENT	CK (161)	CK (163)	QA	QB	QC	QD	
L	L	X	X	X	X		L	L	L	L	RESET TO "0"
H	H	L	X	X			A	B	C	D	PRESET DATA
H	H	H	X	L			NO CHANGE				NO COUNT
H	H	H	L	X			NO CHANGE				NO COUNT
H	H	H	H	H			COUNT UP				COUNT
H	X	X	X	X			NO CHANGE				NO COUNT

Note X : Don't Care
A, B, C, D : Logic Level of Data Inputs
Carry : CARRY = ENT·QA · QB · QC · QD

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 125	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			$I_{OH} = -4\text{mA}$	3.0	2.58	—	—	2.48	
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			$I_{OL} = 12\text{mA}$	3.0	—	—	0.36	—	
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	1.65	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	8.0	—	80.0	μA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig .1	3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{\text{CLR}}$)*	$t_{W(L)}$	Fig .4	3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	7.0 5.0	
Minimum Set - up Time (LOAD, ENP, ENT)	t_s	Fig .2, 3	3.3 ± 0.3 5.0 ± 0.5	11.0 7.0	13.0 7.0	13.0 7.0	
Minimum Set - up Time (A, B, C, D)	t_s	Fig .2	3.3 ± 0.3 5.0 ± 0.5	8.0 4.0	8.0 4.0	8.0 4.0	
Minimum Set - up Time ($\overline{\text{CLR}}$)**	t_s	Fig .5	3.3 ± 0.3 5.0 ± 0.5	6.0 4.0	6.0 4.0	6.0 4.0	
Minimum Hold Time	t_h	Fig .2, 3, 5	3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{\text{CLR}}$)*	t_{rem}	Fig .4	3.3 ± 0.3 5.0 ± 0.5	6.0 4.0	6.0 4.0	6.0 4.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500 Ω , Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK—Q)	t _{pLH} t _{pHL}	Fig.1	3.3 ± 0.3 5.0 ± 0.5	— —	8.8 6.5	15.8 9.6	1.0 1.0	18.0 11.0	ns
Propagation Delay Time (CK—CARRY, Count Mode)	t _{pLH} t _{pHL}	Fig.1	3.3 ± 0.3 5.0 ± 0.5	— —	10.4 8.1	18.4 11.8	1.0 1.0	21.0 13.5	
Propagation Delay Time (CK—CARRY, Preset Mode)	t _{pLH} t _{pHL}	Fig.2	3.3 ± 0.3 5.0 ± 0.5	— —	12.9 9.1	22.4 13.2	1.0 1.0	25.5 15.0	
Propagation Delay Time (ENT—CARRY)	t _{pLH} t _{pHL}	Fig.6	3.3 ± 0.3 5.0 ± 0.5	— —	7.5 5.8	13.2 8.3	1.0 1.0	15.0 9.5	
Propagation Delay Time ($\overline{\text{CLR}}$ —Q)*	t _{pHL}	Fig.4	3.3 ± 0.3 5.0 ± 0.5	— —	10.6 7.7	18.4 11.4	1.0 1.0	21.0 13.0	
Propagation Delay Time ($\overline{\text{CLR}}$ —CARRY)*	t _{pHL}	Fig.4	3.3 ± 0.3 5.0 ± 0.5	— —	12.0 8.6	21.0 12.7	1.0 1.0	24.0 14.5	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3 5.0 ± 0.5	50 90	110 140	— —	50 90	— —	MHz
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	85	—	—	—	

Note * for TC74AC161 only

** for TC74AC163 only

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD} , and ΔI_{CC} which is obtained from the following formula :

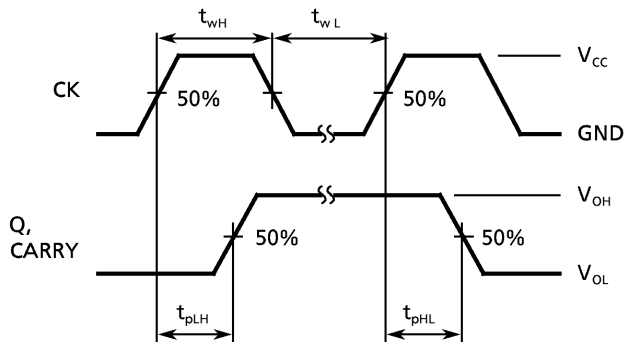
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

$C_{QA} \sim C_{QD}$ and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.

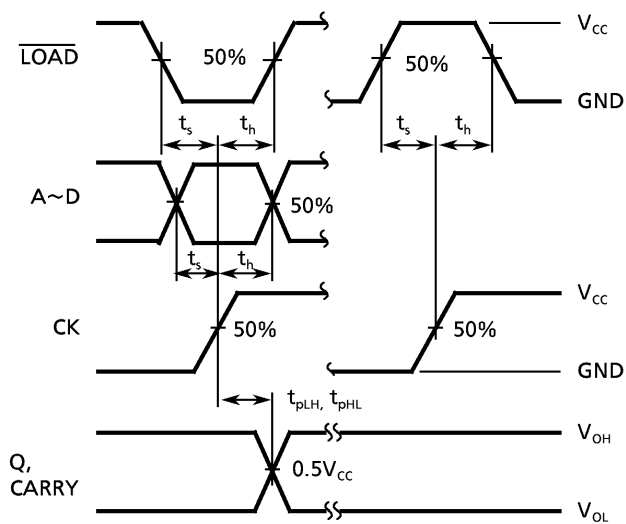
f_{CK} is the input frequency of the CK.

SWITCHING CHARACTERISTICS TEST WAVEFORM

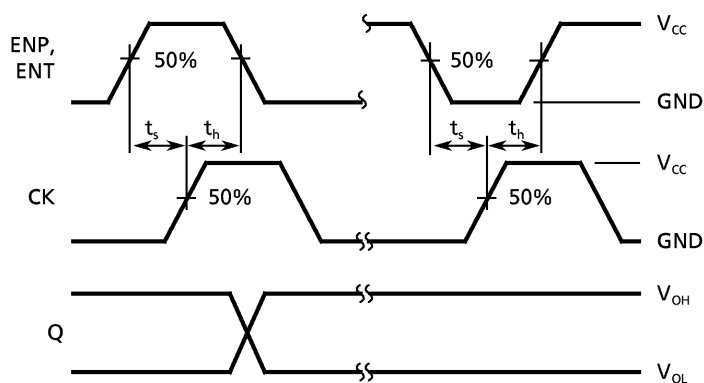
COUNT MODE (Fig. 1)



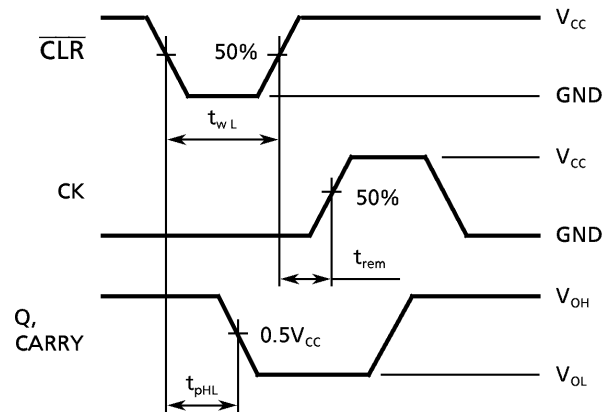
PRESET MODE (Fig. 2)



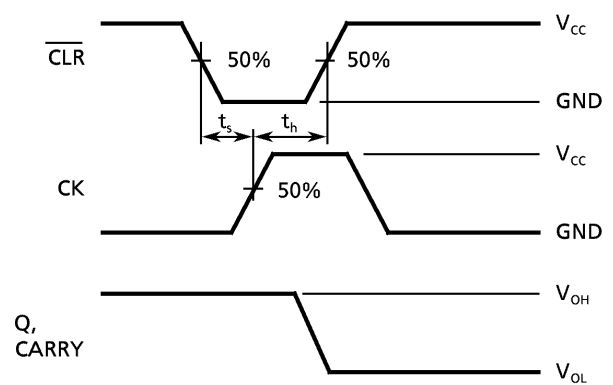
COUNT ENABLE MODE (Fig. 3)



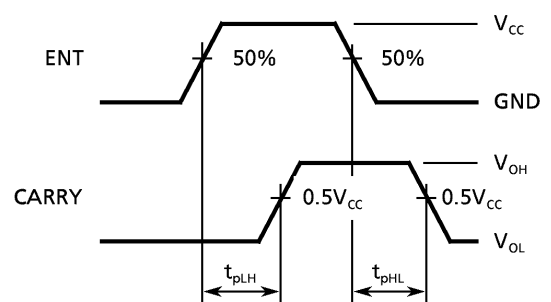
CLEAR MODE (TC74AC161) (Fig. 4)



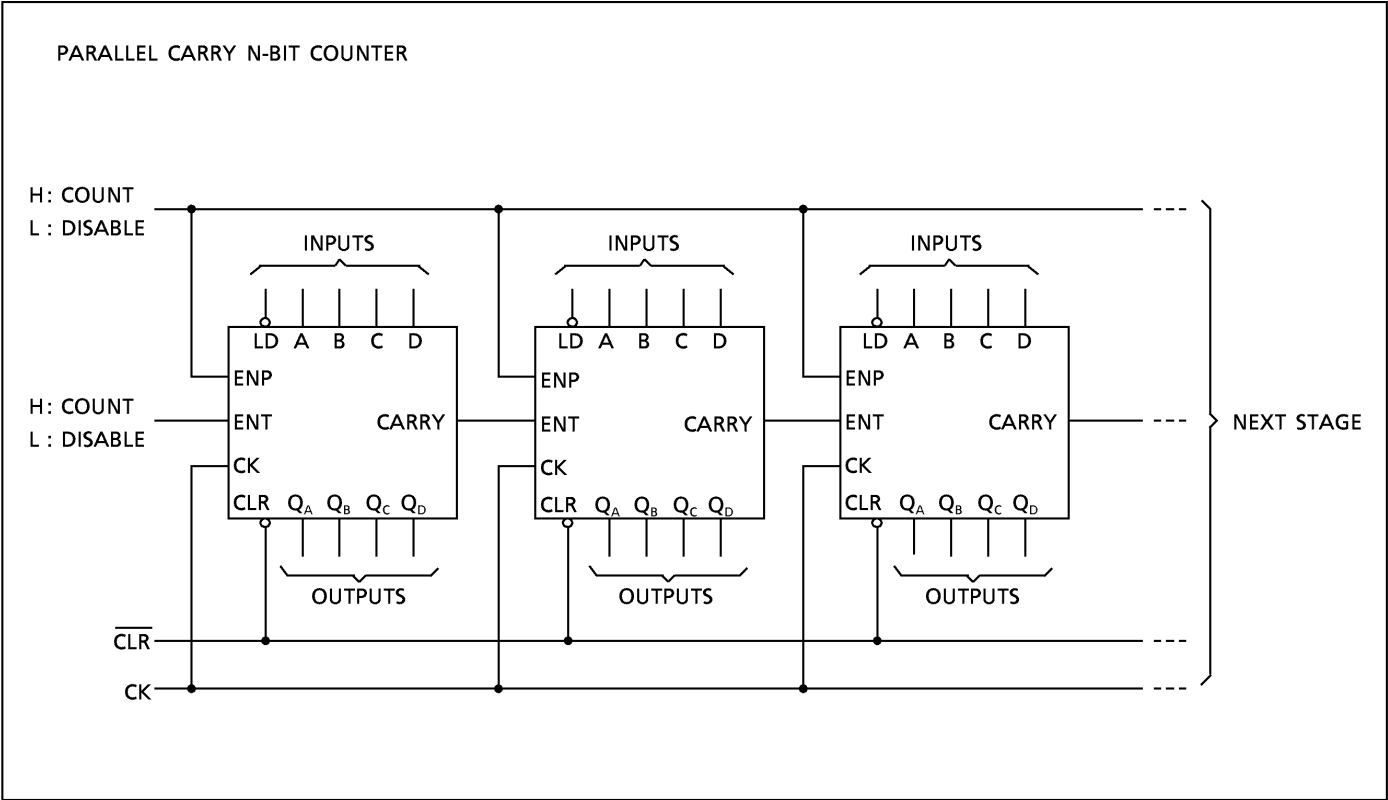
CLEAR MODE (TC74AC163) (Fig. 5)



CASCADE MODE (Fix Maximum Count) (Fig. 6)

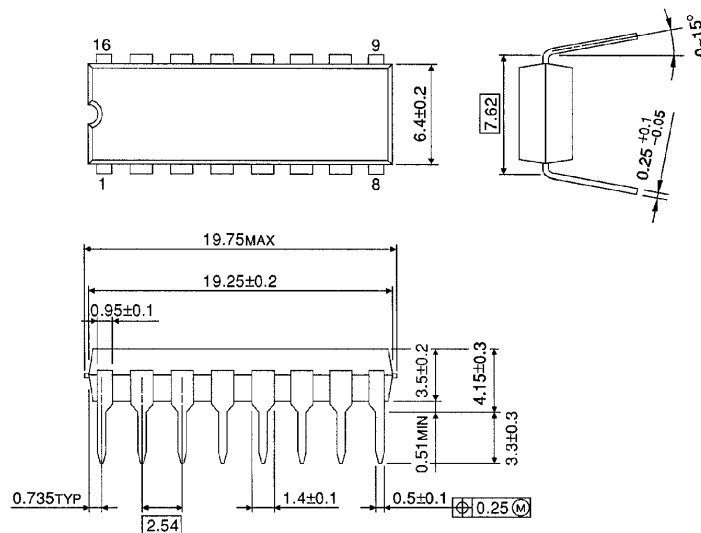


TYPICAL APPLICATION



DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

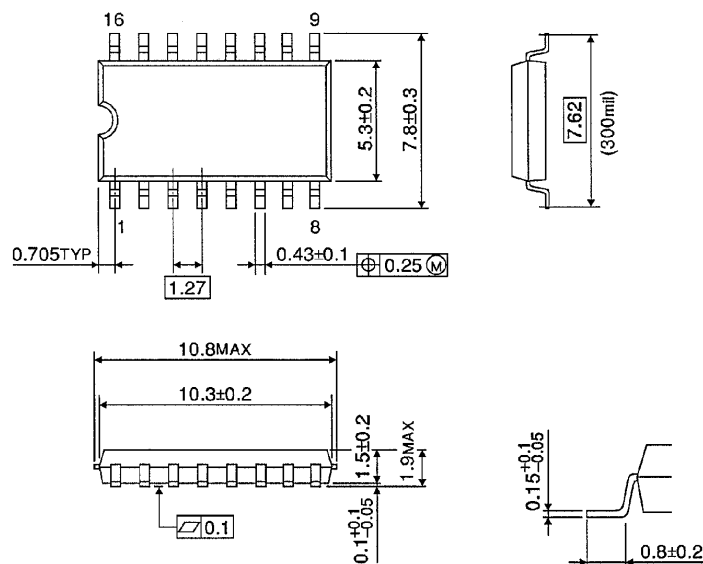
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

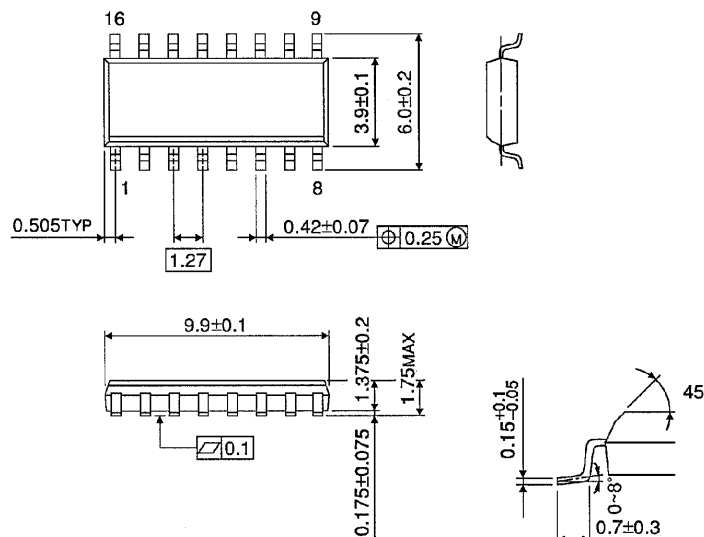


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

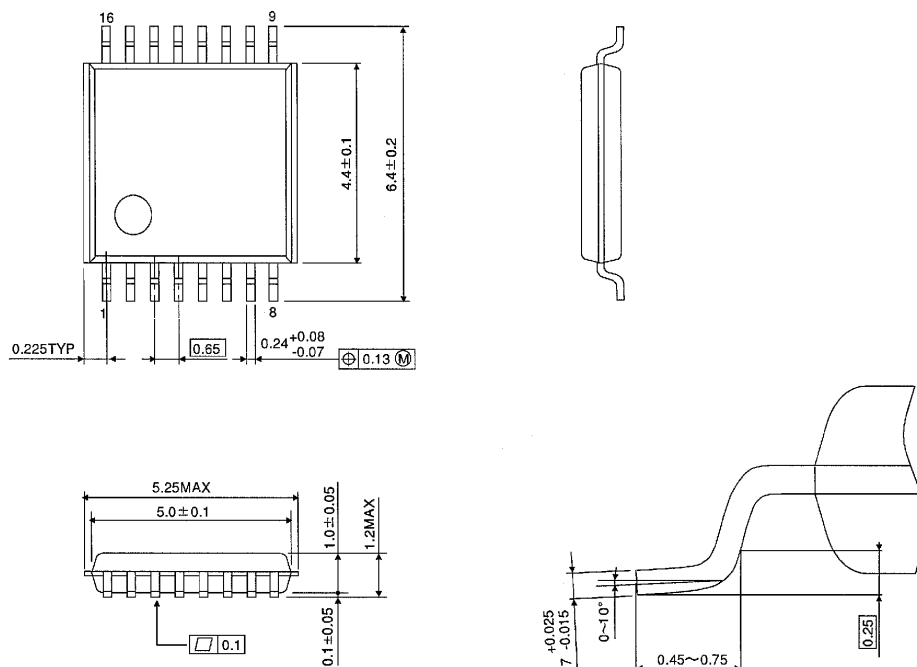
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.