

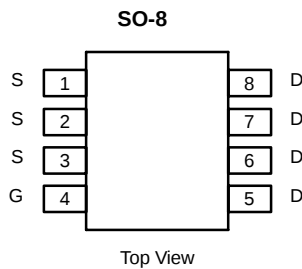


N-Channel 100-V (D-S) MOSFET

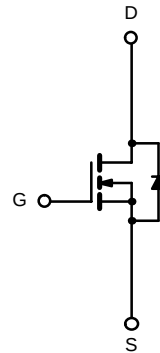
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.060 @ $V_{GS} = 10$ V	4.6
	0.080 @ $V_{GS} = 6$ V	4.0

TrenchFET®
Power MOSFETs



Ordering Information: Si4482DY
Si4482DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	4.6	A
	$T_A = 70^\circ\text{C}$		3.7	
Pulsed Drain Current		I_{DM}	40	
Continuous Source Current (Diode Conduction) ^a		I_S	2.1	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

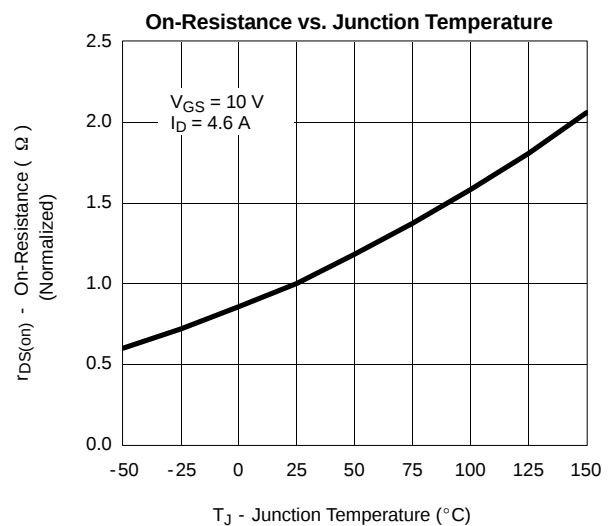
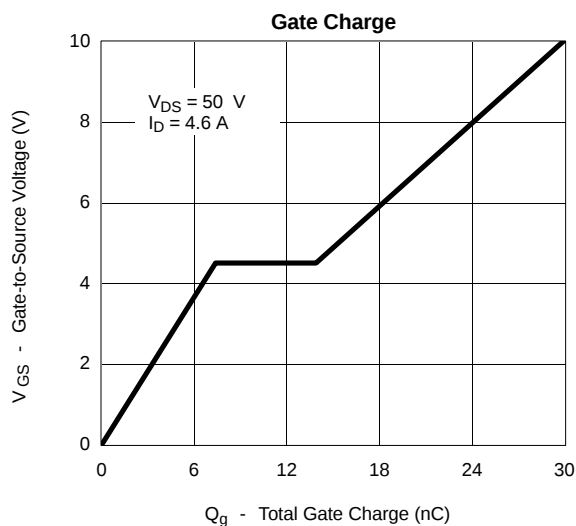
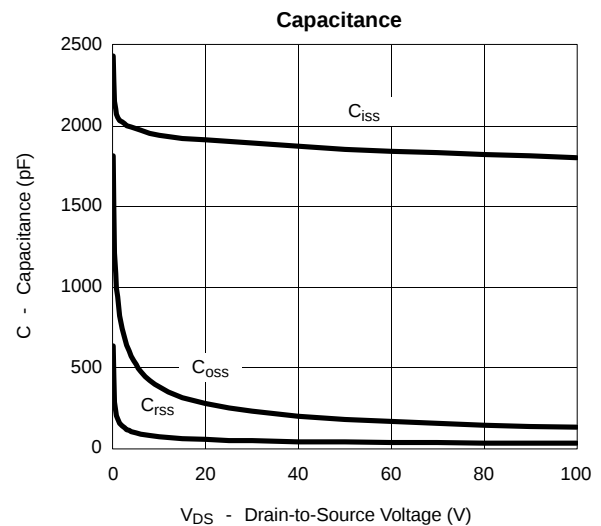
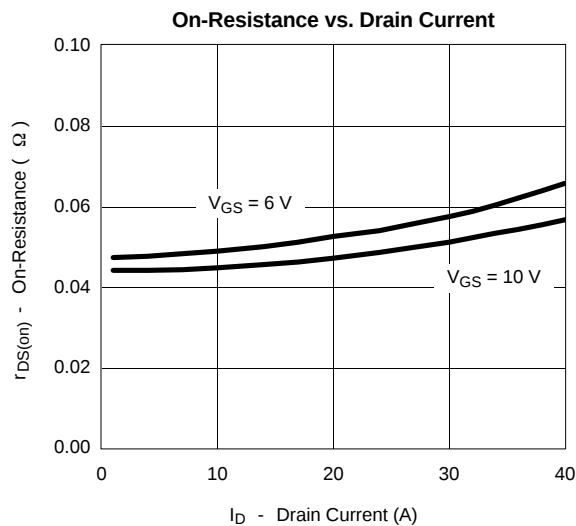
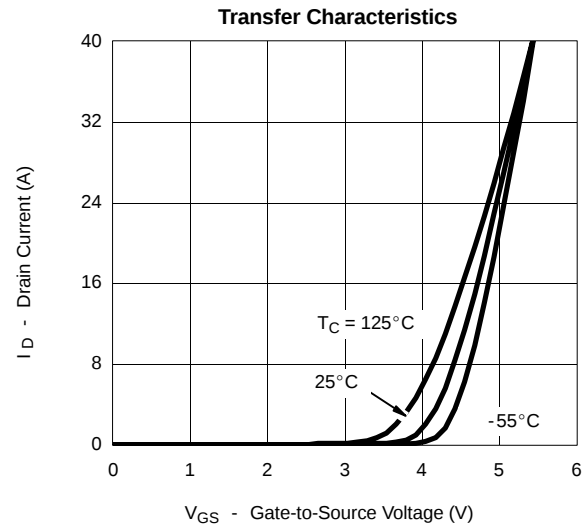
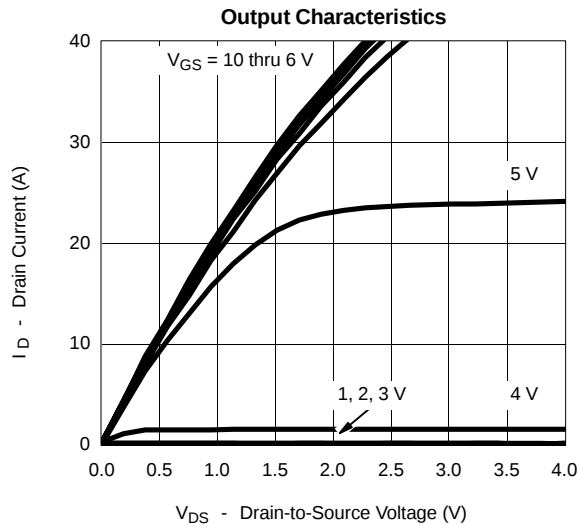
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 4.6\ \text{A}$		0.045	0.060	Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 4.0\ \text{A}$		0.050	0.080	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 4.6\ \text{A}$		20		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\ \text{A}$, $V_{GS} = 0\ \text{V}$			1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 4.6\ \text{A}$		30	50	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			7		
Gate Resistance	R_g		1		4.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}$, $R_L = 50\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		13	25	ns
Rise Time	t_r			12	25	
Turn-Off Delay Time	$t_{d(off)}$			60	90	
Fall Time	t_f			25	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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