SBWS015A – AUGUST 2001

G.SHDSL ANALOG FRONT-END

FEATURES

- **E1, T1, AND SUBRATE OPERATION**
- **COMPLIES WITH G.SHDSL AND HDSL2**
- **16-BIT, DELTA-SIGMA CONVERTERS**
- **ON-CHIP DRIVER AND PGA**
- **PROGRAMMABLE tx AND rx FILTERS**
- **SERIAL DIGITAL INTERFACE**
- **750mW POWER DISSIPATION AT E1**
- **+5V POWER (5V OR 3.3V DIGITAL)**
- **SSOP-28 PACKAGE**
- **–40°C TO +85°C TEMPERATURE RANGE**

DESCRIPTION

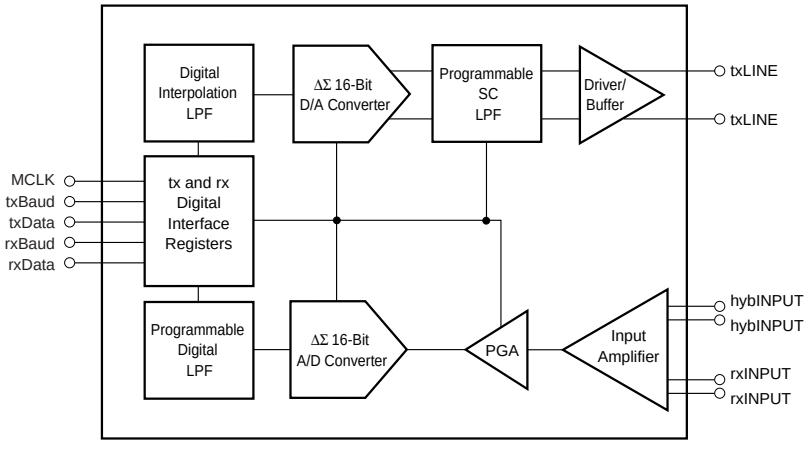
Texas Instrument's analog front-end chip, the AFE1230, is designed to greatly reduce the size and cost of G.SHDSL and HDSL2 application designs. It provides a transceiver as the line interface between the Digital Signal Processor (DSP) and the local loop. The AFE1230 is designed to handle upstream and downstream data transmission over a wide range of data rates from 64kbps to 2.5Mbps. Functionally, this unit consists of a transmitter and receiver section.

The transmitter section consists of a digital interpolation filter, a 16-bit, delta-sigma Digital-to-Analog (D/A) converter, a digitally programmable fifth-order or seventh-order SC (Switched Capacitor) low-pass filter, and a differential output line driver. The receiver section includes an input Programmable Gain Amplifier (PGA), a 16-bit, delta-sigma Analog-to-Digital (A/D) converter, and a programmable decimation filter.

The AFE1230 receives a 16-bit data word plus an 8-bit control byte via the serial interface to facilitate the D/A conversion and control functions. The subsequent analog signal is sent to the on-chip line driver that provides 14.5dBm power into a 135Ω line for G.SHDSL operation. In addition, the on-chip line driver can be used as an output buffer with an external line driver, such as the OPA2677, to generate over 17dBm power into a 135Ω line for HDSL2 operation. With an appropriate DSP, the transmitted Power Spectral Density (PSD) complies with either the G.SHDSL standard or with the HDSL2 standard (via an OPA2677 used as an external driver).

In the receive path, the input amplifier sums the signals from the line and hybrid path to perform first-order analog echo cancellation. The resultant signal is then digitized by the rest of the receive section into a 16-bit digital word that is sent to the external DSP.

This IC operates on a single 5V supply, while the digital supply can be from 3.3V to 5V. It is housed in a SSOP-28 package. The typical power consumption is 750mW at E1 rates with G.SHDSL (560mW for HDSL2 operation) and an operation temperature range of –40°C to +85°C.



AFE1230

Patents Pending

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	±100mA, Momentary
Analog Input: Current	±10mA, Continuous
Analog Input: Voltage	AGND –0.3V to AV_{DD} +0.3V
Analog Outputs Short-Circuit to Ground (+25°C)	Continuous
AV_{DD} to AGND	–0.3V to +6V
DV_{DD} to DGND	–0.3V to +6V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
AGND, DGND Differential Voltage	0.3V
Junction Temperature (Tj)	150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature Range (soldering, 3s)	+260°C
Power Dissipation	1000mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

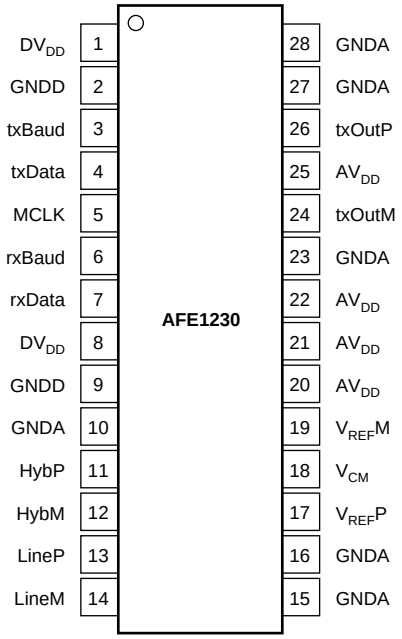
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
AFE1230E	SSOP-28	324	DBQ	–40°C to +85°C	AFE1230E	AFE1230E	Rail
AFE1230E/1K	"	"	"	"	"	AFE1230E/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "AFE1230E/1K" will get a single 1000-piece Tape and Reel. The AFE1230E/1K can only be ordered in 1000-unit increments.

PIN CONFIGURATION

Top View SSOP



PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	DV_{DD}	Power	Digital Supply
2	GNDD	Ground	Digital Ground
3	txBaud	Input	Transmit Baud Clock
4	txData	Input	Digital Input of Transmit Section
5	MCLK	Input	Master Clock 48x Clock
6	rxBaud	Input	Recieve Baud Clock
7	rxData	Output	Digital Output of Recieve Section
8	DV_{DD}	Power	Digital Supply
9	GNDD	Ground	Digital Ground
10	GNDA	Ground	Analog Ground
11	HybP	Input	Positive Hybrid Input
12	HybM	Input	Negative Hybrid Input
13	LineP	Input	Positive Line Input
14	LineM	Input	Negative Line Input
15	GNDA	Ground	Analog Ground—Recieve
16	GNDA	Ground	Analog Ground—Reference
17	$V_{REF}P$	Output	Positive Reference Voltage, rx/tx
18	V_{CM}	Output	Common-Mode Voltage, rx/tx
19	$V_{REF}M$	Output	Negative Reference Input, rx/tx
20	AV_{DD}	Power	Analog Supply—Reference
21	AV_{DD}	Power	Analog Supply—Recieve
22	AV_{DD}	Power	Analog Supply—Transmit
23	GNDA	Ground	Analog Ground/Driver
24	txOutM	Output	Line Driver Output Negative
25	AV_{DD}	Power	Analog Supply/Driver
26	txOutP	Output	Line Driver Output Positive
27	GNDA	Ground	Analog Ground/Driver
28	GNDA	Ground	Analog Ground Transmit

ELECTRICAL CHARACTERISTICS

All specifications are typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, MCLK = 37.1MHz (E1 rate), unless otherwise noted.

PARAMETER	CONDITIONS	AFE1230E			UNITS
		MIN	TYP	MAX	
RECEIVE CHANNEL					
Number of Inputs	Differential		2		
Input Voltage Range	Balanced Differential(1)		±3.1		V
Common-Mode Voltage			AV_{DD}/2		V
A/D Converter Code	ΔΣ A/D Converter		16		Bits
Programmable Gain Range	3dB Steps	0		+21	dB
Gain Absolute Accuracy	R_{IN} = 10kΩ		±20%		%
Gain Step Accuracy	3dB Steps, Accuracy Relative to Gain = 1			±0.5	dB
Settling Time for Gain Change			6		Symbol Periods
Output Data Coding	Binary Two's Complement		16		Bits
MCLK	Master Clock	1.28		40.8	MHz
System Bit Rate		80k		2.55M	bps
Symbol Rate	Three Bits/Symbol	26.7		850	kHz
Output Word Rate (OWR)	Two rx Words/Symbol Period(2)	53.4		1700	kHz
Filter Cutoff Frequency(3)	Programmable 5th-Order LPF, 0.25x and 0.5x OWR	0.25		0.5	OWR
TRANSMIT CHANNEL					
D/A Converter Code	ΔΣ D/A Converter		16		Bits
Output Line Power(4)	Internal Line Driver, PAR = 3, Provides 14.5dBm at 135Ω Line with 1:3.7 Transformer	14.5			dBm
Output Power(5)	Internal Line Buffer, PAR = 4, Load is External Driver OPA2677	10			dBm
Output Voltage	Balanced Differential		±3.1		V
Common-Mode Voltage, V_{CM}			AV_{DD}/2		V
Output Resistance	DC to 1MHz		0.2		Ω
Input Data Coding	Binary Two's Complement		16		Bits
MCLK	Master Clock	1.28		40.8	MHz
System Bit Rate	Three Bits/Symbol	80k		2.55M	bps
Input Symbol Rate	Three Bits/Symbol	26.7		850	kHz
Input Word Rate (IWR)	Two Words/Symbol Period	53.4		1700	kHz
Filter Cutoff Frequency(6)	5th or 7th LPF, 0.25x, 0.38x, 0.5x IWR	0.25		0.5	IWR
TRASNSCEIVER PERFORMANCE					
Uncancelled Echo(7)	rxGAIN = 12dB			–80	dB
DIGITAL INTERFACE					
Logic Levels:					
V_{IH}	$\|I_{IH}\|$ < 10µA	DV_{DD} – 1		DV_{DD} + 0.3	V
V_{IL}	$\|I_{IL}\|$ < 10µA	–0.3		+0.8	V
V_{OH}	I_{OH} = –20µA	DV_{DD} – 0.5			V
V_{OL}	I_{OL} = 20µA			+0.4	V
POWER					
Analog Power-Supply Voltage	Specification		5		V
Analog Power-Supply Voltage	Operating Range	4.75		5.25	V
Digital Power-Supply Voltage	Specification		3.3		V
Digital Power-Supply Voltage	Operating Range	3.15		5.25	V
Power Dissipation(8)	AV_{DD} = 5V, DV_{DD} = 3.3V, 14.5dBm at 135Ω Line, E1		750		mW
Power Dissipation(9)	AV_{DD} = 5V, DV_{DD} = 3.3V		560		mW
PSRR			60		dB
TEMPERATURE RANGE					
Operating(10)		–40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out-of-phase with the negative input, therefore, the actual voltage swing about the common-mode voltage on each pin is ±1.55V to achieve a total input range of ±3.1V or 6.2Vp-p. (2) The A/D converter oversamples the receive signal and outputs data words at twice the symbol rate; the A/D converter conversion rate is called the Output Word Rate (OWR). (3) The digital low-pass filter that is part of the A/D converter can be programmed by the user for a 3dB frequency of 1/2 of the OWR or 1/4 of the OWR. (4) The internal line driver is designed for G.SHDSL. (5) An external driver (OPA2677) should be used for HDSL2 application. (6) The cutoff frequencies are user programmable. (7) Uncancelled echo is the sum of all noise and distortion errors for both the transmit and receive channels. (8) For a random sequence of the symbol, using an internal driver providing 14.5dBm power to the line for G.SHDSL. (9) For a random sequence while driving an external line driver (OPA2677) for HDSL2. (10) Functionality only guaranteed over temperature range.

APPLICATION INFORMATION

THEORY OF OPERATION

The AFE1230 consists of a transmitter and receiver section, as shown in Figure 1; the transmitter section consists of a digital interpolation filter, a 16-bit, delta-sigma D/A converter, a programmable fifth-order or seventh-order SC low-pass filter, and a differential output line driver. The receiver section includes a digitally programmable gain amplifier, a 16-bit, delta-sigma A/D converter, and a decimation filter. The AFE1230 receives a 16-bit word plus an 8-bit control byte via the serial interface to facilitate the D/A conversion and control functions. The received 16-bit word is up sampled by two through the digital interpolation filter, then oversampled by the delta-sigma modulator by a factor of 12x where it is then processed by the multilevel D/A converter section before being filtered by the fifth-order or seventh-order Butterworth low-pass SC filter section.

The subsequent analog signal is sent to the on-chip line driver where the analog signal can be driven into an appropriate transformer to provide up to 14.5dBm power into a 135Ω line for G.SHDSL. In addition, the on-chip line driver can be used as an output buffer to generate 17dBm into a 135Ω line via an external line driver (such as the OPA2677) for HDSL2. With an appropriate DSP, the transmitted PSD complies with either the G.SHDSL standard or, with an OPA2677 used as an external driver, the HDSL2 standard.

In the receive path, the input amplifier sums the signals from the line and hybrid paths to perform first-order analog echo cancellation. The resultant signal is then digitized by a fourth-order cascaded delta-sigma A/D converter with an OSR (OverSampling Ratio) of 24x. The subsequent oversampled signal is processed by a $sinc^5$ filter as well as a programmable IIR filter for droop compensation and additional quantization noise reduction. The resulting digital signal is sent to the serial interface for processing by the DSP.

Transmit Filter

The transmit filter consists of two sections, a digital interpolation filter and a programmable SC low-pass filter (SCLPF). The interpolation filter is an anti-imaging low-pass filter. The SCLPF serves two important functions. First it is designed to remove quantization noise from the delta-sigma D/A converter in the front end of the transmit path. Secondly, the filter is used to help shape the received digital signal's spectral density in conjunction with pre-spectral shaping within the DSP. Depending on the particular response desired, the transmit filter section can be programmed for three different breakpoints, as shown in Table 1, as well as two filter order (fifth or seventh) configurations. The 3dB frequency listed in Table I is in relation to the designed breakpoint for the SC filter only. However, because the digital signal is sampled and held for 24 more samples (the AFE1230 increases the sample rate by 24x in relation to the input data rate), the actual transmit spectral curves contain a small amount of droop due to the sinc function performed by the sample and hold function of the delta-sigma modulator section of the transmit path. See Figures 2 and 3 for the overall spectral templates.

tx CUTOFF (txData Bits 29, 28)	RATIO (Corner Frequency)
00	0.25 MCLK/24
01	0.38 MCLK/24
10	0.5 MCLK/24

TABLE I. tx Filter Cutoff Frequency Setting.

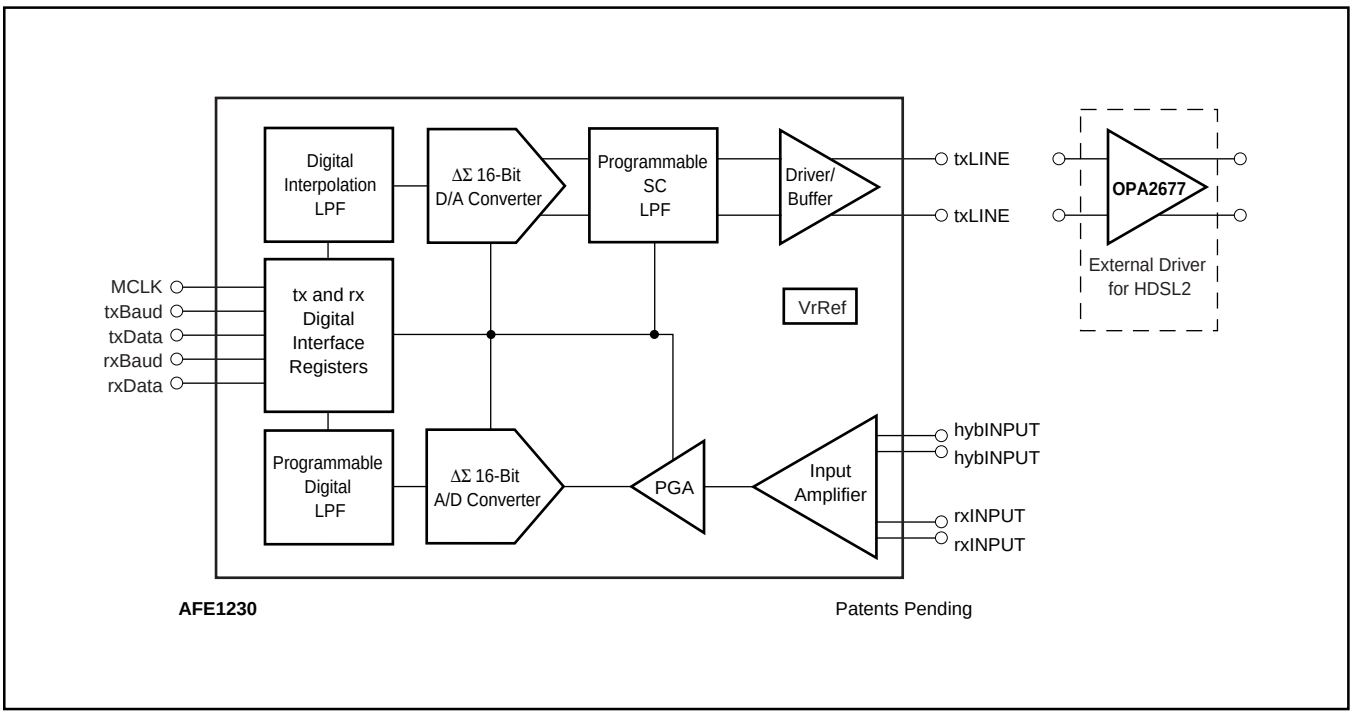


FIGURE 1. Functional Block Diagram of the AFE1230.

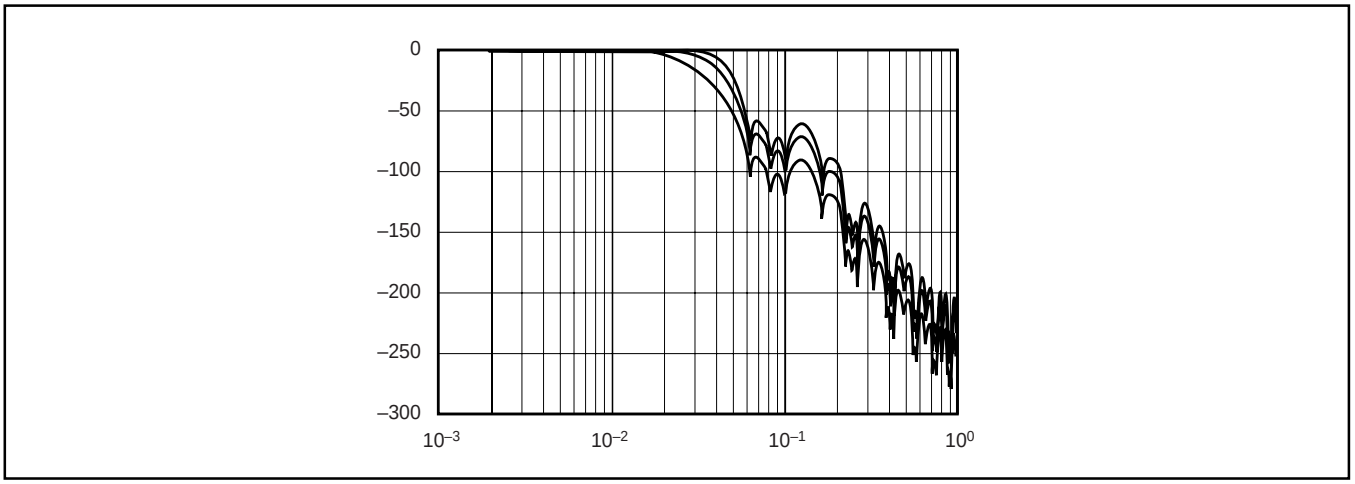


FIGURE 2. Overall Transmit Filter. D/A Converter Frequency Response, Fifth-Order with 0.25x, 0.38x, and 0.5x.

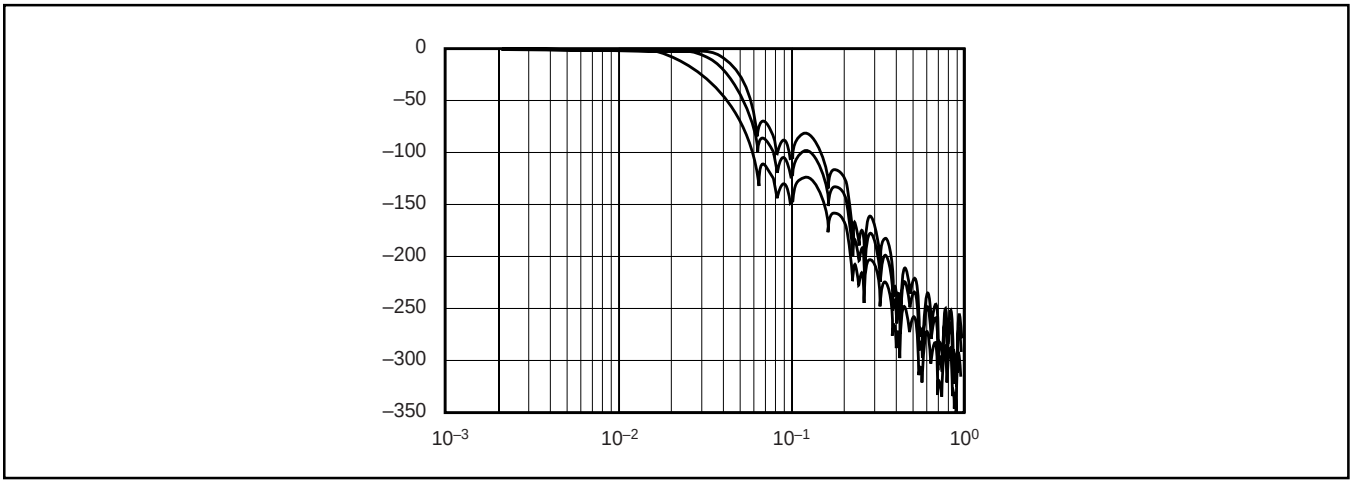


FIGURE 3. Overall Transmit Filter. D/A Converter Frequency Response, Seventh-Order with 0.25x, 0.38x, and 0.5x.

Receive Filter

The receive filter consists of three independent sections used for both the removal of quantization noise as well as the reduction of data rate (otherwise known as downsampling). The first section is comprised of a $sinc^5$ filter with a downsampling ratio of 12x. The resulting digital signal is then passed to a droop compensation filter before being sent through the final IIR filter section, while being downsampled by two. Two filter cutoff configurations are available, as seen in Table II. The corresponding cutoff frequencies relate to the full-rate low-pass filter spectral template of the filter, as seen from the inputs of Table II.

rx CUTOFF (txData Bit 24)	RATIO (Corner Frequency)
0	0.25 MCLK/24
1	0.5 MCLK/24

TABLE II. rx Filter Cutoff Frequency Setting.

Transmit Power

The on-chip differential line driver is designed to drive G.SHDSL power levels directly, or it can be used as a low-power buffer for driving a higher power external driver (for example the OPA2677) for applications such as HDSL2. The AFE1230 driver will generate an output swing of 6.2V peak-to-peak differential. When used with a suitable transformer (see Figures 8 and 10), the AFE1230 can generate up to 14.5dBm of power into a 135Ω line load. When used as a buffer with an OPA2677 driver, 17dBm of power can be generated. Relative transmit power can be controlled digitally through control bits sent to the transmit section by the serial interface. Relative transmit power reduction can be set to 0, –6, –12, or –18dB, depending on the control bits presented to the AFE1230, as shown in Table III.

TRANSMIT POWER BACK OFF CODE (txData Bits 25, 26)	TRANSMIT POWER REDUCTION	TRANSMIT POWER	
		G.SHDSL	HDSL2
00	0dB	14.5dBm	17.0dBm
01	–6dB	8.5dBm	11.0dBm
10	–12dB	2.5dBm	5.0dBm
11	–18dB	–4.5dBm	–1.0dBm

TABLE III. Transmit Power Backoff.

Receive Amplifier

The AFE1230 receive channel includes an input amplifier with a differential summer junction on-chip for echo cancellation, as shown in Figure 4. Four external resistors are needed with 10kΩ as the required value for each receiver-input pair as well as 20kΩ for each hybrid-input pair. The common-mode voltage of the receive amplifier is $AV_{DD}/2$ (typical value is 2.5V).

Serial Digital Interface Operation

The AFE1230 digital interface uses a five-line serial interface, signal names are: Master Clock (MCLK), Transmit Baud Clock (txBaud), Transmit Data (txData), Receive Baud Clock (rxBaud), and Receive Data (rxData). MCLK, txBaud, rxBaud, and txData must come from the external DSP where data is transmitted in synchronization with MCLK. MCLK is used as the internal master clock to the AFE1230 and can run up to 40.8MHz. txBaud and rxBaud must be the same frequency and synchronous with MCLK, however, the phase of these signals may be different. Each baud period contains 48 MCLK cycles. During each baud cycle, txData will contain two 16-bit transmit words with two control bytes. Each bit is latched internally to the AFE at the rising edge of MCLK. Figures 5, 6, and 7 illustrate the bit designations as well as the proper timings required to operate the AFE1230.

MCLK: The master clock of AFE1230 for both transmit and receive sections, generated by the DSP. It runs at 48x the symbol rate and can be varied from 1.28MHz to 40.8MHz (37.12MHz for E1). MCLK must use a 50/50 duty cycle.

txBaud: The transmit data baud clock, generated by the DSP. txBaud is 517.33kHz for T1 and 773.33kHz for E1 (2.3Mbps). It may vary from 26.7kHz to 850kHz. A txBaud period consists of 48 periods of the MCLK. The time (t_W) of the txBaud should not be smaller than one MCLK period. Within the period of 48 MCLK clocks, the rising edge of the txBaud can occur any time except in the period of t_F, and the falling edge of txBaud can occur at any time of the t_F period.

txData: The input digital data of AFE1230. This signal comes from an external DSP with 48 bits per baud period. The 48 bits include two 16-bit words of D/A converter input data and two 8-bit control bytes (see Tables IV and V). The D/A converter is updated two times per symbol period and data is latched by the AFE1230 on the rising edge of MCLK. txData must be stable at least 2.5ns before the rising edge of MCLK and it must remain stable at least 2.5ns after the rising edge of MCLK.

rxBaud: The receive data baud clock, generated by the DSP. rxBaud is 517.33kHz for T1 and 773.33kHz for E1 (2.3Mbps). It may vary from 26.7kHz to 850kHz. One rxBaud period consists of 48 periods of the MCLK. Within the period of 48 MCLK clocks, the rising edge of the rxBaud can occur at any time except in t_F period, and the falling edge of rxBaud can occur at any time during t_F. The width of the rxBaud pulse should be no shorter than one period of MCLK.

rxData: The output digital data of AFE1230, sent to the external DSP with 48 bits per baud period. The 48 bits include two 16-bit words of receive data and two 8-bit control words (Reserved) (see Tables VI and VII). The A/D converter is updated two times per symbol period and rxData is changed by AFE1230 at the falling edge of MCLK. rxData is stable at least 2.5ns before the rising edge of MCLK and it remains stable at least 2.5ns after the rising edge of MCLK.

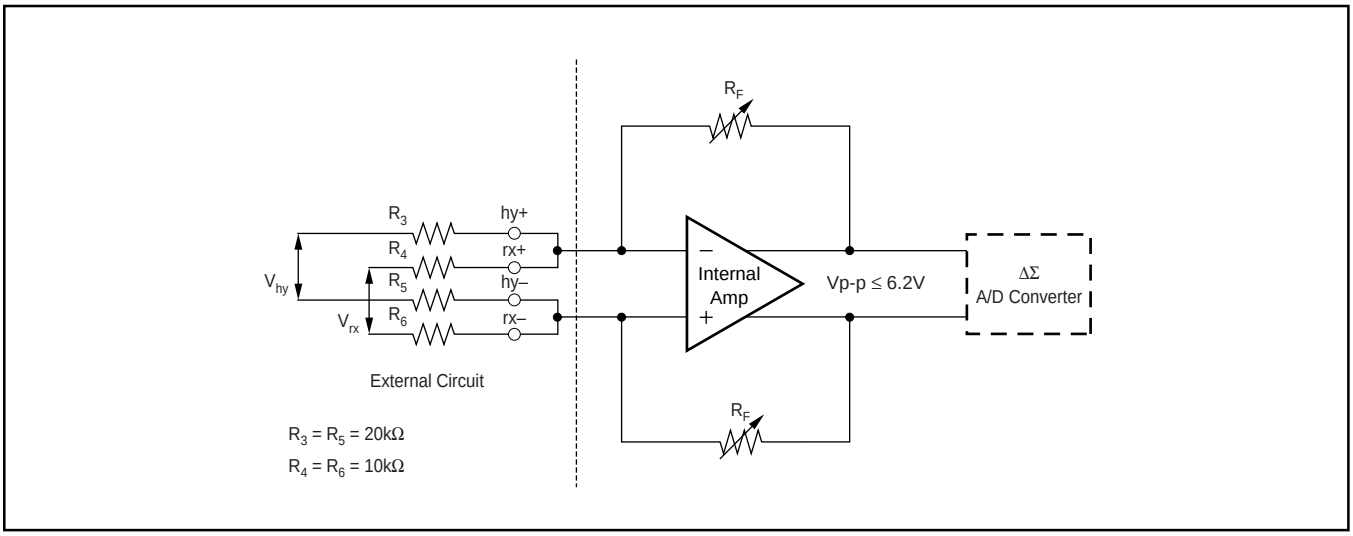


FIGURE 4. Internal Receive Amplifier.

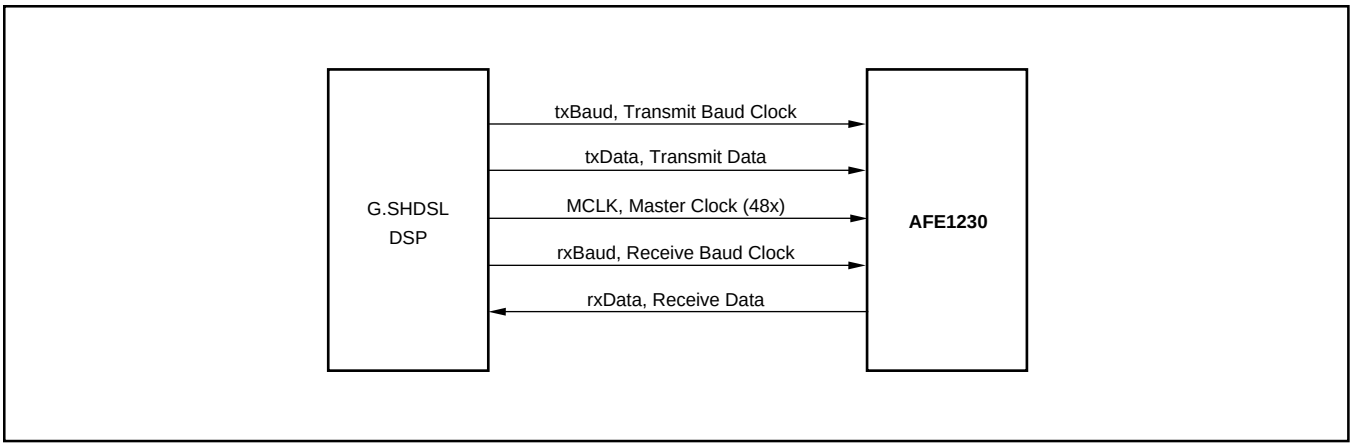


FIGURE 5. AFE1230/DSP Digital Interface.

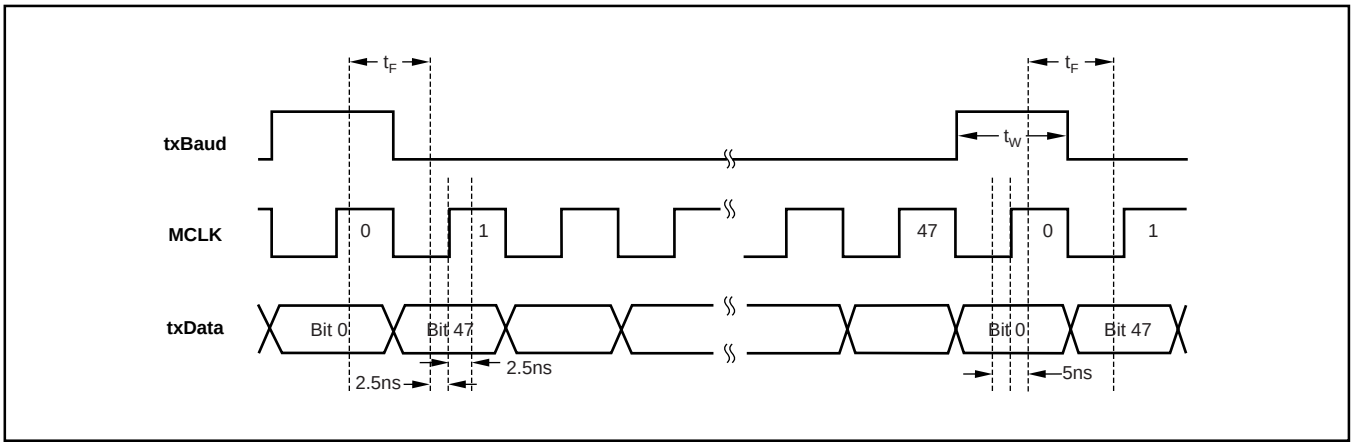


FIGURE 6. AFE1230 Transmit Timing Diagram.

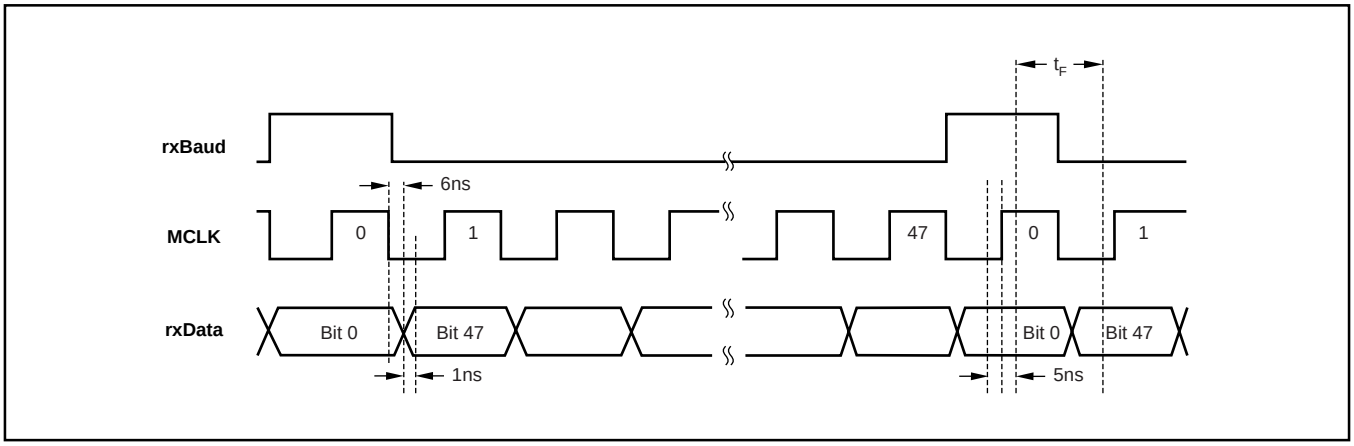


FIGURE 7. AFE1230 Receive Timing Diagram.

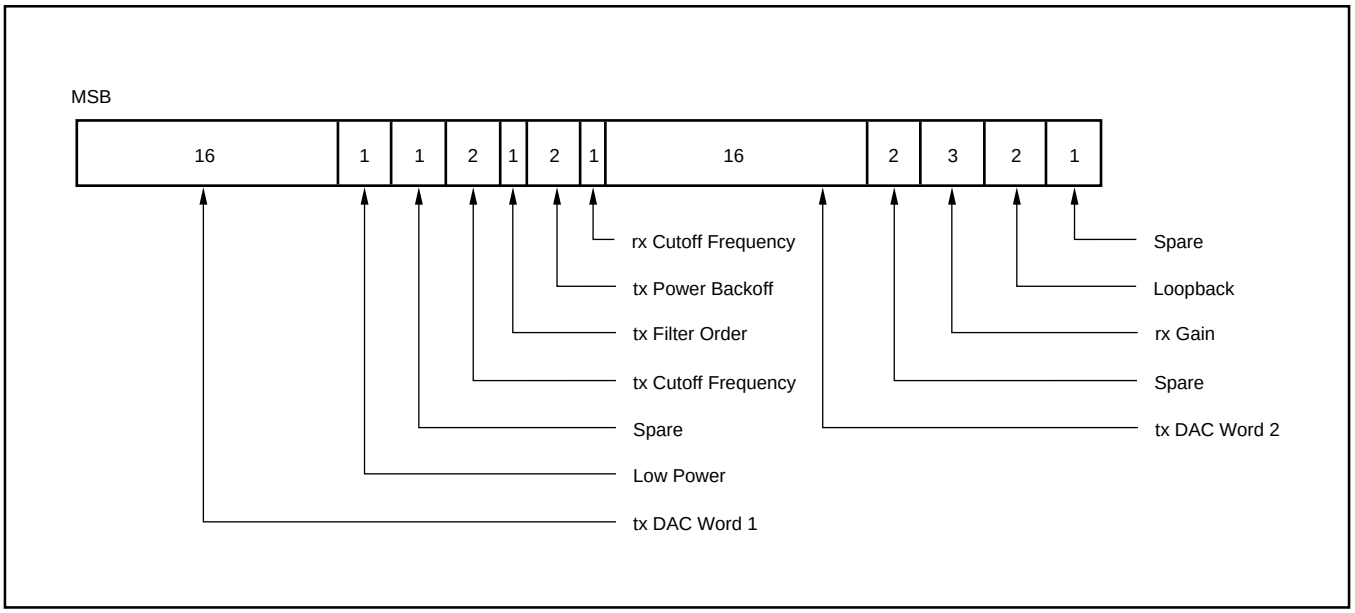


TABLE IV. tx Data Structure.

BIT	DESCRIPTION	BIT STATE	OUTPUT STATE
47-32	tx D/A Converter Word 1	XXXX	16-Bit Binary Two's Complement Word to tx D/A Converter (MSB First)
31	Power Control	0	Normal Power, Any Speed
		1	Low Power, Low Speed (< 1/2 Full Word Rate)
30	Reserved(1)	0	Reserved for Future Use
29-28	tx Cutoff Frequency Control	00	0.25x Word Rate
		01	0.38x Word Rate
		10	0.5x Word Rate
		11	Not Used
27	tx Filter Order	0	Fifth-Order Butterworth
		1	Seventh-Order Butterworth
26-25	tx Power Backoff	00	Normal Transient Power
		01	Normal Transient Power –6dB
		10	Normal Transient Power –12dB
		11	Normal Transient Power –18dB
24	rx Cutoff Frequency Control	0	0.25x Word Rate
		1	0.5x Word Rate
23-8	tx D/A Converter Word 2	XXXX	16-Bit Binary Two's Complement Word to tx D/A Converter (MSB First)
7-6	Reserved(1)	00	Reserved for Future Use
5-3	rx Gain Settings	000	rx Gain = 0dB
		001	rx Gain = 3dB
		010	rx Gain = 6dB
		011	rx Gain = 9dB
		100	rx Gain = 12dB
		101	rx Gain = 15dB
		110	rx Gain = 18dB
		111	rx Gain = 21dB
2-1	Loop-Back Control	00	Normal Operation
		01	Loop-Back Mode Digital, tx Data to rx Data
		10	Hybrid Mode, Line Input Connected to V_{CM}
		11	Line Mode, Hybrid Input Connected to V_{CM}
0	Reserved(1)	0	Reserved

NOTE: (1) Reserved Bits must be set to 0.

TABLE V. tx Data Format.

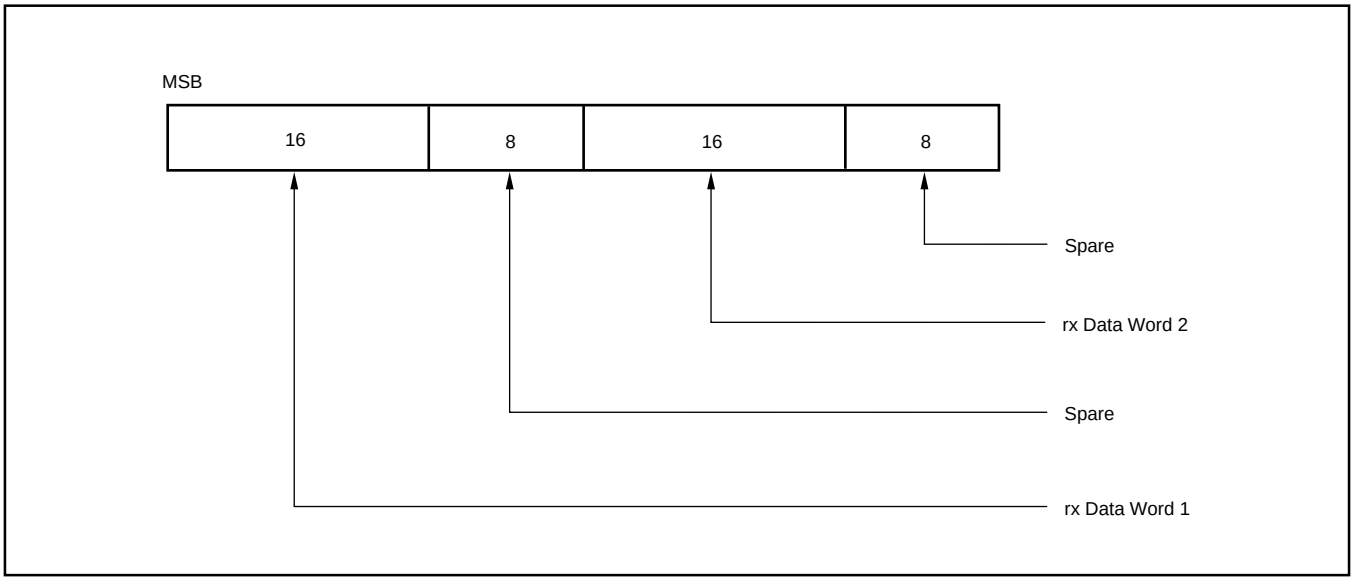


TABLE VI. rx Data Structure.

BIT	DESCRIPTION	BIT STATE	OUTPUT STATE
47-32	rx A/D Converter Word 1	XXXX	16-Bit Binary Two's Complement Word from rx A/D Converter (MSB First)
31-24	Reserved	Set All Bits Always to 0	Reserved for Future Use
23-8	rx A/D Converter Word 2	XXXX	16-Bit Binary Two's Complement Word from rx A/D Converter (MSB First)
7-0	Reserved	Set All Bits Always to 0	Reserved for Future Use

TABLE VII. rx Data Format.

Digital Data Scale

The digital input and output data is coded in Binary Two's complement with 16 bits; the scale is shown in Table VIII.

ANALOG INPUT	A/D CONVERTER DATA
	MSB LSB
Positive Full Scale	0111111111111111
Mid Scale	0000000000000000
Negative Full Scale	1000000000000000

TABLE VIII. Digital Input/Output Data Scale.

Sampling Phase

The DSP will determine the sampling phase used for the AFE1230. In the case of a phase jump (i.e.: when the rxBaud or txBaud symbol clocks move one MCLK period forward or backward, resulting in 49 or 47 MCLK cycles per rxBaud), the receive data will be invalid for six symbol periods while the data settles to the final value.

Loop Back

The AFE1230 includes digital and analog loop-back options, as shown in Table IX.

Echo Cancellation in the AFE1230

The rxHYB input is designed to be subtracted from the rxLINE input for first-order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (+ to + and – to –), while the rxHYB input is connected to opposite polarity through the compromise hybrid (– to + and + to –).

LOOPBACK	OPERATION
Loopback = 00	Normal Operation
Loopback = 01	Digital Loopback: Data In is Shortened to Data Out.
Loopback = 10	Analog Loopback: The rxLINE inputs are shortened to V_{CM}, while the transmit and rxHYB inputs are connected normally.
Loopback = 11	Analog Loopback: The rxHYB inputs are shortened to V_{CM}, while the transmit and rxLINE inputs are connected normally.

TABLE IX. Loopback Table.

APPLICATIONS

AFE1230 BASIC APPLICATION CIRCUITS

There are two basic circuits for AFE1230 evaluation and applications in this section. Figure 8 is a basic setting of a 135Ω line interface circuit, used to test the basic transmit and receive functions as well as uncancelled echo of the AFE1230. In the circuit, R_1 and R_2 are used to control far-end reflection and maximize the energy exchange between the transmitter and loop. The value of R_1 and R_2, (see Figure 8), is designed to match a 135Ω line with turns ratio of 1:3.7 (device:line) transformer from Midcom (51185 Rev6A). R_4 and R_6 are line input resistors; 10kΩ is a suggested value. R_3 and R_5 are hybrid input resistors that control the echo cancellation. The two 53nF capacitors are used for external transmit low-pass filters with a cutoff frequency about 600kHz.

When Figure 8 is used for uncancelled echo test, it provides total noise measurement of AFE1230 transmit and receive paths (this includes linearity error, distortion, and noise). The measurement of uncancelled echo is made as follows: the AFE1230 is connected to the external circuit (see Figure 8) and the hybrid resistors can be different values. The line is simulated by a 135Ω resistor. A symbol sequence is generated by the tester and sent to both the AFE1230 and an external adaptive filter. The symbol sequence through the transmit path is then loopbacked to the hybrid input and line input. Different loopback conditions are applied in the test, such as line input disconnected, hybrid input disconnected, or 135Ω resistor shorted. The output of the adaptive filter is subtracted from the AFE1230 output to form the uncancelled echo signal. Since there is no far-end signal source, or additive line noise, the uncancelled echo contains only noise and linearity errors generated in transmit and receive channels of the AFE1230. The uncancelled echo is defined as a ratio of the rms uncancelled echo to the rms voltage of the nominal transmitted signal (for example 14.5dBm).

Figure 8 also shows a basic setting for G.SHDSL applications that can provide 14.5dBm power directly to a 135Ω line. The typical performance is listed in Table X. A power spectrum density of a random sequence through this circuit with 30M bit rate is shown in Figure 9.

PARAMETER	VALUE
Line Power	14.5dBm
Line Peak-to-Peak Voltage	11.7V
PAR	3.0 (Vp/Vrms)
Line Termination Resistance	135Ω
Transformer Turns Ratio	1:3.7
AFE1230 Output Peak-to-Peak Voltage	6.2Vp-p (Differential)
External tx Low-Pass Filter Cutoff Frequency	≅ 600kHz
External rx Low-Pass Filter (Optional) Cutoff Frequency	≅ 600kHz

TABLE X. Typical Performance for G.SHDSL Circuit, Shown in Figure 8.

Figure 10 is a basic application circuit with an external driver (OPA2677) to provide 17.3dBm power on a 135Ω loop for HDSL2 transmission. The analog signal from the AFE1230 has 6.2V peak-to-peak voltage and is loaded by a 1kΩ resistor. The OPA2677 is configured as a wideband power amplifier with a constant AC gain of 2.8V and 17.3V peak-to-peak output voltage. The output signal from the OPA2677 is filtered to minimize noise by a tx RC low-pass filter with a cutoff frequency of 600kHz. A 1:2.3 transformer from Midcom (51440R Rev00) is used. The receive amplifier receives far-end signals from the line through the line transformer with 2.3 times of step down. The line input resistors of the AFE1230 are set to 10kΩ. The basic resistor network hybrid circuit is used to isolate transmit signals from receivers. The receive low-pass filter (optional) performs bandlimit to the receive signal to minimize aliasing. Table XI gives the line interface basic performance for HDSL2.

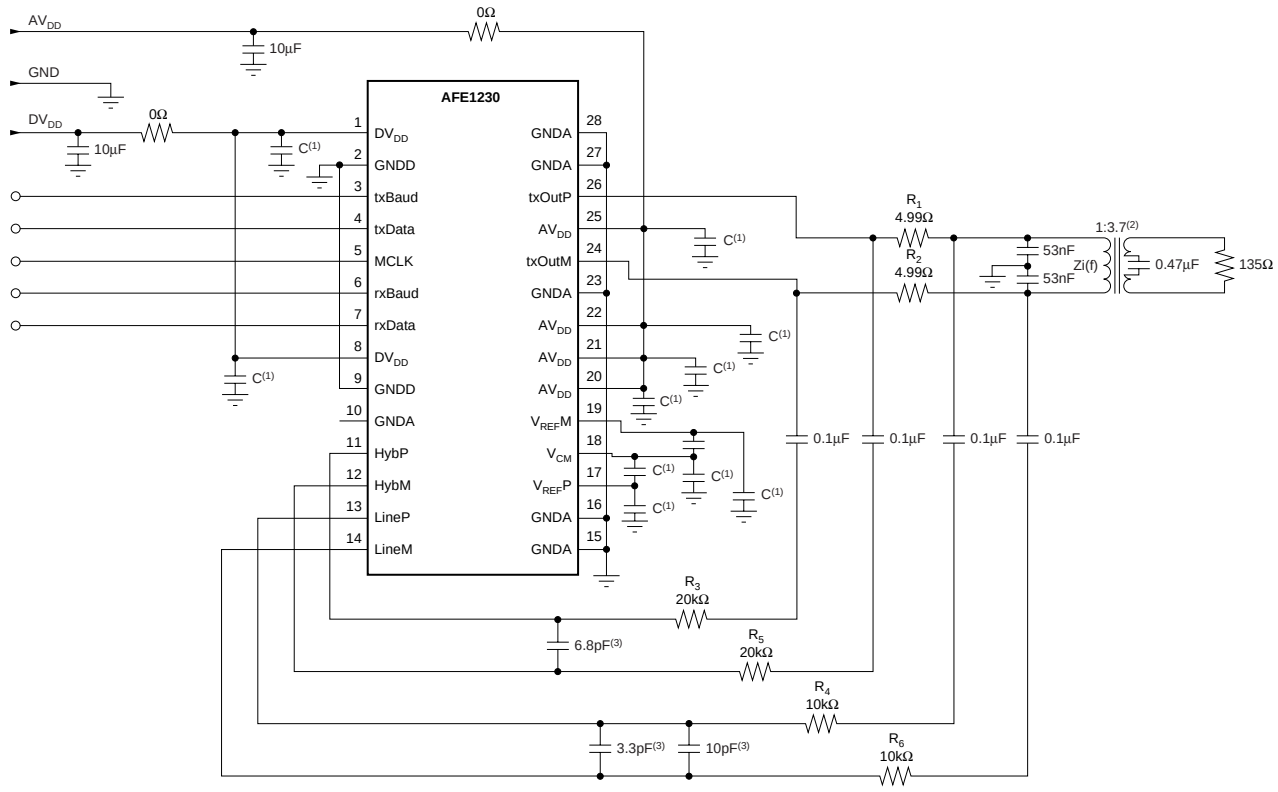
PARAMETER	VALUE
Line Power	16.8 ± 0.5dBm
PAR	4 (Vp/Vrms)
Line Termination Resistance	135Ω
Transformer Turns Ratio	1:2.3
External Driver	OPA2677
OPA2677 Power Supply	+12V
DC Gain	1(v/v)
AC Gain (R Can Be Adjusted)	2.8 (v/v)
AFE1230 Peak-to-Peak Output Voltage	6.2Vp-p (Differential)
OPA2677 Peak-to-Peak Output Voltage	17.3V (Differential)
AFE1230 Power Dissipation	560mW
Transmit Low-Pass Filter Cutoff Frequency	≅ 600kHz
Receive Low-Pass Filter (Optional) Cutoff Frequency	≅ 600kHz

TABLE XI. Typical Performance for HDSL2 Circuit, (See Figure 10).

In practice, the line impedance is changed with frequency under the different loop conditions. An RC or RLC compromise network is generally inserted in the external hybrid path to track the impedance over the frequency band interested. The components of the compromise networks are adjustable for minimizing far-end, near-end, and trans-hybrid reflections. The coupling capacitance (0.1µF) on the tx and rx paths is used for AFE evaluation only. With the DSL external hybrid circuit, this capacitance should be adjusted.

AFE1230 Power Dissipation

When using the on-chip driver at E1 rates, 3.3V digital power supply (5V analog power supply) for G.SHDSL operation, with 14.5dBm power to the line, the AFE1230 power dissipation including both analog and digital circuitry is about 750mW. Most power dissipation on the chip is in the on-chip driver and other analog circuitry (about 120mW power dissipation is from digital circuitry). Digital power dissipation is reduced when the operating frequency decreases, but the analog power dissipation stays the same with the frequency changing. When an external driver (OPA2677) is used, the power dissipation of the AFE1230 is about 560mW.



NOTES: (1) C = 0.1µF (Ceramic SMT). (2) Transformer = Midcom—51185. (3) These components provide low-pass filtering to the input signal and are optional, since the AFE1230 provides an internal low-pass filter with 1MHz cutoff frequency on the front end of the receiver, as well as oversampling by the A/D converter.

FIGURE 8. AFE1230 Line Interface with 14.5dBm Line Power for G.SHDSL.

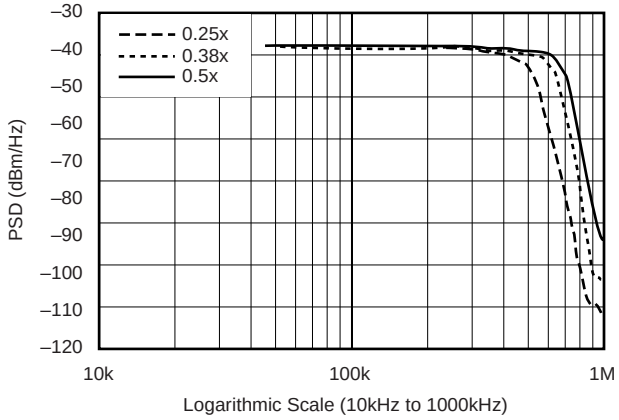
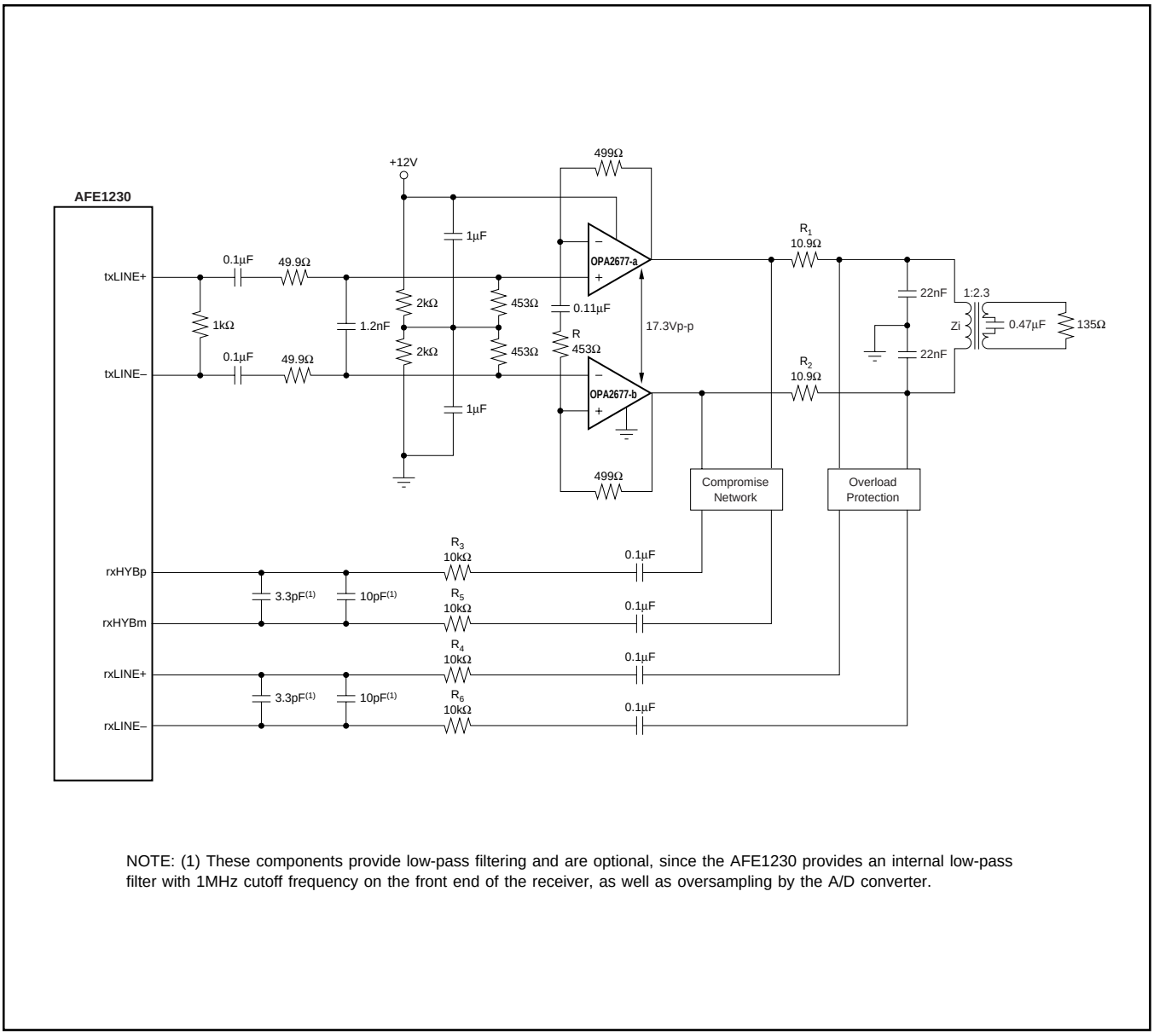


FIGURE 9. AFE1230 Transmit PSD with 30MHz of Master Clock, Seventh-Order tx Filter and Cutoff Frequency Ratio of 0.5x, 0.38x, and 0.25x.



NOTE: (1) These components provide low-pass filtering and are optional, since the AFE1230 provides an internal low-pass filter with 1MHz cutoff frequency on the front end of the receiver, as well as oversampling by the A/D converter.

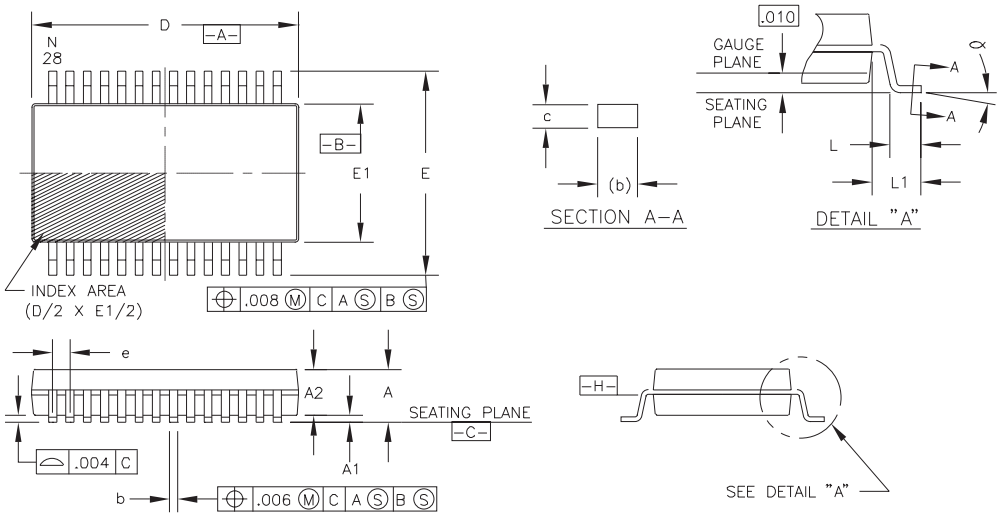
FIGURE 10. AFE1230 Line Interface with OPA2677 for HDSL2.

LAYOUT

The AFE1230 has two conflicting requirements: it must accept and deliver high-speed digital signals and it must generate, drive, and convert precision analog signals. To achieve optimal system performance with the AFE1230, both the digital and the analog sections must be treated carefully in board layout design. The power supply for the digital section of AFE1230 can range from 3.3V to 5V. This supply should be decoupled to digital grounds with ceramic 0.1µF capacitors placed as close to the GNDD and DV_{DD} pins as possible. DV_{DD} may be supplied by a wide-printed circuit board trace. A digital ground plane underneath all digital pins is strongly recommended. All GNDA pins should be connected directly to a common analog ground plane and all the AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to power supply. The analog power-supply pins should be decoupled to analog grounds with ceramic 0.1µF capacitors placed as close to the AFE1230 as possible. One 10µF tantalum capacitor should be used between the analog supply and analog ground. Ideally, all ground planes and traces and all power planes and traces should return to the power connector before being connected together (if necessary). Each ground and power pair should be routed over each other, and should not overlay any portion of another pair, and the pairs should be separated by a distance of 0.25 inches (6mm) at least. One exception is that the digital and analog ground planes should be connected together underneath the AFE1230 by a small trace.

PACKAGE DRAWING

Package Number 324 - 28-Lead Plastic SSOP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.079	--	2.00	
A1	.002	--	0.05	--	
A2	.065	.073	1.65	1.85	
b	.009	.015	0.22	0.38	3,7
c	.004	.010	0.09	0.25	7
D	.390	.413	9.90	10.50	2
E	.291	.323	7.40	8.20	
E1	.196	.220	5.00	5.60	2
e	.0256 BASIC		0.65 BASIC		
L	.022	.037	0.55	0.95	4
L1	.049 REF		1.25 REF		
N	28		28		5
θ	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. D AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE -H- MOLD PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .008 INCH PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN .003 INCH AT LEAST MATERIAL CONDITION.
4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
5. N IS THE NUMBER OF TERMINAL POSITIONS.
6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: ZZ324	REV.: C
JEDEC NUMBER: MO-150	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AFE1230E	ACTIVE	SSOP	DB	28	48	None	CU SNPB	Level-3-220C-168 HR
AFE1230E/1K	ACTIVE	SSOP	DB	28	1000	None	CU SNPB	Level-3-220C-168 HR
AFE1230E/1KG4	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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