3A, 2MHz Monolithic Synchronous Regulator for DDR/QDR Memory Termination

FEATURES

- **High Efficiency: Up to 90%**
- **±3A Output Current**
- **Symmetrical Source and Sink Output Current Limit**
- **Low $R_{DS(ON)}$ Internal Switch: 85mΩ**
- No Schottky Diode Required
- 2.25V to 5.5V Input Voltage Range
- $V_{OUT} = V_{REF}/2$
- ±1% Output Voltage Accuracy
- Programmable Switching Frequency: Up to 2MHz
- Power Good Output Voltage Monitor
- Overtemperature Protected
- Available in 16-Lead TSSOP Exposed Pad Package

APPLICATIONS

- Bus Termination: DDR and QDR™ Memory, SSTL, HSTL, ...
- Notebook Computers
- Distributed Power Systems

DESCRIPTION

The LTC®3413 is a high efficiency monolithic synchronous step-down DC/DC converter utilizing a constant frequency, current mode architecture. It operates from an input voltage range of 2.25V to 5.5V and provides a regulated output voltage equal to (0.5)V_{REF} while sourcing or sinking up to 3A of output current. An internal voltage divider reduces component count and eliminates the need for external resistors by dividing the reference voltage in half. The internal synchronous power switch with 85mΩ on-resistance increases efficiency and eliminates the need for an external Schottky diode. Switching frequencies up to 2MHz are set by an external resistor.

Forced-continuous operation in the LTC3413 reduces noise and RF interference. Fault protection is provided by an overcurrent comparator that limits output current during both sourcing and sinking operations. Adjustable compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress Semiconductor, Hitachi, IDT, Micron Technology, Inc. and Samsung.

TYPICAL APPLICATION

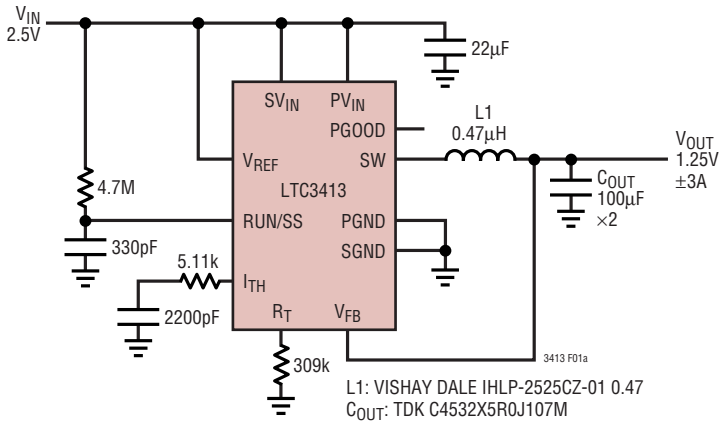


Figure 1a. High Efficiency Bus Termination Supply

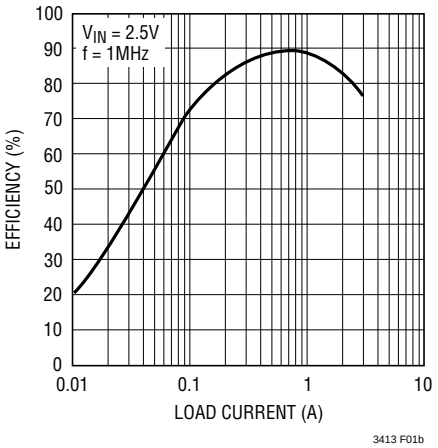


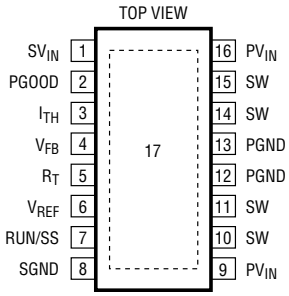
Figure 1b. Efficiency vs Load Current

ABSOLUTE MAXIMUM RATINGS

(Note 1)

SV_{IN}, PV_{IN} Supply Voltages ..... –0.3V to 6V
I_{TH}, RUN/SS, V_{FB}, PGOOD Voltages ..... –0.3V to V_{IN}
V_{REF} Voltage ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Peak SW Sink and Source Current 7.2A
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Notes 5, 8) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 17)
MUST BE SOLDERED TO SGND

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER
LTC3413EFE
FE PART MARKING
3413EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range			2.25		5.5	V
V_{FB}	Feedback Voltage Accuracy	(Note 3)	●			±1	%
I_{FB}	Voltage Feedback Leakage Current					0.4	µA
I_{RUN}	RUN/SS Leakage Current					1	µA
ΔV_{FB}	Feedback Voltage Line Regulation	V_{IN} = 2.7V to 5.5V (Note 3)	●		0.04	0.2	%/V
$V_{LOADREG}$	Feedback Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 0.36V Measured in Servo Loop, V_{ITH} = 0.84V	● ●		0.02 –0.02	0.2 –0.2	% %
ΔV_{PGOOD}	Power Good Range				±10	±12	%
R_{PGOOD}	Power Good Pull-Down Resistance				120	200	Ω
I_Q	Input DC Bias Current Active Current Shutdown	(Note 4) V_{FB} = 1.5V, V_{ITH} = 1.4V, V_{REF} = 2.5V V_{RUN} = 0V (Note 7)			 250 0.02	 330 1	 µA µA
f_{OSC}	Switching Frequency Switching Frequency Range	R_{OSC} = 309k (Note 6)		0.88 0.30	1.00	1.12 2.00	MHz MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 300mA			85	110	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = 300mA			65	90	mΩ
I_{LIMIT}	Peak Current Limit			3.8	5.4		A
V_{UVLO}	Undervoltage Lockout Threshold			1.75	2	2.25	V
I_{LSW}	SW Leakage Current	V_{RUN} = 0V, V_{IN} = 5.5V (Note 7)			0.1	1	µA
V_{RUN}	RUN Threshold			0.5	0.65	0.8	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3413E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3413E is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows: LTC3413E: $T_J = T_A + (P_D \bullet 38°C/W)$

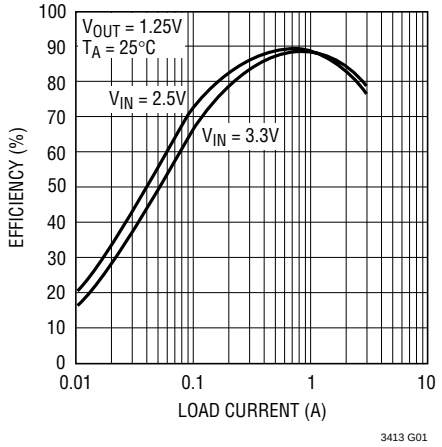
Note 6: 2MHz operation is guaranteed by design and not production tested.

Note 7: Shutdown current and SW leakage current are only tested during wafer sort.

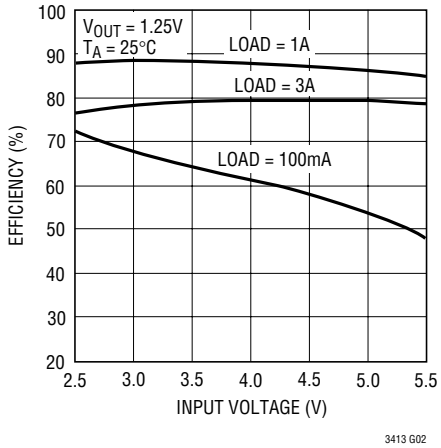
Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

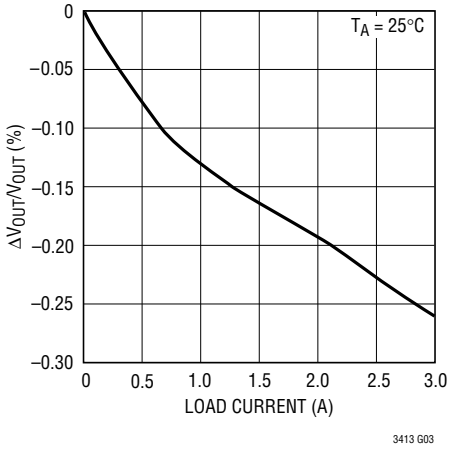
Efficiency vs Load Current



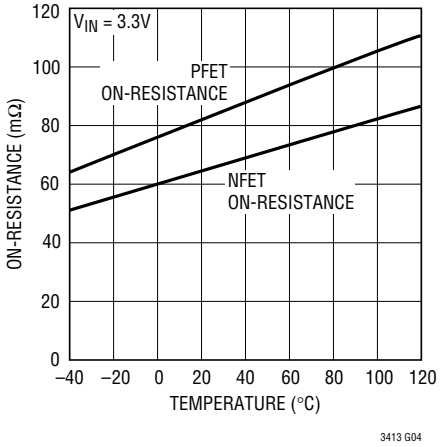
Efficiency vs Input Voltage



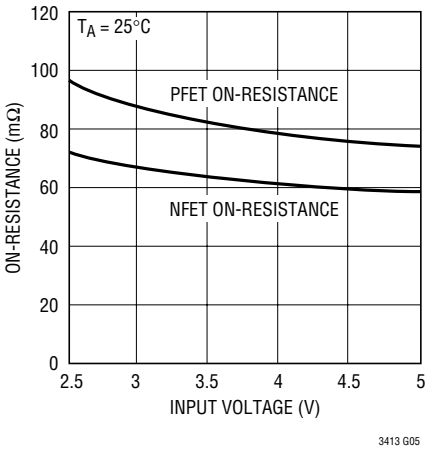
Load Regulation



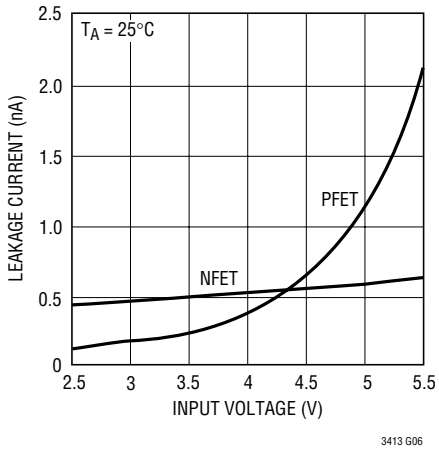
Switch On-Resistance vs Temperature



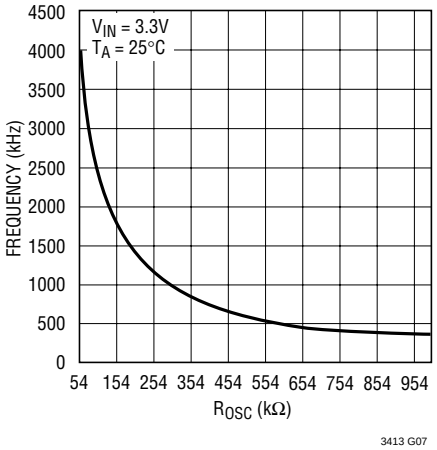
Switch On-Resistance vs Input Voltage



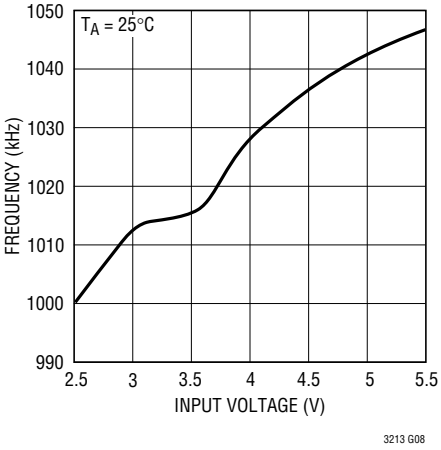
Switch Leakage vs Input Voltage



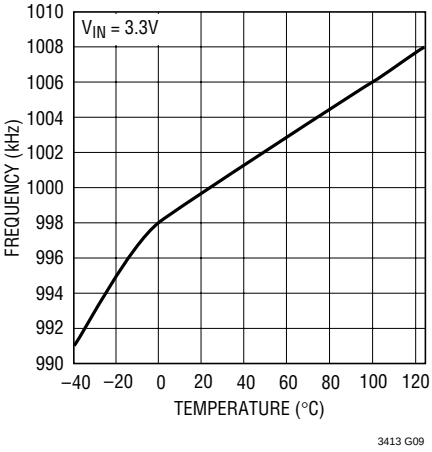
Frequency vs R_{OSC}



Frequency vs Input Voltage

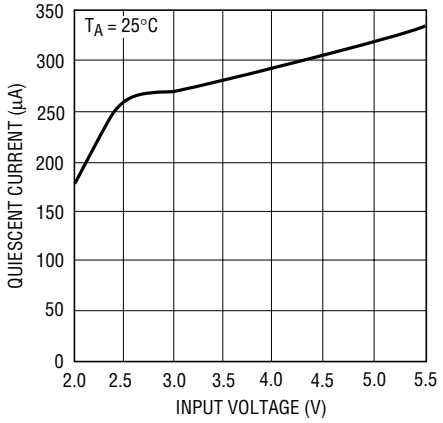


Frequency vs Temperature



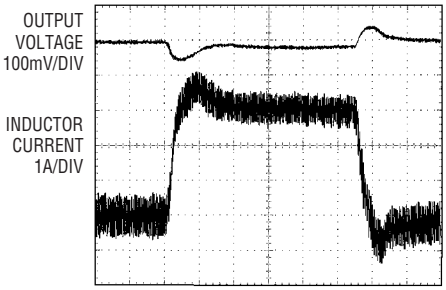
TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current vs Input Voltage



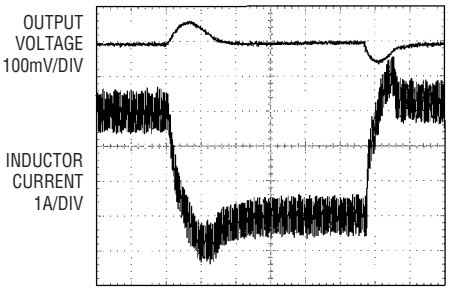
3413 G10

Load Step Transient



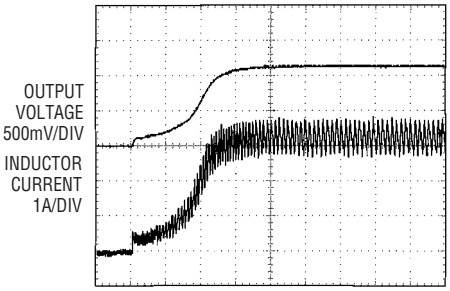
V_{IN} = 2.5V 20µs/DIV 3413 G11
V_{OUT} = 1.25V
LOAD STEP = 0A TO 3A

Load Step Transient



V_{IN} = 2.5V 20µs/DIV 3413 G12
V_{OUT} = 1.25V
LOAD STEP = 0A TO –3A

Start-Up



V_{IN} = 2.5V 1ms/DIV 3413 G13
V_{OUT} = 1.25V
LOAD = 0.4Ω

PIN FUNCTIONS

SV_{IN} (Pin 1): Signal Input Supply. Decouple this pin to SGND with a capacitor. SV_{IN} must be greater or equal to PV_{IN}, however, the difference between SV_{IN} and PV_{IN} must be less than 0.5V.

PGOOD (Pin 2): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of regulation point.

I_{TH} (Pin 3): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.2V to 1.4V with 0.6V corresponding to the zero-sense voltage (zero current).

V_{FB} (Pin 4): Feedback Pin. Receives the feedback voltage from the output.

R_T (Pin 5): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

V_{REF} (Pin 6): Reference Voltage Input. The positive input of the internal error amplifier senses one-half of the voltage at this pin through a resistor divider.

RUN/SS (Pin 7): Run Control and Soft-Start Input. Forcing this pin below 0.5V shuts down the LTC3413. In shutdown all functions are disabled drawing < 1μA of supply current. A capacitor to ground from this pin sets the ramp time to full output current.

SGND (Pin 8): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

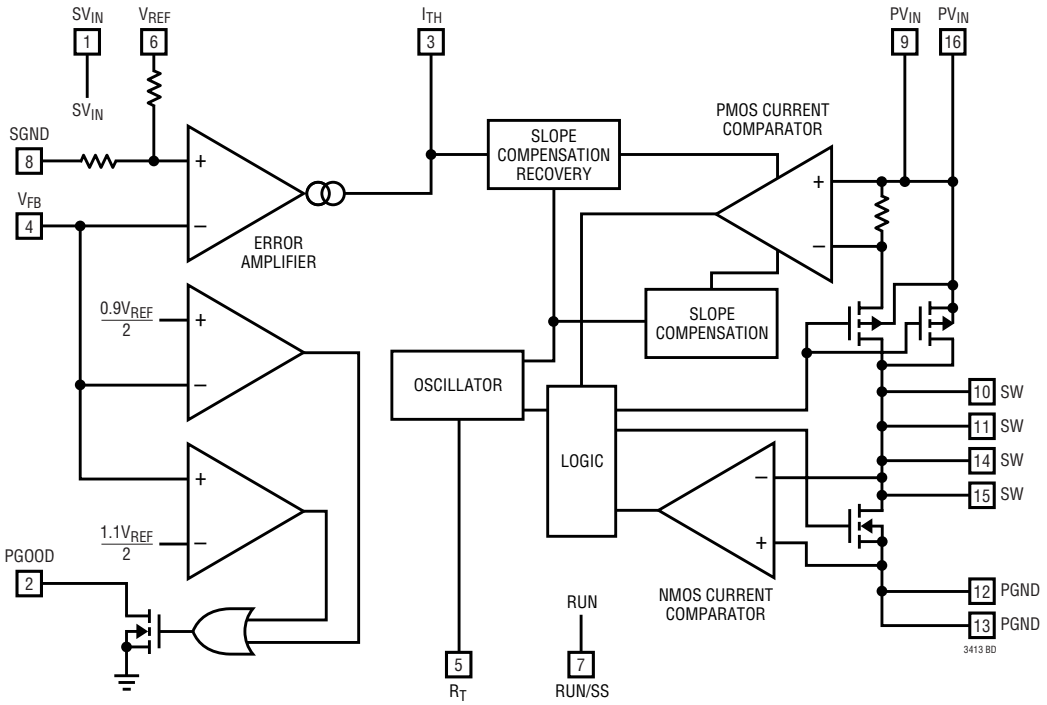
PV_{IN} (Pins 9, 16): Power Input Supply. Decouple this pin to PGND with a capacitor.

SW (Pins 10, 11, 14, 15): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

PGND (Pins 12, 13): Power Ground. Connect this pin closely to the (–) terminal of C_{IN} and C_{OUT}.

EXPOSED PAD (Pin 17): Should be connected to SGND.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3413 is a monolithic, constant frequency, current mode step-down DC/DC converter that is capable of sourcing and sinking current at the output. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the I_{TH} pin. The error amplifier adjusts the voltage on the I_{TH} pin by comparing the feedback signal on the V_{FB} pin with a reference voltage that is equal to one-half of the voltage on the V_{REF} pin. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the I_{TH} voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –7A.

The operating frequency is set by an external resistor connected between the R_T pin and ground. The switching frequency can range from 300kHz to 2MHz.

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±10%. In an overvoltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3413 is designed to operate down to an SV_{IN} input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3413 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3413, however, slope compensation recovery is implemented to keep the maximum inductor peak current constant throughout the range of duty cycles.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current increases greater than 5A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

APPLICATIONS INFORMATION

The basic LTC3413 application circuit is shown in Figure 1a. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3413 is determined by an external resistor that is connected between pin R_T and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation.

$$R_{OSC} = \frac{3.23 \bullet 10^{11}}{f}(\Omega) - 10k\Omega$$

Although frequencies as high as 2MHz are possible, the minimum on-time of the LTC3413 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 • 110ns • f (Hz).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} or V_{OUT} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are used often at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

APPLICATIONS INFORMATION

Table 1 shows some recommended surface mount inductors for LTC3413 applications.

Table 1. Recommended Surface Mount Inductors

Manufacturer	Part Number	Value (μH)	DCR (mΩ)
Murata	LQH55DNR47M01	0.47	13.0
Vishay/Dale	IHLP2525CZPJR47M01	0.47	4.2
Pulse	P1166.681T	0.44	6.0
Cooper	SD20-R47	0.47	20.0

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the source of the top MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies.

Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These

APPLICATIONS INFORMATION

dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

In most applications, V_{OUT} is connected directly to V_{FB}. The output voltage will be equal to one-half of the voltage on the V_{REF} pin for this case.

$$V_{OUT} = \frac{V_{REF}}{2}$$

If a different output voltage relationship is desired, an external resistor divider from V_{OUT} to V_{FB} can be used. The output voltage will then be set according to the following equation:

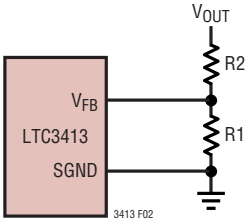


Figure 2. Setting the Output Voltage

$$V_{OUT} = \frac{V_{REF}}{2}\left(1+\frac{R2}{R1}\right)$$

Soft-Start

The RUN/SS pin provides a means to shut down the LTC3413 as well as a timer for soft-start. Pulling the RUN/SS pin below 0.5V places the LTC3413 in a low quiescent current shutdown state ($I_Q < 1\mu A$).

The LTC3413 contains an internal soft-start clamp that gradually raises the clamp on I_{TH} after the RUN/SS pin is pulled above 2V. The full current range becomes available on I_{TH} after 1024 switching cycles. If a longer soft-start period is desired, the clamp on I_{TH} can be set externally with a resistor and capacitor on the RUN/SS pin as shown in Figure 1a. The soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS} \bullet C_{SS} \ln\left(\frac{V_{IN}}{V_{IN} - 1.8V}\right) \text{(Seconds)}$$

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from

APPLICATIONS INFORMATION

high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3413 does not dissipate much heat due to its high efficiency.

But, in applications where the LTC3413 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3413 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3413 in dropout at an input voltage of 3.3V, a load current of 3A and an ambient temperature of 70°C. From the Typical Performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 97mΩ. Therefore, power dissipated by the part is:

$$P_D = (I_{LOAD}^2)(R_{DS(ON)}) = (3A)^2(97m\Omega) = 0.87W$$

For the TSSOP package, the θ_{JA} is 38°C/W. Thus the junction temperature of the regulator is:

$$T_J = 70°C + (0.87W)(38°C/W) = 103°C$$

which is below the maximum junction temperature of

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125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components and output capacitor shown in Figure 1a will provide adequate compensation for most applications.

Output Voltage Tracking of V_{REF}

For applications in which the V_{REF} pin is connected to the V_{IN} pin, the output voltage will be equal to one-half of the voltage on the V_{IN} pin. Because the output voltage will track the input voltage, any disturbance on V_{IN} will appear on V_{OUT}. For example, a load step transient could cause the input voltage to drop if there is insufficient bulk capacitance at the V_{IN} pin. The corresponding drop in the output voltage during the load step transient is caused by the V_{OUT} tracking of V_{IN} and should not be confused with poor load regulation.

Design Example

As a design example, consider using the LTC3413 in an application with the following specifications: V_{IN} = 2.5V, V_{OUT} = 1.25V, $I_{OUT(MAX)}$ = ±3A, f = 1MHz.

First, calculate the timing resistor:

$$R_{OSC} = \frac{3.23 \bullet 10^{11}}{1 \bullet 10^{6}} - 10k\Omega = 313k\Omega$$

Use a standard value of 309k. Next, calculate the inductor value for about 40% ripple current:

$$L = \left(\frac{1.25V}{1MHz \bullet 1.2A}\right)\left(1 - \frac{1.25V}{2.5V}\right) = 0.47\mu H$$

Using a 0.47µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{1.25V}{1MHz \bullet 0.47\mu H}\right)\left(1 - \frac{1.25V}{2.5V}\right) = 1.33A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100µF ceramic capacitors will be used. C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 3A\left(\frac{1.25V}{2.5V}\right)\sqrt{\frac{2.5V}{1.25V} - 1} = 1.5A_{RMS}$$

Decoupling the PV_{IN} pins with two 100µF capacitors is

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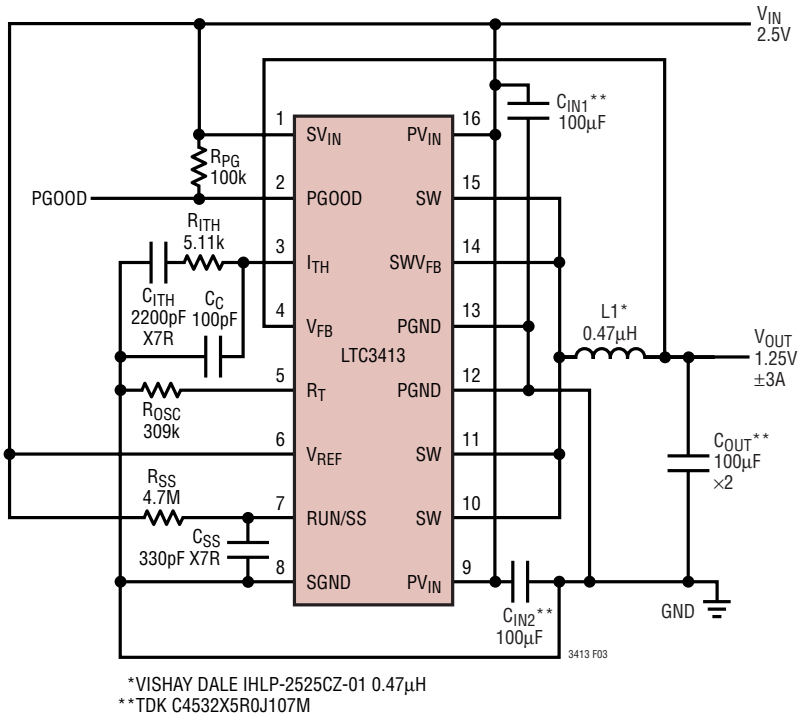


Figure 3. One-Half V_{REF}, ±3A DDR Memory Termination Supply at 1MHz (Efficiency Curve is Shown in Figure 1b)

adequate for most applications. Connect the V_{REF} pin directly to SV_{IN}. Connecting the V_{FB} pin directly to V_{OUT} will set the output voltage equal to one-half of the voltage on the V_{REF} pin. The complete circuit for this design example is illustrated in Figure 3.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3413. Check the following in your layout.

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3413.

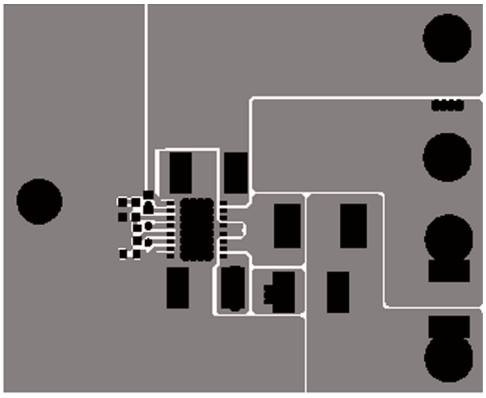
2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.

3. Keep the switching node, SW, away from all sensitive small-signal nodes.

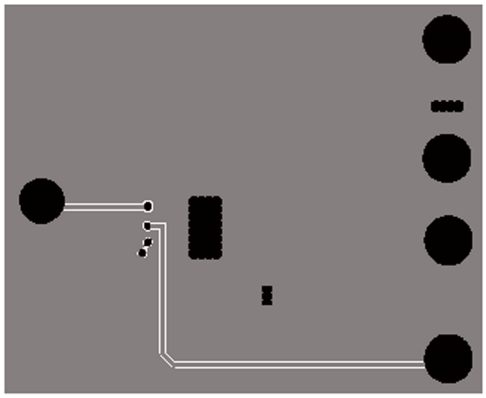
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (PV_{IN}, SV_{IN}, V_{OUT}, PGND, SGND or any other DC rail in your system).

5. Connect the V_{FB} pin directly to the V_{OUT} pin.

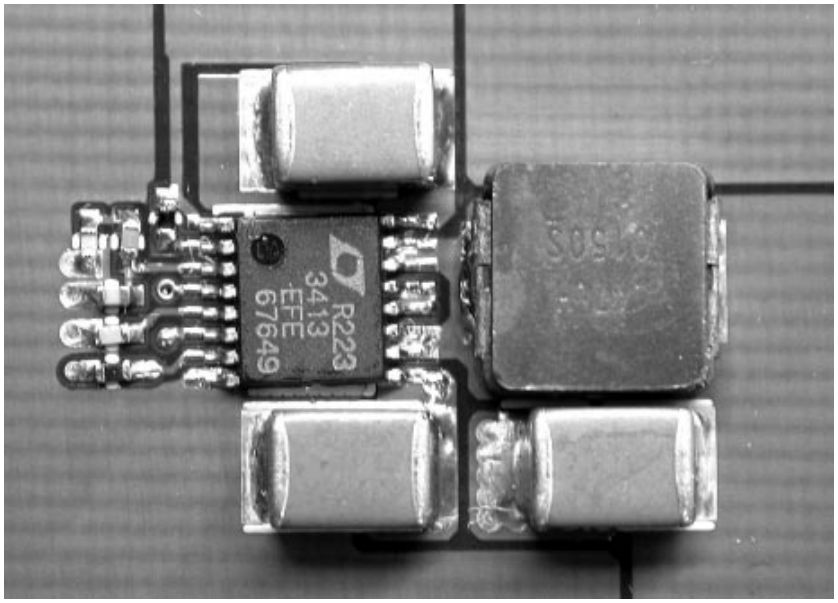
APPLICATIONS INFORMATION



(4a) Top Layer



(4b) Bottom Layer

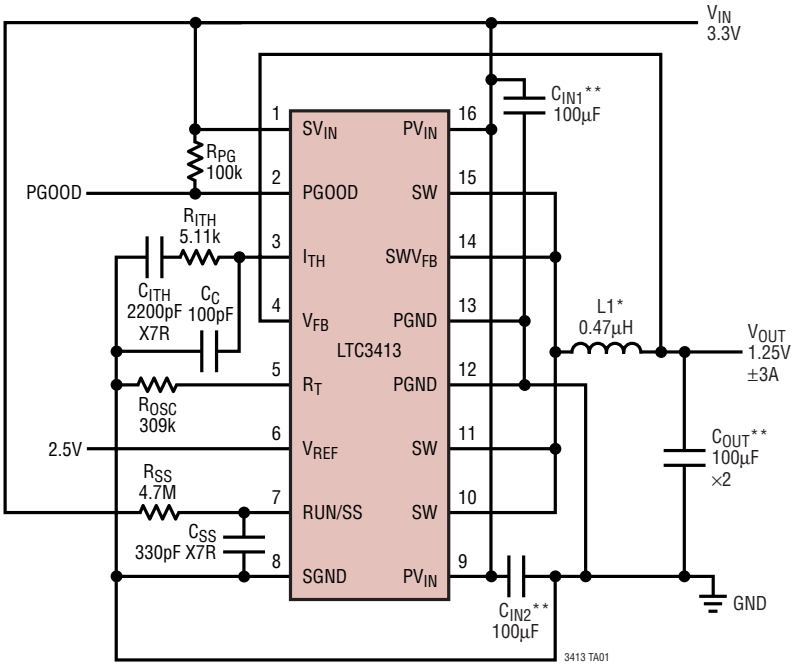


(4c) PCB Photo

Figure 4. LTC3413 Layout Diagram

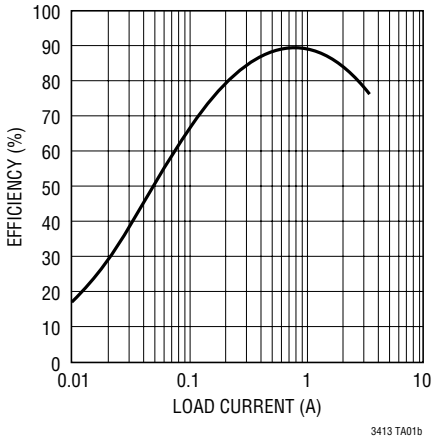
TYPICAL APPLICATION

1.25V, ±3A DDR Memory Termination Supply at 1MHz



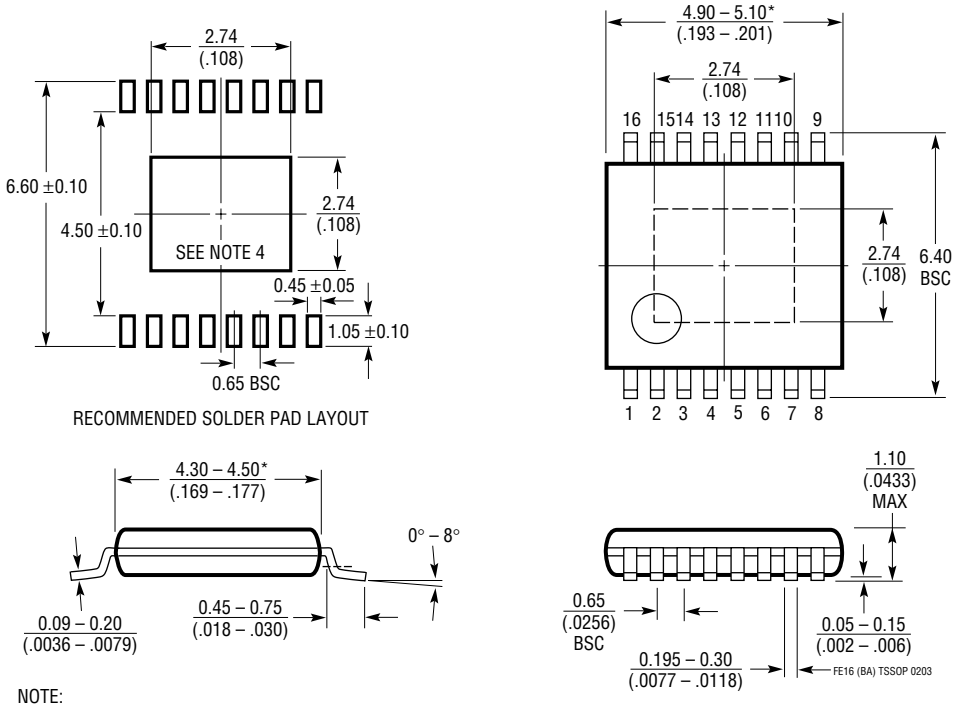
*VISHAY DALE IHLP-2525CZ-01 0.47µH
**TDK C4532X5R0J107M

Efficiency vs Load Current, V_{IN} = 3.3V, V_{OUT} = 1.25V, f = 1MHz



PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663,
Exposed Pad Variation BA)



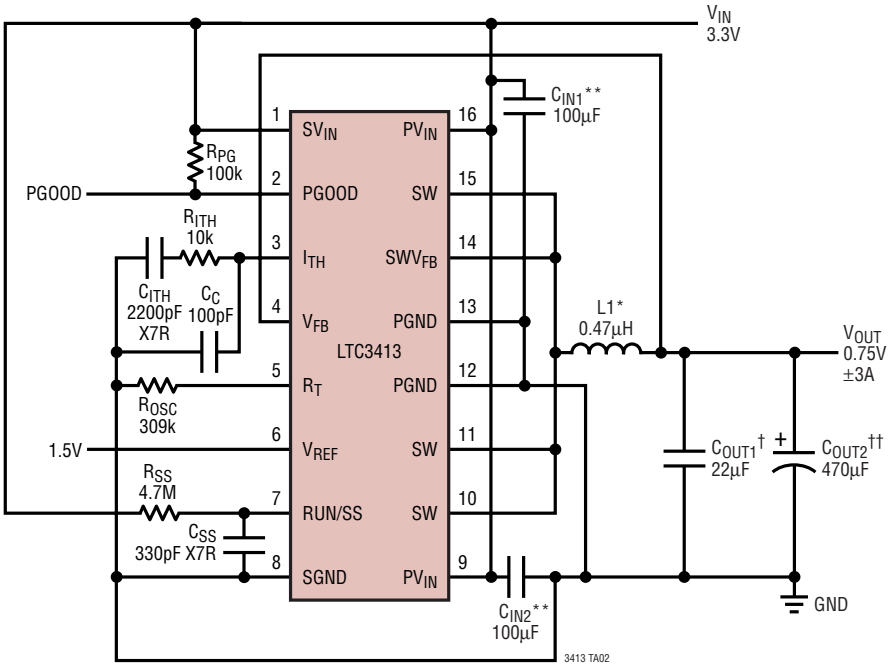
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

3.3V to 0.75V, ±3A HSTL Application



*VISHAY DALE IHLP-2525CZ-01 0.47µH
**TDK C4532X5R0J107M
†TAIYO YUDEN JMK325BJ226MM
††SANYO POSCAP 4TPD470M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3406	600mA, (I_{OUT}) 1.5MHz Synchronous Step-Down Regulator	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q: 20µA, ThinSOT
LTC3407	Dual 600mA, (I_{OUT}) 1.5MHz, Synchronous Step-Down Regulator	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q: 40µA, MS10E
LTC3411	1.25A, (I_{OUT}) 4MHz, Monolithic Synchronous Step-Down Regulator	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 60µA, MS, DFN-10
LTC3412	2.5A, (I_{OUT}) 4MHz, Monolithic Synchronous Step-Down Regulator	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 60µA, TSSOP-16
LTC3414	4A, (I_{OUT}) 4MHz, Monolithic Synchronous Step-Down Regulator	V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 64µA, TSSOP-20E
LTC3713	Low Input Voltage, No R_{SENSE}™ Synchronous Controller	V_{IN}: 1.5V to 10V, $V_{OUT(MIN)}$: 0.8V, SSOP-24
LTC3717	No R_{SENSE} Controller for DDR Memory Termination	V_{IN}: 5V to 36V, $V_{OUT(MIN)}$: 0.8V, SSOP-24
LTC3718	Low Input Voltage, No R_{SENSE} Controller for DDR Memory Termination	V_{IN}: 1.5V to 10V,$V_{OUT(MIN)}$: 0.8V, SSOP-24

No R_{SENSE} is a trademark of Linear Technology Corporation.

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