

January 1997

CD74FCT653, CD74FCT654

FCT Interface Logic, Octal Bus Transceivers/ Registers, Open Drain (A Side), Three-State (B Side)

Features

- Buffered Inputs
- Typical Propagation Delay:
6.8ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- CD74FCT653
 - Inverting
- CD74FCT654
 - Non-Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

**NOT RECOMMENDED
FOR NEW DESIGNS**
Use CMOS Technology

Description

The CD74FCT653 and CD74FCT654 octal bus transceivers/registers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC} . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64mA.

The CD74FCT653 is an inverting type having open drains on the A output and three state outputs on the B side. The CD74FCT654 differs only in that it is a noninverting type. These devices consist of bus transceiver circuits, D-Type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and OEBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data. The following examples demonstrate the four fundamental bus management functions that can be performed with the octal bus transceivers and registers.

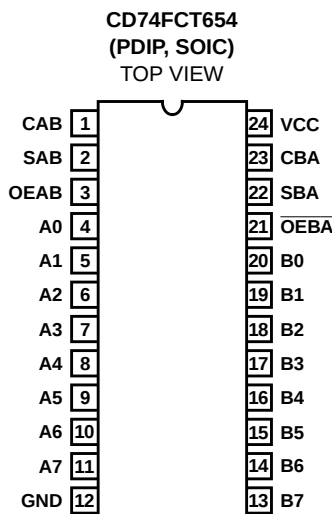
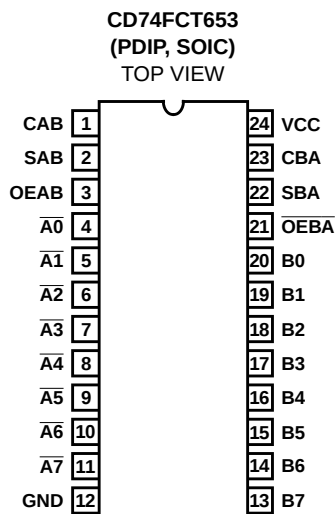
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low to high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-Type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

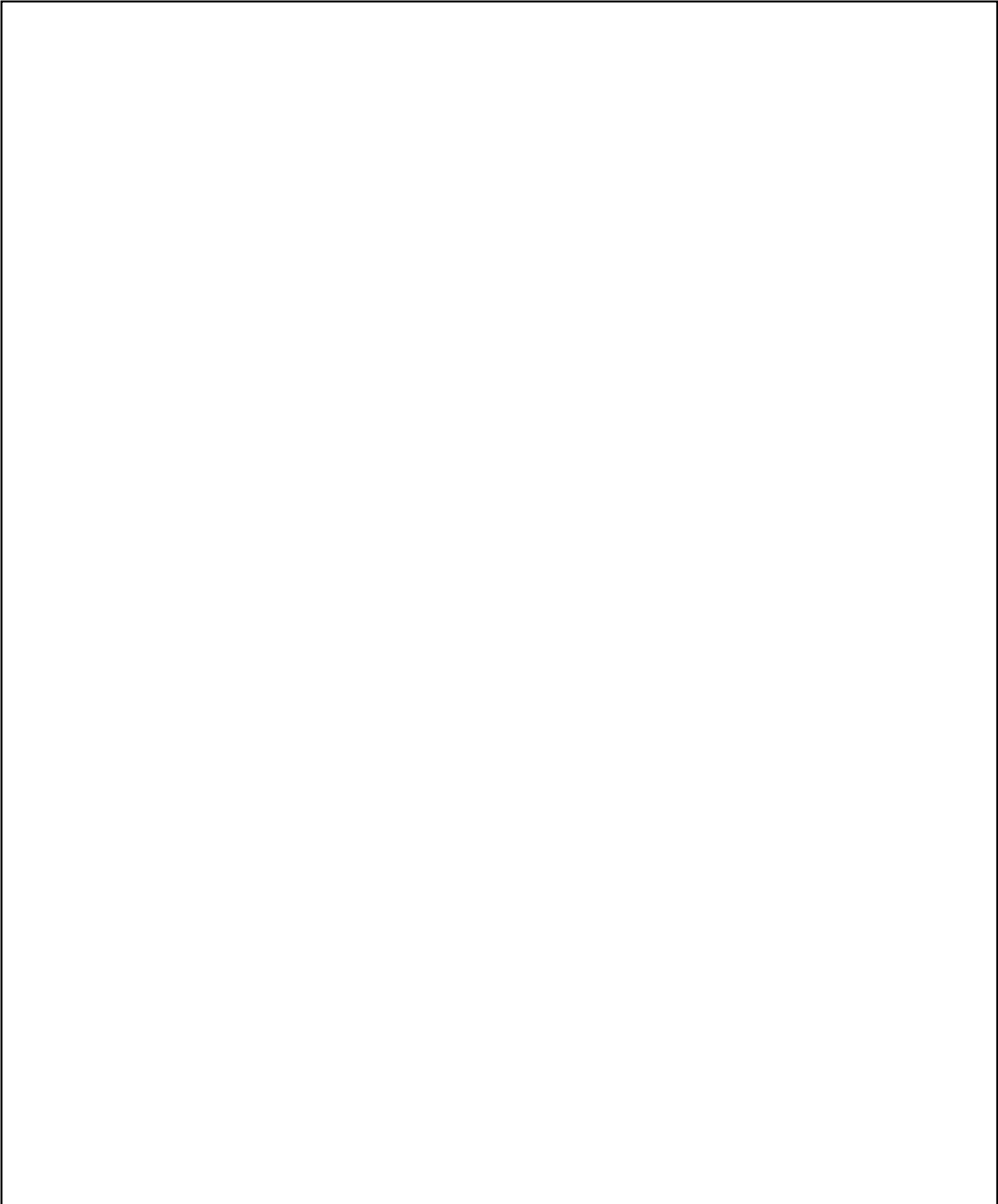
Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE	PKG. NO.
CD74FCT653EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT654EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT653M	0 to 70	24 Ld SOIC	M24.3
CD74FCT654M	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

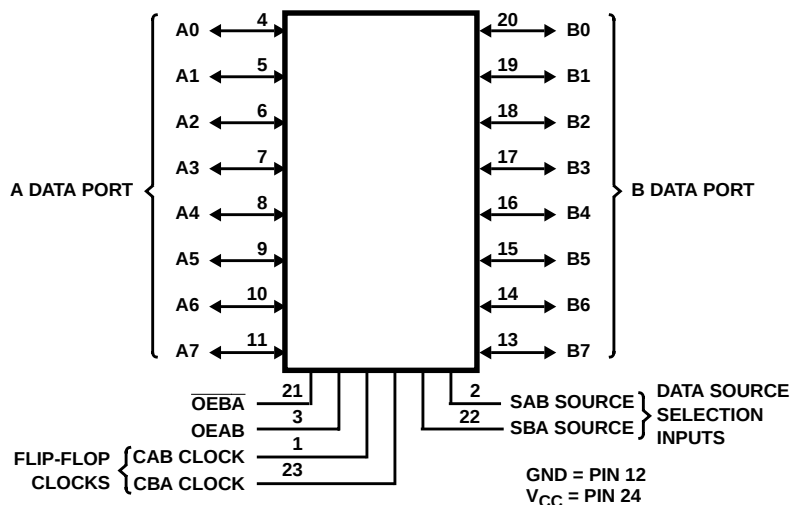
Pinouts





CD74FCT653, CD74FCT654

Functional Diagram



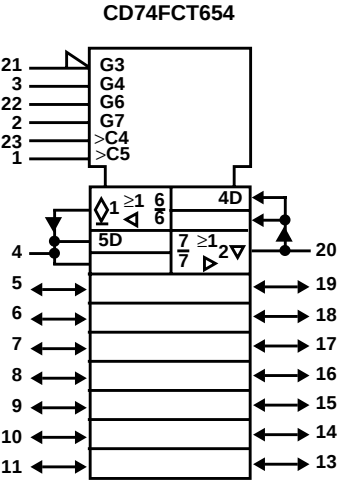
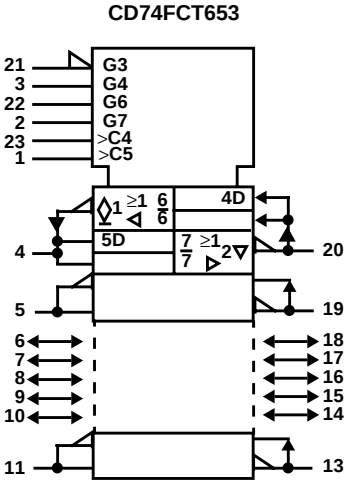
TRUTH TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	OEBA	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT653	CD74FCT654
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (2)	Store A, Hold B	Store A, Hold B
X	H	↑	↑	X (3)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (3)	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\bar{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\bar{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\bar{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\bar{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\bar{A}$ Data to B Bus	Stored A Data to B Bus
								Stored $\bar{B}$ Data to A Bus	Stored B Data to A Bus

NOTES:

1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered in order to load both registers.

IEC Logic Symbols



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Absolute Maximum Ratings

DC Supply Voltage (V_{CC})	-0.5V to 6V
DC Diode Current, I_{IK} (For $V_I < -0.5V$)	-20mA
DC Output Diode Current, I_{OK} (for $V_O < -0.5V$)	-50mA
DC Output Sink Current per Output Pin, I_O	70mA
DC Output Source Current per Output Pin, I_O	-30mA
DC V_{CC} Current (I_{CC})	140mA
DC Ground Current (I_{GND})	528mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	75
SOIC Package	75
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, V_{CC}	4.75V to 5.25V
DC Input Voltage, V_I	0 to V_{CC}
DC Output Voltage, V_O	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv	0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A)				UNITS
		V _I (V)	I _O (mA)		25°C		0°C TO 70°C		
					MIN	MAX	MIN	MAX	
High Level Input Voltage	V _{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V _{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I _{IH}	V _{CC}		Max	-	0.1	-	1	μA
Low Level Input Current	I _{IL}	GND		Max	-	-0.1	-	-1	μA
Three-State Leakage Current	I _{OZH}	V _{CC}		Max	-	0.5	-	10	μA
	I _{OZL}	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 5)	I _{OS}	V _O = 0 V _{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI _{CC}	3.4V (Note 6)		Max	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at V_{CC} or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70 $^{\circ}C$.

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Switching Specifications Over Operating Range $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figures 3, 4)

PARAMETER		SYMBOL	V _{CC} (V)	25°C	0°C TO 70°C		UNITS
				TYP	MIN	MAX	
Propagation Delays							
Stored A _n → B _n [̄]	CD74FCT653	t _{PLH} , t _{PHL}	5	6.8	2	9	ns
Stored A _n → B _n	CD74FCT654	t _{PLH} , t _{PHL}	5	6.8	2	9	ns
Stored B _n [̄] → A _n	CD74FCT653	t _{PZL}	5	6	2	8	ns
		t _{PLZ}	5	6.8	2	9	ns
Stored B _n → A _n	CD74FCT654	t _{PZL} , t _{PLZ}	5	6.8	2	9	ns
A _n → B _n [̄]	CD74FCT653	t _{PLH} , t _{PHL}	5	6	2	8	ns
A _n → B _n	CD74FCT654	t _{PLH} , t _{PHL}	5	6.8	2	9	ns
B _n [̄] → A _n	CD74FCT653	t _{PZL}	5	6	2	8	ns
		t _{PLZ}	5	6.8	2	9	ns
B _n → A _n	CD74FCT654	t _{PZL} , t _{PLZ}	5	6.8	2	9	ns
Select to Data (B Bus)	CD74FCT653, CD74FCT654	t _{PLH} , t _{PHL}	5	8.3	2	11	ns
Select to Data (A Bus)	CD74FCT653	t _{PZL}	5	6	2	8	ns
		t _{PLZ}	5	6.8	2	9	ns
Select to Data (A Bus)	CD74FCT654	t _{PZL} , t _{PLZ}	5	6.8	2	9	ns
Three-State Enabling Times (B Bus), Bus to Output or Register to Output	CD74FCT653	t _{PZL} , t _{PZH}	5	10.5	2	14	ns
	CD74FCT654	t _{PZL} , t _{PZH}	5	11.3	2	15	ns
Three-State Disabling Time (B Bus), Bus to Output or Register to Output	CD74FCT653	t _{PLZ} , t _{PZH}	5	6.8	2	9	ns
	CD74FCT654	t _{PLZ} , t _{PZH}	5	6.8	2	9	ns
Off State Enabling Times (A Bus), Bus to Output or Register to Output	CD74FCT653	t _{PZL}	5	10.5	2	14	ns
	CD74FCT654	t _{PZL}	5	11.3	2	15	ns
Off State Disabling Time (A Bus), Bus to Output or Register to Output	CD74FCT653	t _{PLZ}	5	6.8	2	9	ns
	CD74FCT654	t _{PLZ}	5	6.8	2	9	ns

Prerequisite for Switching $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figures 3, 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Maximum Frequency (B Side as Outputs)	f_{MAX}	5 (Note 8)	-	80	-	MHz
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	6	-	ns

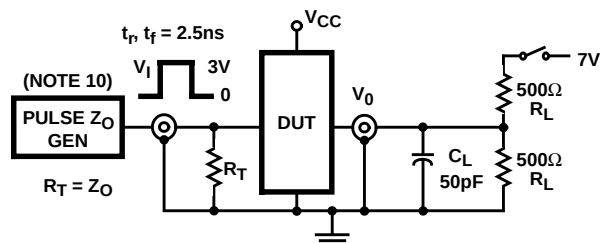
Switching $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figures 3, 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Power Dissipation Capacitance	C_{PD}	-	-	-	-	pF
Min (Valley) V_{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} (Figure 1)	5	0.5	-	-	V
Max (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance (B Side)	C_O	-	-	-	15	pF
Off-State Output Capacitance (A Side)	C_O	-	-	-	15	pF

NOTES:

8. 5V: minimum is at 4.75V for 0°C to 70°C, typical is at 5V.
9. C_{PD} , measured per flip-flop, is used to determine the dynamic power consumption. PD (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
 V_{CC} = supply voltage
 ΔI_{CC} = flow through current x unit load
 C_L = output load capacitance
 D = duty cycle of input high
 f_O = output frequency
 f_I = input frequency

Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

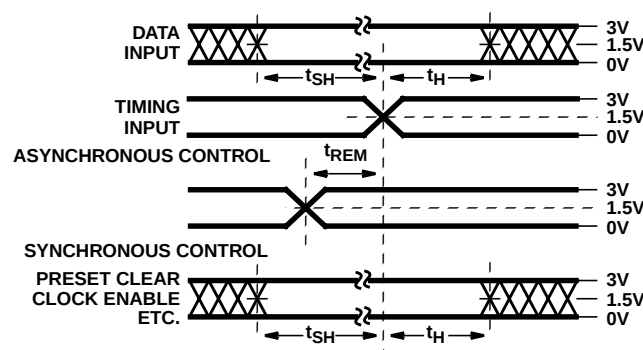


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL} , Open Drain	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

- C_L = Load capacitance, includes jig and probe capacitance.
- R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.
- $V_{IN} = 0\text{V}$ to 3V .
- Input: $t_r = t_f = 2.5\text{ns}$ (10% to 90%), unless otherwise specified

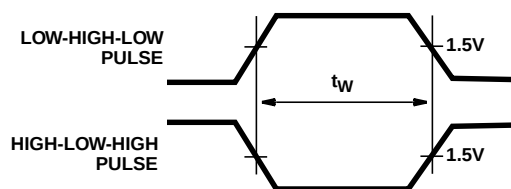


FIGURE 3. PULSE WIDTH

Test Circuits and Waveforms (Continued)

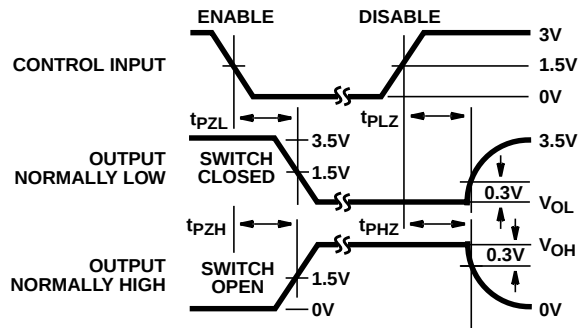


FIGURE 4. ENABLE AND DISABLE TIMING

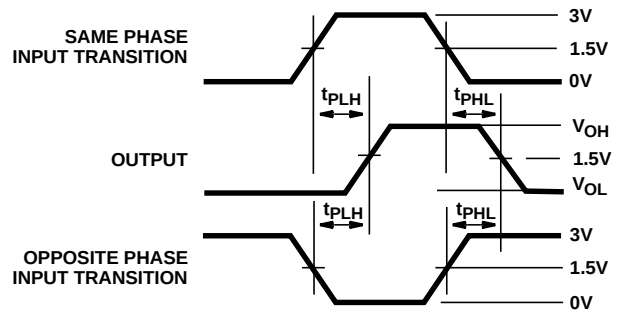
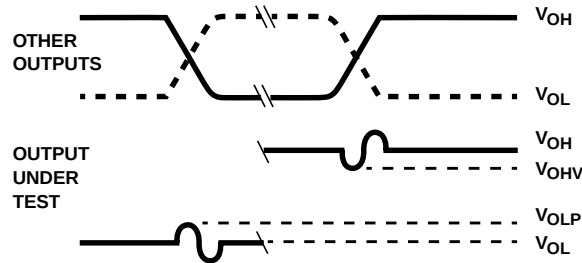


FIGURE 5. PROPAGATION DELAY



NOTES:

11. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH} .
12. Input pulses have the following characteristics:
 $P_{RR} \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns .
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

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