



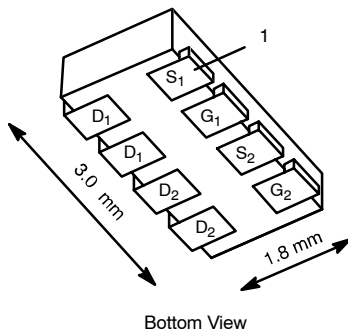
Complementary 20-V (D-S) MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
N-Channel	20	0.075 @ $V_{GS} = 4.5$ V	4.2	4
		0.134 @ $V_{GS} = 2.5$ V	3.1	
P-Channel	-20	0.155 @ $V_{GS} = -4.5$ V	-2.9	3
		0.260 @ $V_{GS} = -2.5$ V	-2.2	

TrenchFET®
Power MOSFETs

1206-8 ChipFET®

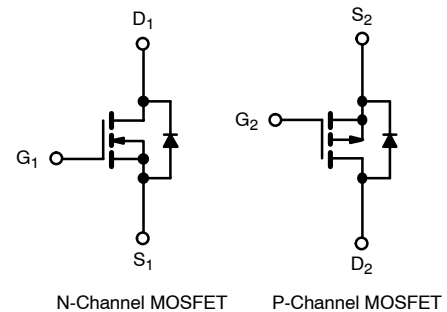


Marking Code

EB XX

Lot Traceability
and Date Code

Part # Code



N-Channel MOSFET

P-Channel MOSFET

Ordering Information: Si5513DC-T1
Si5513DC-T1—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	N-Channel		P-Channel		Unit
			5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage		V _{DS}	20		-20		V
Gate-Source Voltage		V _{GS}	± 12				
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	4.2	3.1	-2.9	-2.1	A
	T _A = 85°C		3.0	2.2	-2.1	-1.5	
Pulsed Drain Current		I _{DM}	10		-10		
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9	-1.8	-0.9	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.1	1.1	2.1	1.1	W
	T _A = 85°C		1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150				°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260				

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	50	60	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6		1.5	V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6		-1.5		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch P-Ch			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch			-1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	N-Ch			5		
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 70 °C	P-Ch			-5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	10			A	
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-10				
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.1 A	N-Ch		0.065	0.075	Ω	
		V _{GS} = -4.5 V, I _D = -2.1 A	P-Ch		0.130	0.155		
		V _{GS} = 2.5 V, I _D = 2.3 A	N-Ch		0.115	0.134		
		V _{GS} = -2.5 V, I _D = -1.7 A	P-Ch		0.215	0.260		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 3.1 A	N-Ch		8		S	
		V _{DS} = -10 V, I _D = -2.1 A	P-Ch		5			
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V	
		I _S = -0.9 A, V _{GS} = 0 V	P-Ch		-0.8	-1.2		
Dynamic ^b								
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 3.1 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -2.1 A	N-Ch P-Ch		4 3	6 6	nC	
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		0.6 0.9			
Gate-Drain Charge	Q _{gd}		N-Ch P-Ch		1.3 0.6			
Turn-On Delay Time	t _{d(on)}		N-Ch P-Ch		12 13	18 20		ns
Rise Time	t _r	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _g = 6 Ω	N-Ch P-Ch		35 35	55 55		
Turn-Off Delay Time	t _{d(off)}		N-Ch P-Ch		19 25	30 40		
Fall Time	t _f		N-Ch P-Ch		9 25	15 40		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs	N-Ch		40	80		
		I _F = -0.9 A, di/dt = 100 A/μs	P-Ch		40	80		

Notes

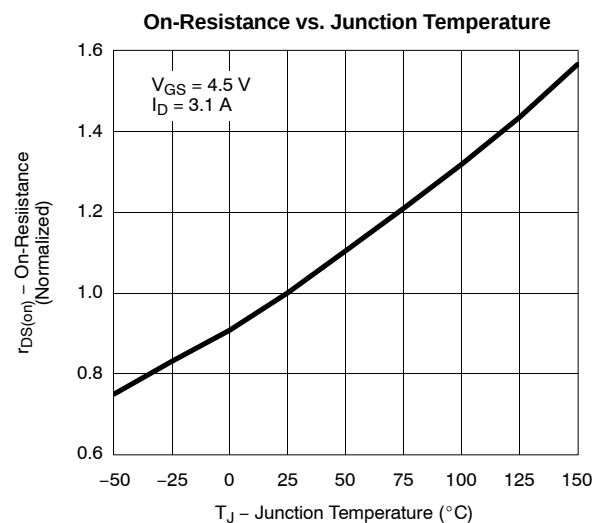
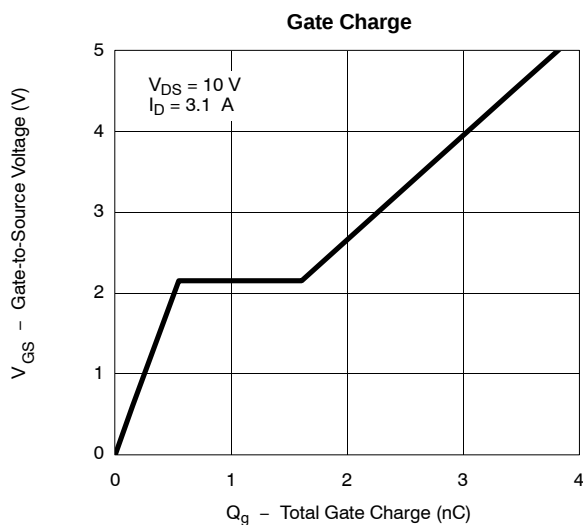
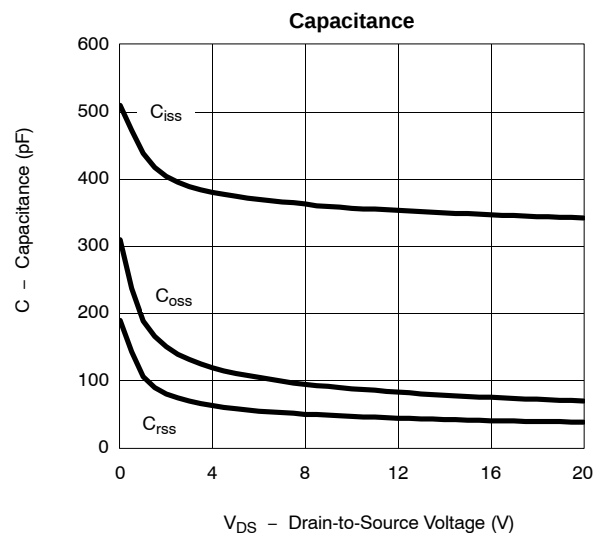
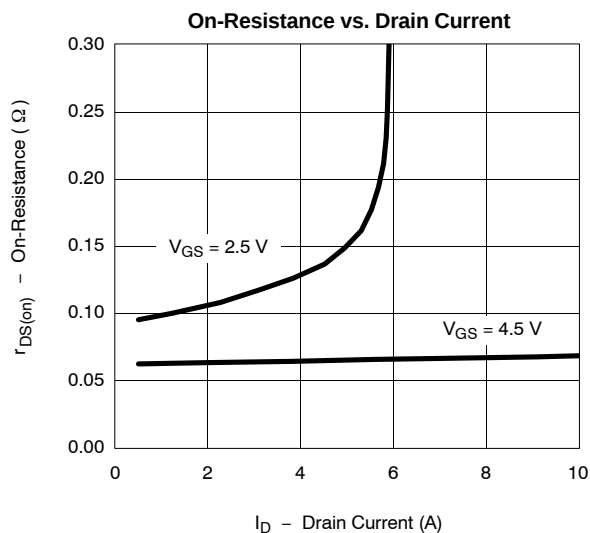
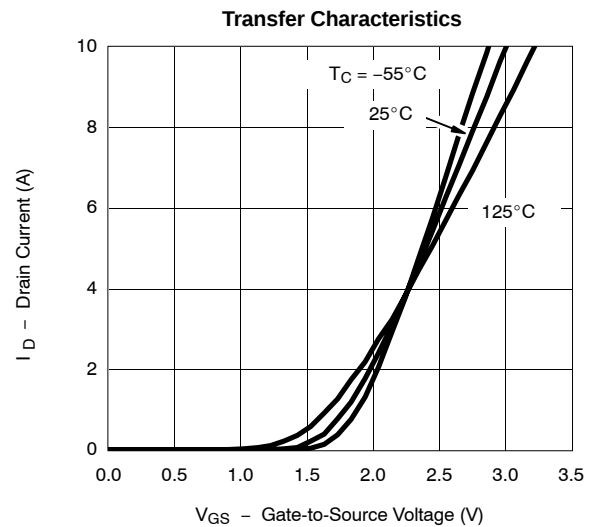
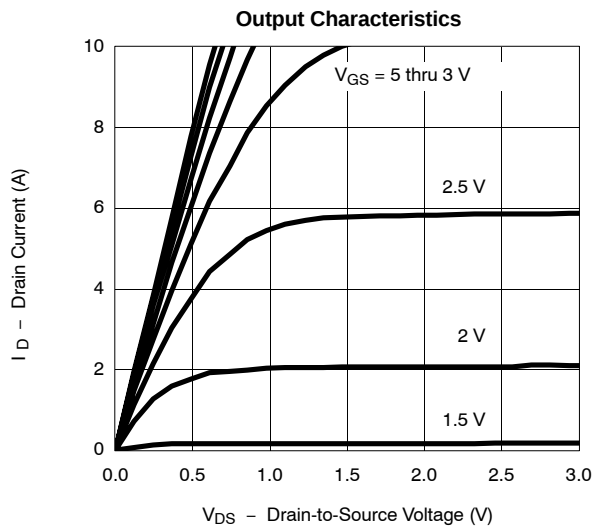
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%,
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



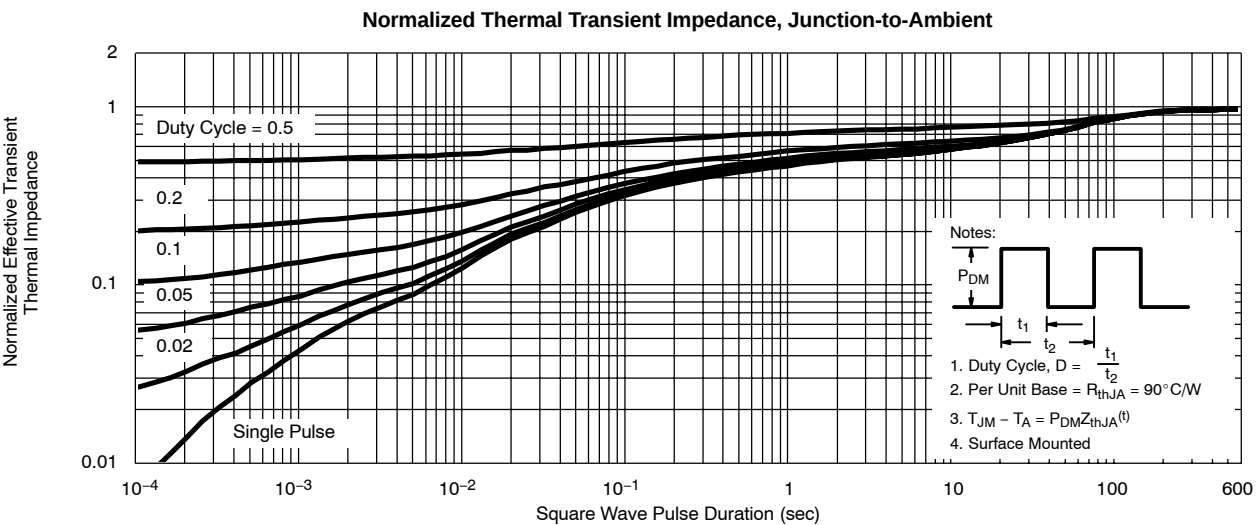
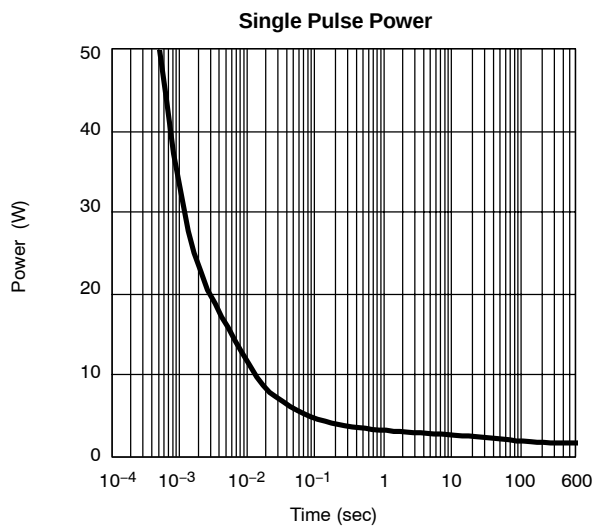
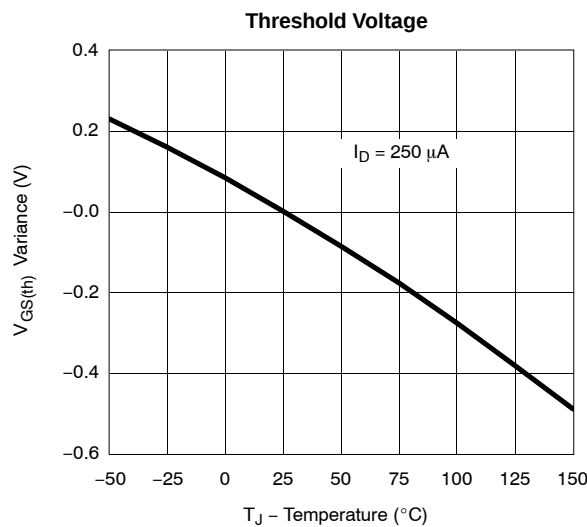
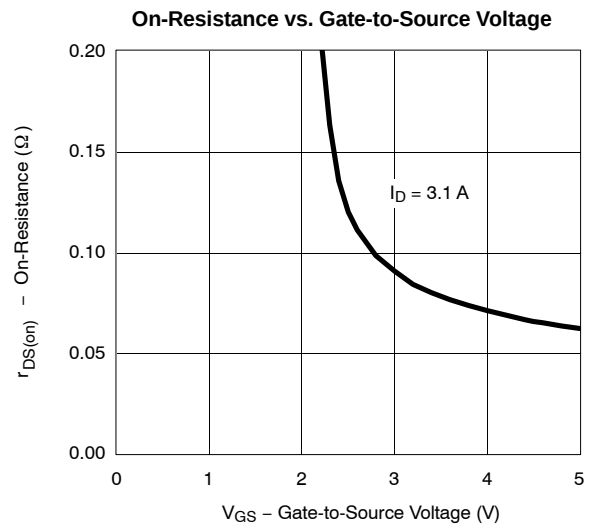
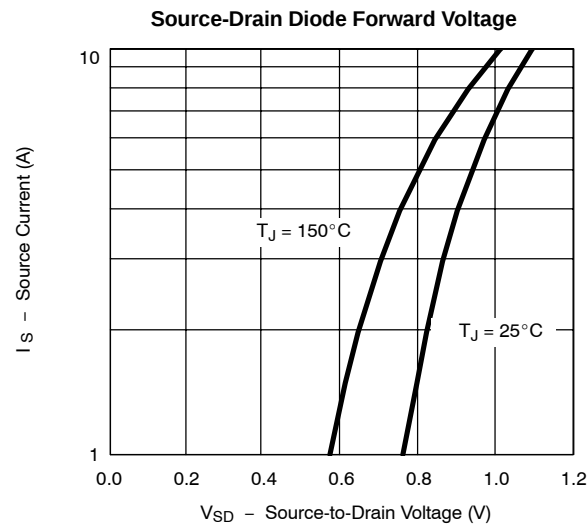
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) **N-CHANNEL**

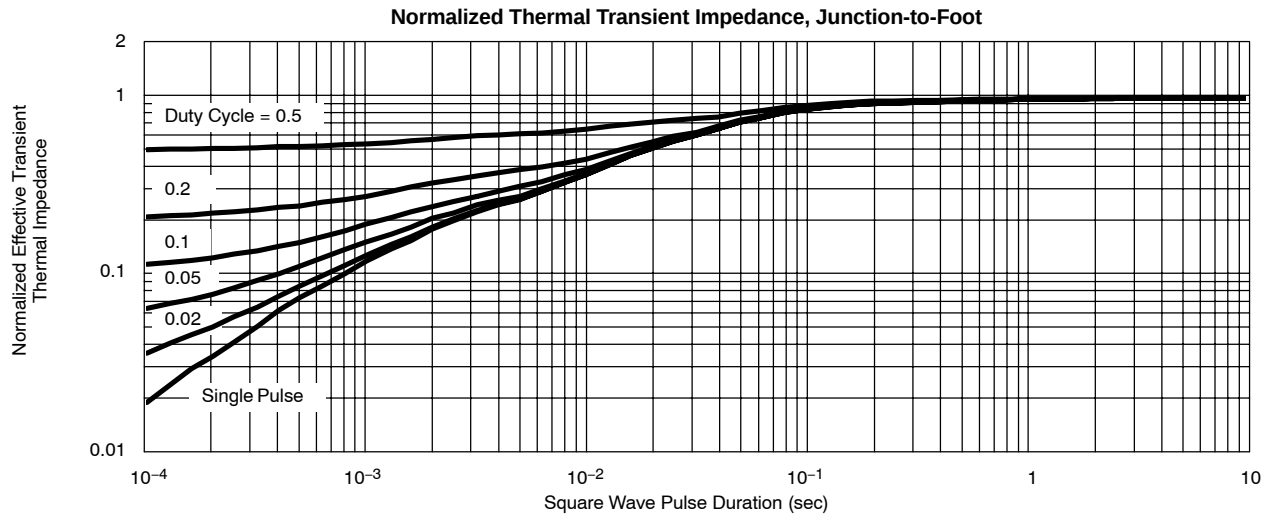


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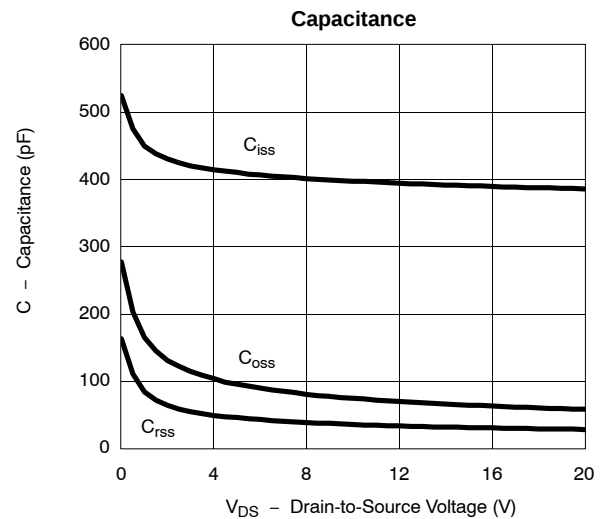
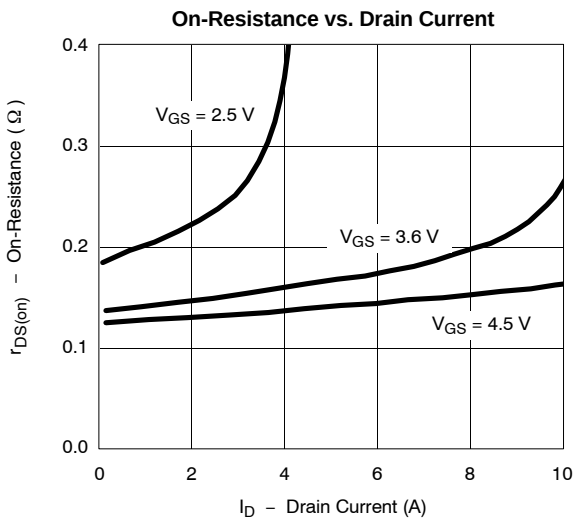
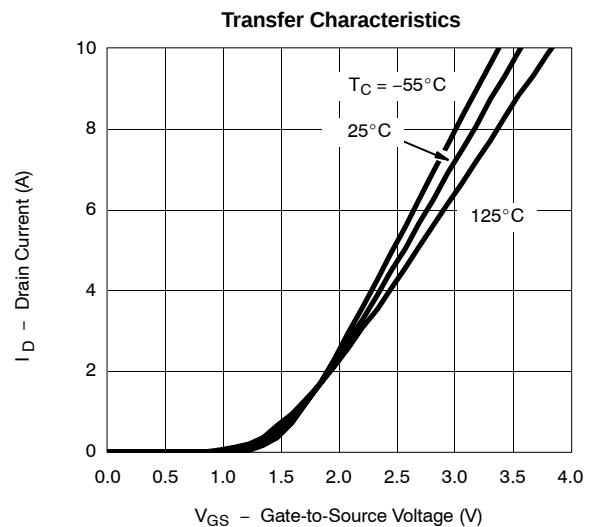
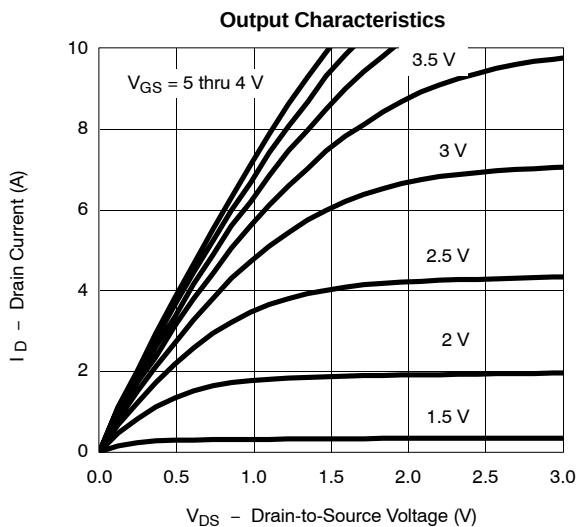
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

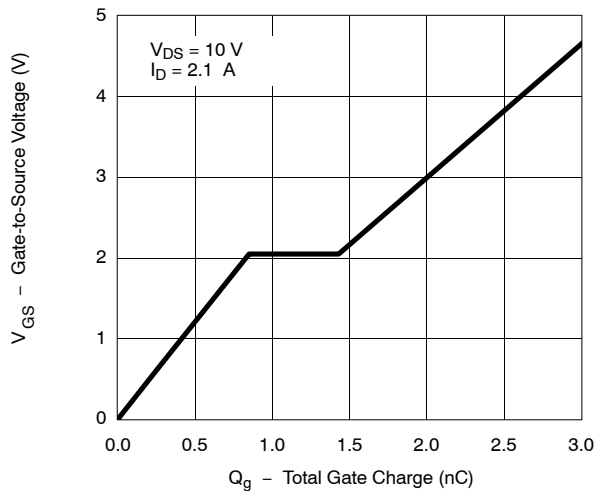
P-CHANNEL



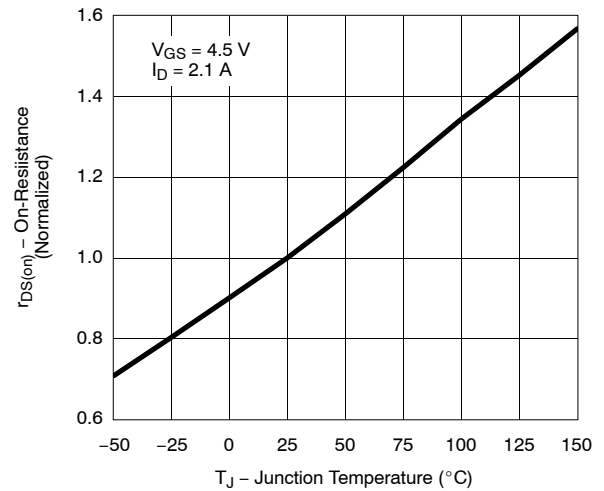
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

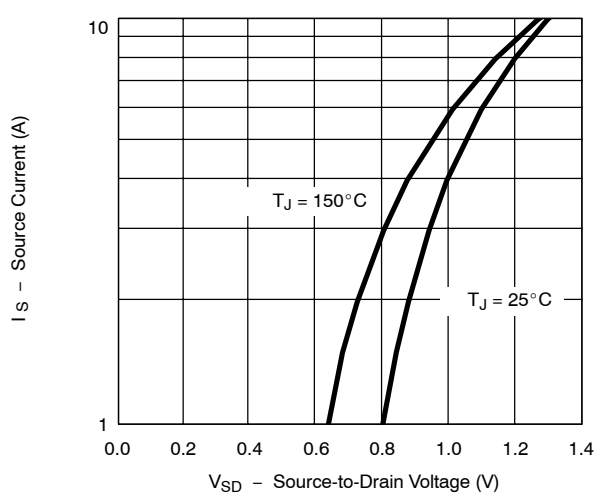
Gate Charge



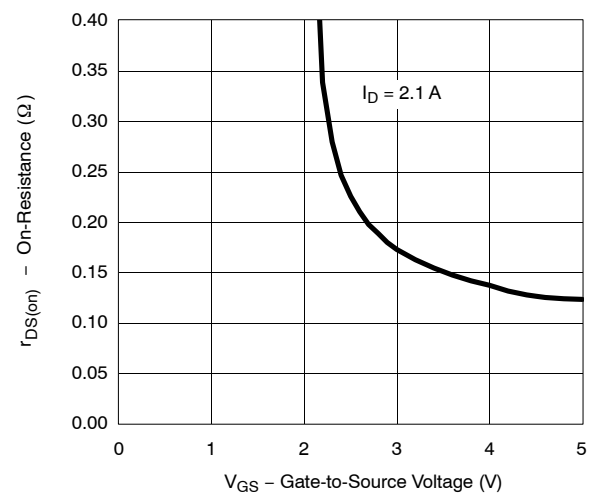
On-Resistance vs. Junction Temperature



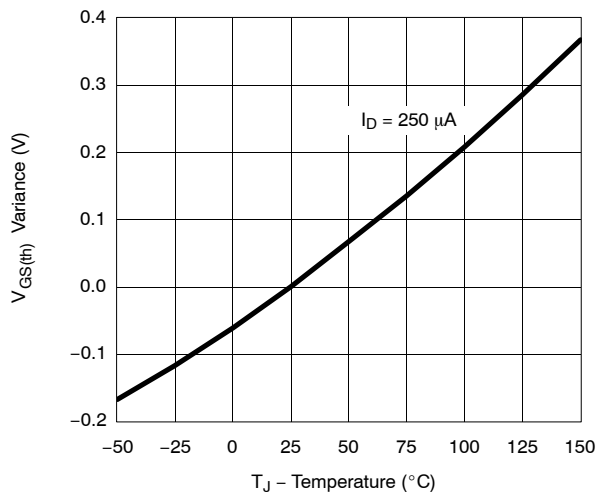
Source-Drain Diode Forward Voltage



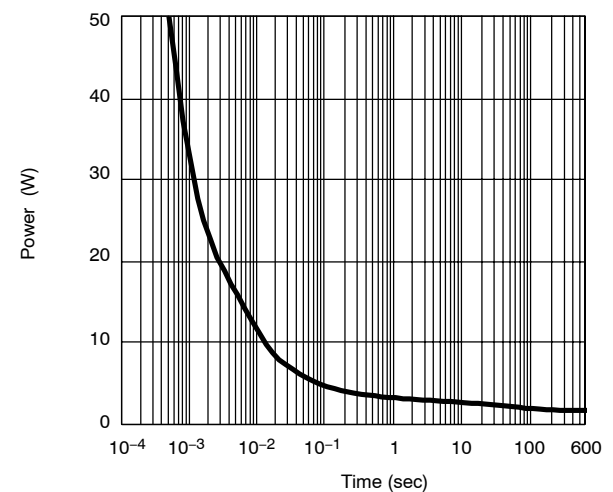
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power

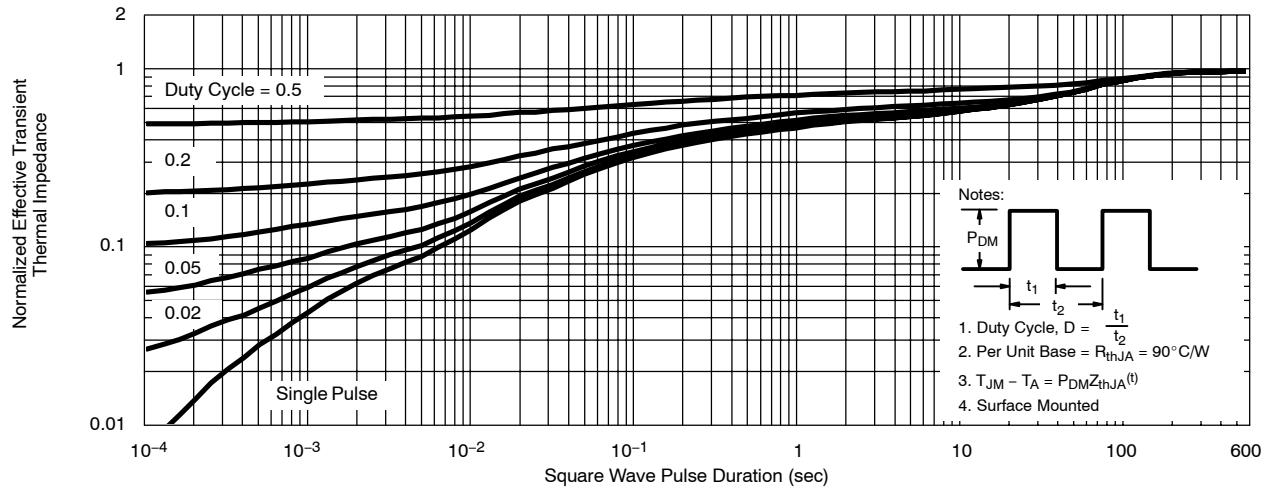




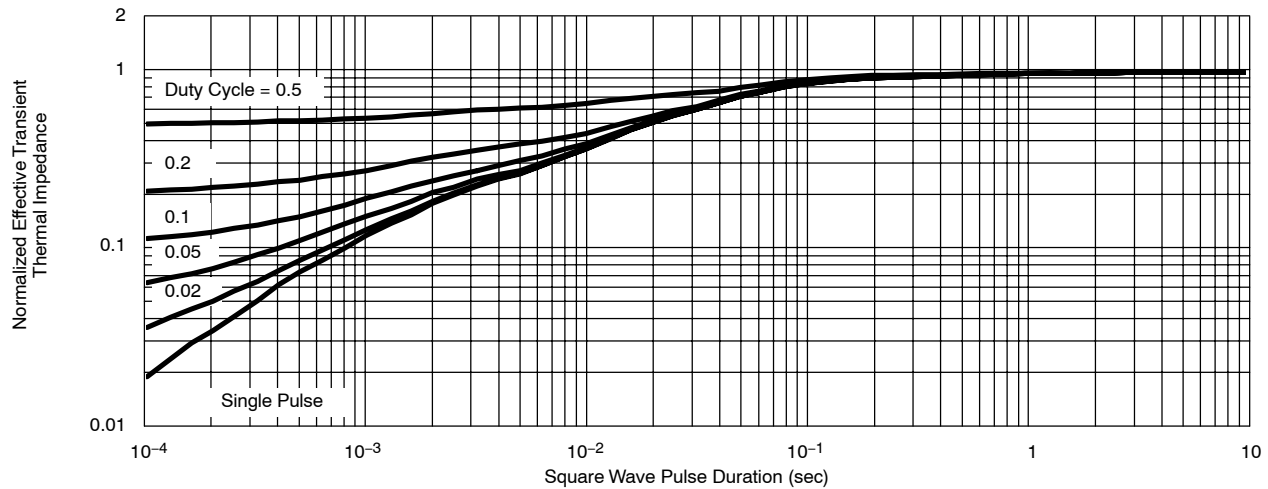
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71186>.