



128K x 16 Static RAM

Features

- High Speed
 - 55 ns and 70 ns availability
- Low voltage range:
 - 1.65V–1.95V
- Pin Compatible with CY62136BV18
- Ultra-low active power
 - Typical Active Current: 0.5 mA @ $f = 1$ MHz
 - Typical Active Current: 1.5 mA @ $f = f_{\max}$ (70 ns speed)
- Low standby power
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

The CY62136CV18 is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life® (MoBL™) in portable applications such as cellular telephones. The device also has

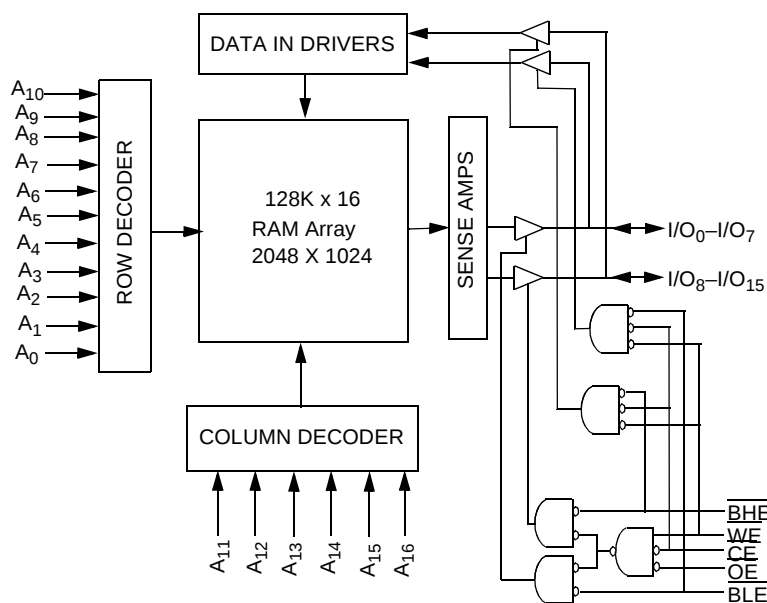
an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{\text{CE}}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

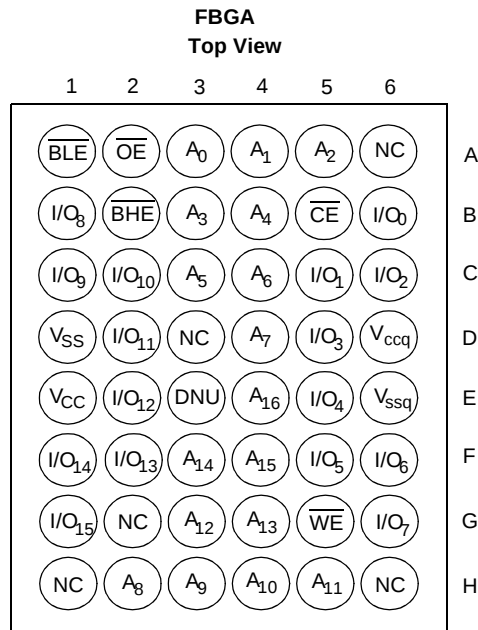
Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62136CV18 is available in 48-ball FBGA packaging.

Logic Block Diagram



Pin Configuration^[1, 2]



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied.....	–55°C to +125°C
Supply Voltage to Ground Potential	–0.2V to +2.4V

DC Voltage Applied to Outputs

in High Z State^[3]..... –0.2V to $V_{CC} + 0.2V$

DC Input Voltage^[3]..... –0.2V to $V_{CC} + 0.2V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62136CV18	Industrial	–40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I _{CC})				Standby (I _{SB2})	
					f = 1 MHz		f = f _{max}		Typ. ^[4]	Max.
	Typ. ^[4]	Max.	Typ. ^[4]		Max.					
CY62136CV18	1.65V	1.80V ^[4]	1.95V	55 ns	0.5 mA	2 mA	2 mA	7 mA	1 μA	8 μA
				70 ns	0.5 mA	2 mA	1.5 mA	6 mA		

Notes:

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
- $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62136CV18-55			CY62136CV18-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 1.65V	1.4			1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 1.65V			0.2			0.2	V
V _{IH}	Input HIGH Voltage		1.4		V _{CC} + 0.2V	1.4		V _{CC} + 0.2V	V
V _{IL}	Input LOW Voltage		-0.2		0.4	-0.2		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 1.95V I _{OUT} = 0 mA CMOS levels		2	7		1.5	6	mA
		f = 1 MHz		0.5	2		0.5	2	mA
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)		1	8		1	8	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 1.95V							

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	6	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

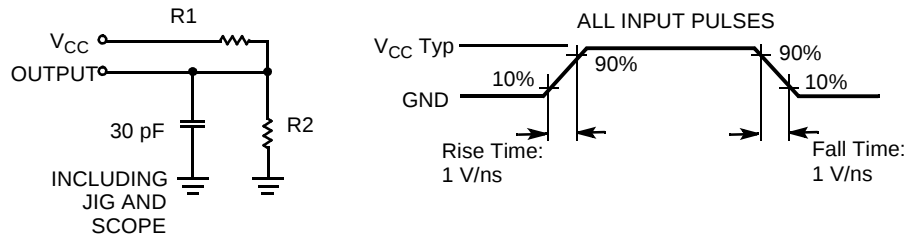
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[5]		Θ _{JC}	16	°C/W

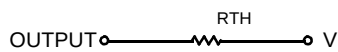
Note:

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

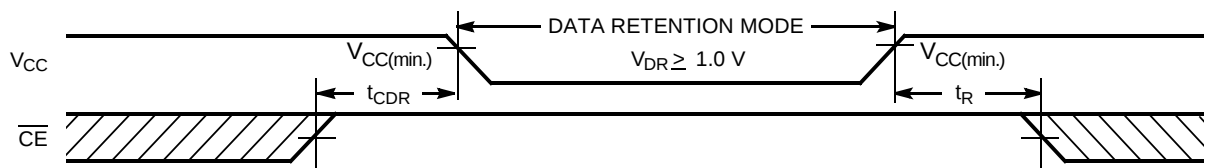


Parameters	1.8V	UNIT
R1	13500	Ohms
R2	10800	Ohms
R _{TH}	6000	Ohms
V _{TH}	0.80	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.0		1.95	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.0V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		0.5	5	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time		0			ns
t _R ^[6]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform



Note:

6. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.

Switching Characteristics Over the Operating Range^[7]

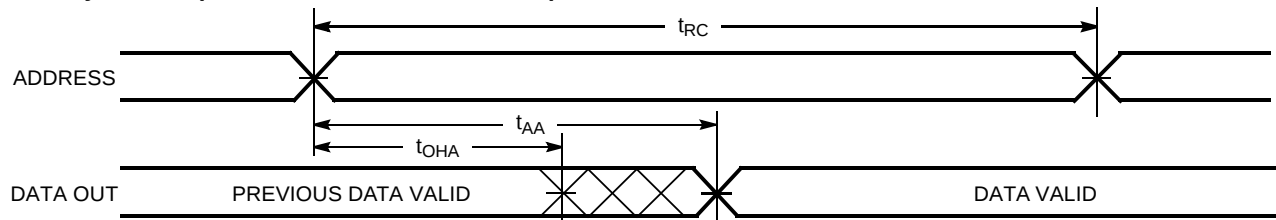
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[8]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[8, 9]		20		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[8]	5		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[8, 9]		20		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t _{DBE}	$\overline{\text{BLE/BHE}}$ LOW to Data Valid		25		35	ns
t _{LZBE}	$\overline{\text{BLE/BHE}}$ LOW to Low Z ^[8]	5		5		ns
t _{HZBE}	$\overline{\text{BLE/BHE}}$ HIGH to High Z ^[8, 9]		20		25	ns
Write Cycle ^[10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	40		60		ns
t _{AW}	Address Set-Up to Write End	40		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t _{BW}	$\overline{\text{BLE/BHE}}$ LOW to Write End	40		60		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[8, 9]		20		25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[8]	5		10		ns

Notes:

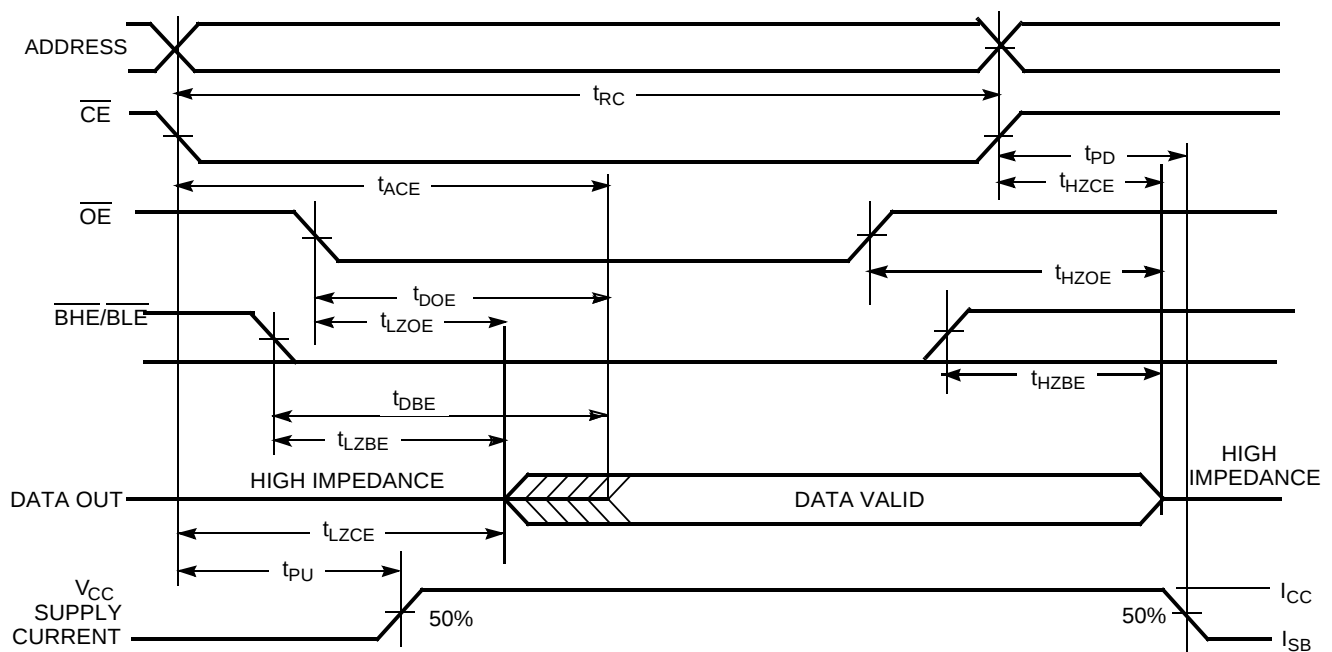
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , t_{HZBE} and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[11, 12]



Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[12, 13]

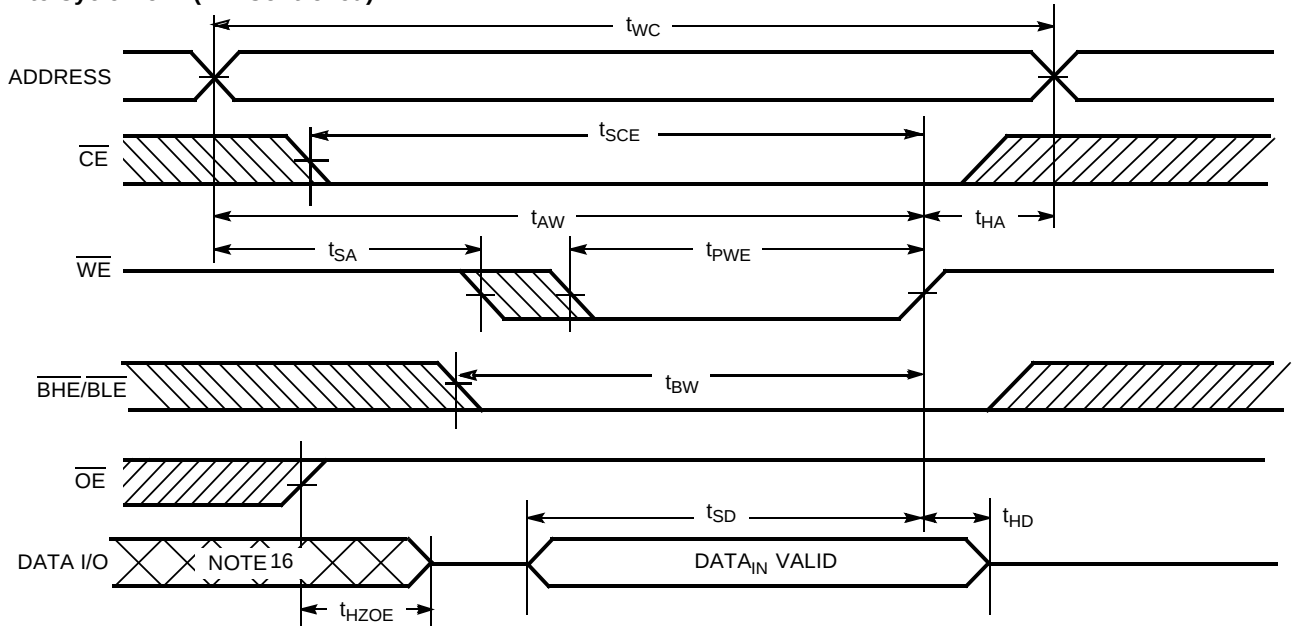


Notes:

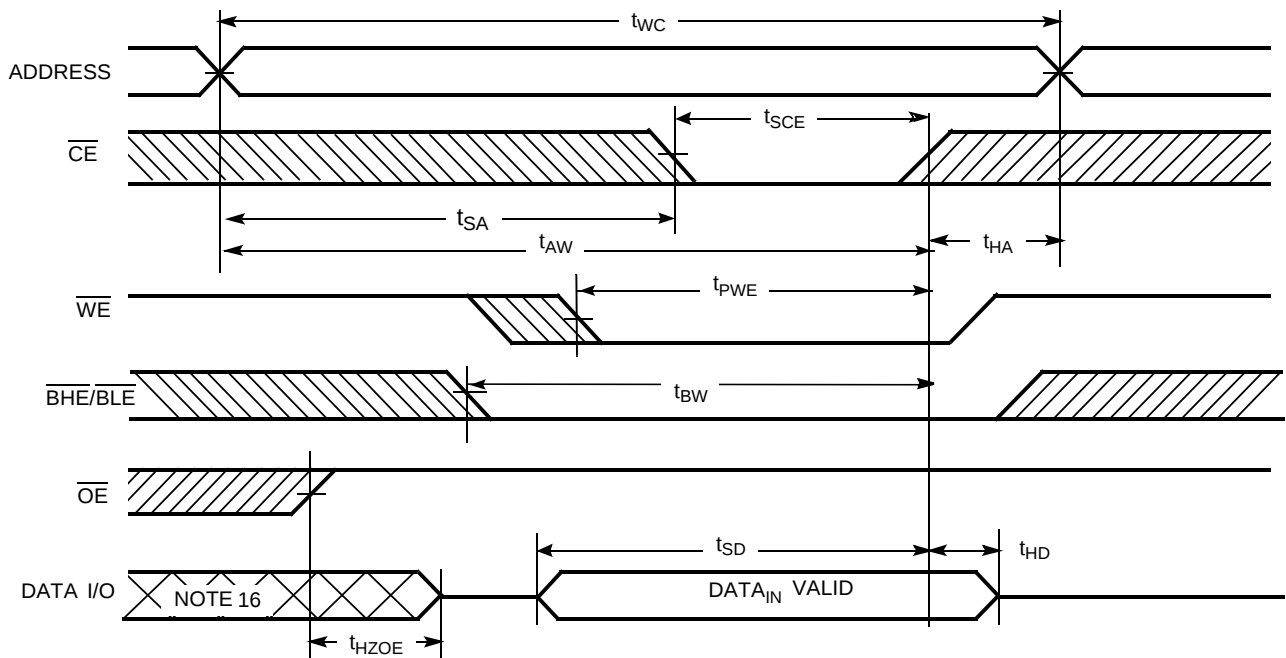
11. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$.
12. $\overline{\text{WE}}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, transition LOW.

Switching Waveforms

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) ^[10, 14, 15]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) ^[10, 14, 15]

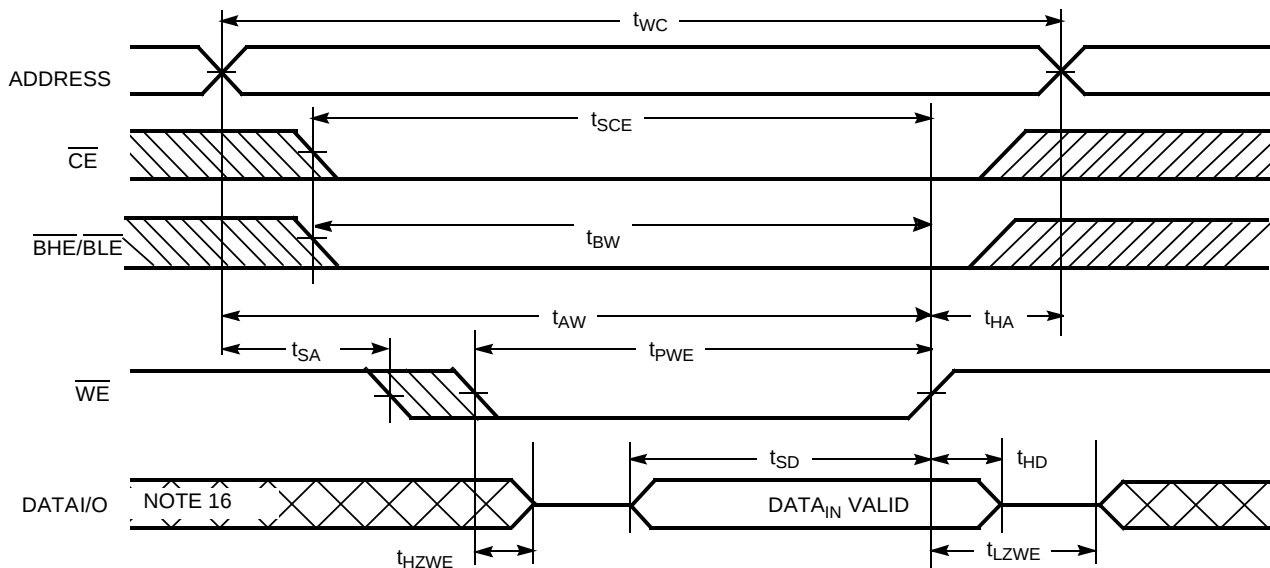


Notes:

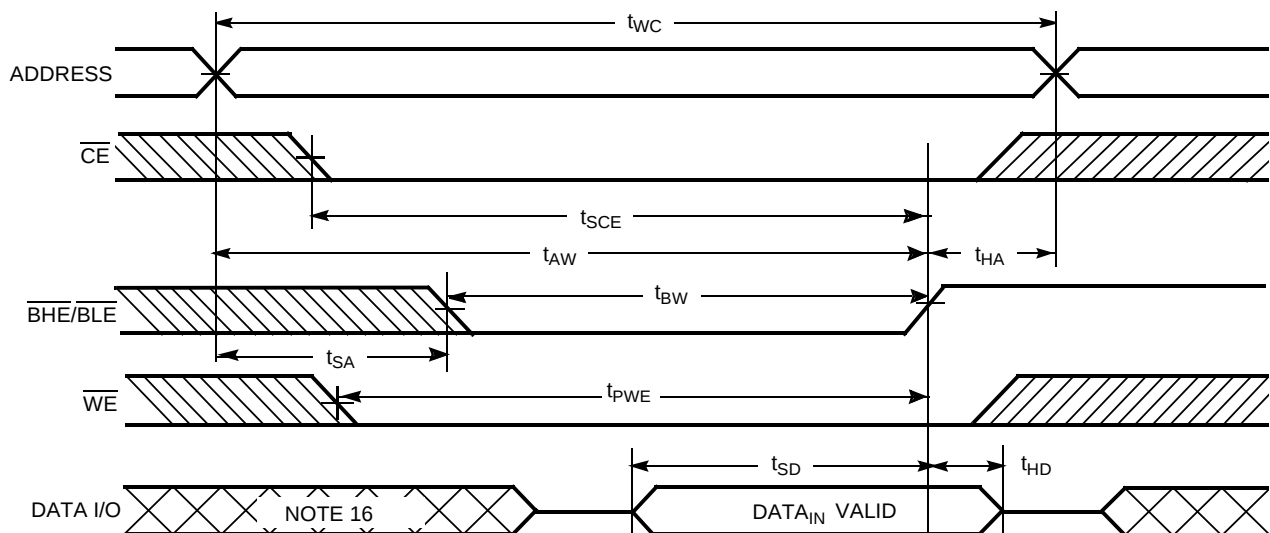
14. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)

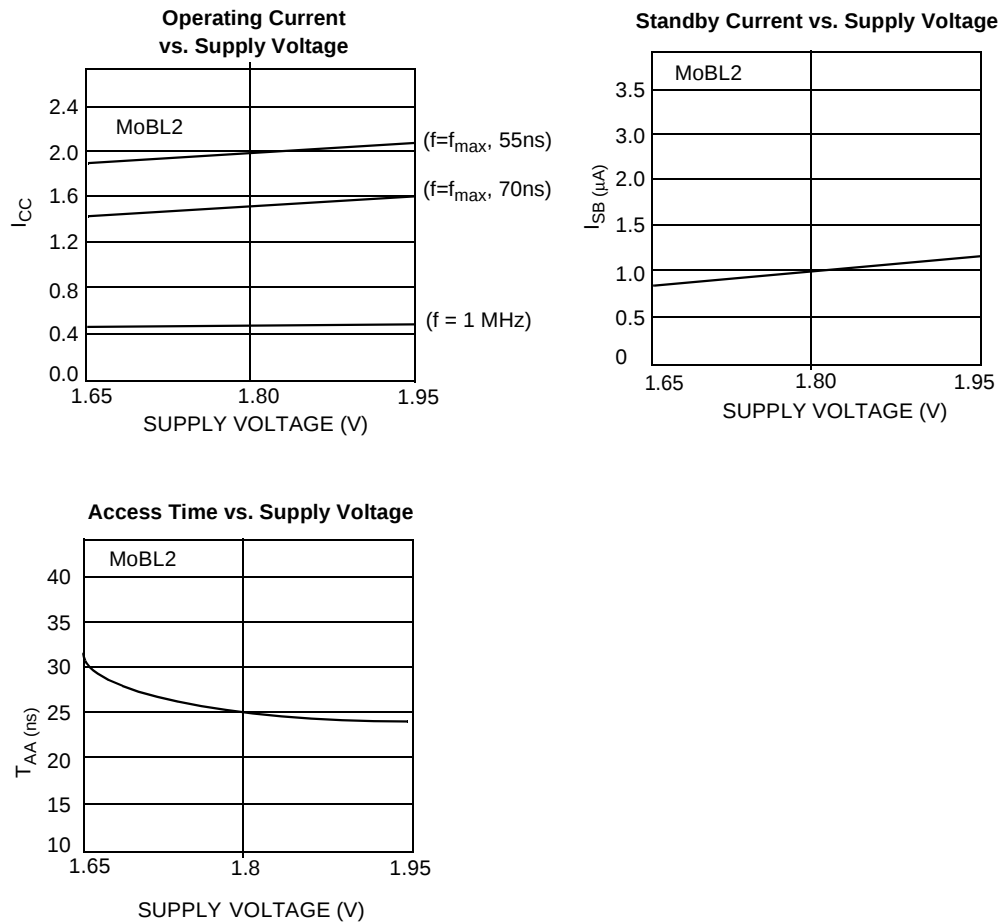


Write Cycle No. 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]



Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.)



Truth Table

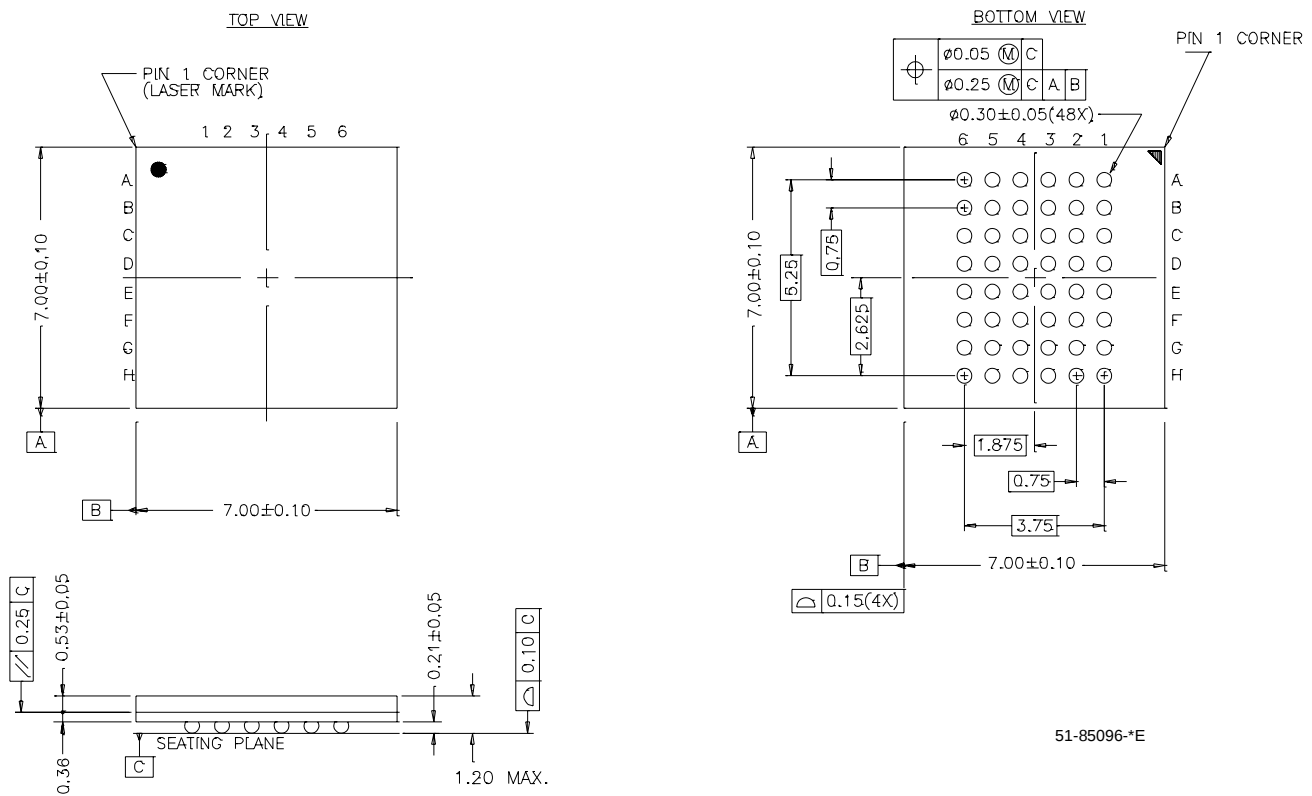
CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

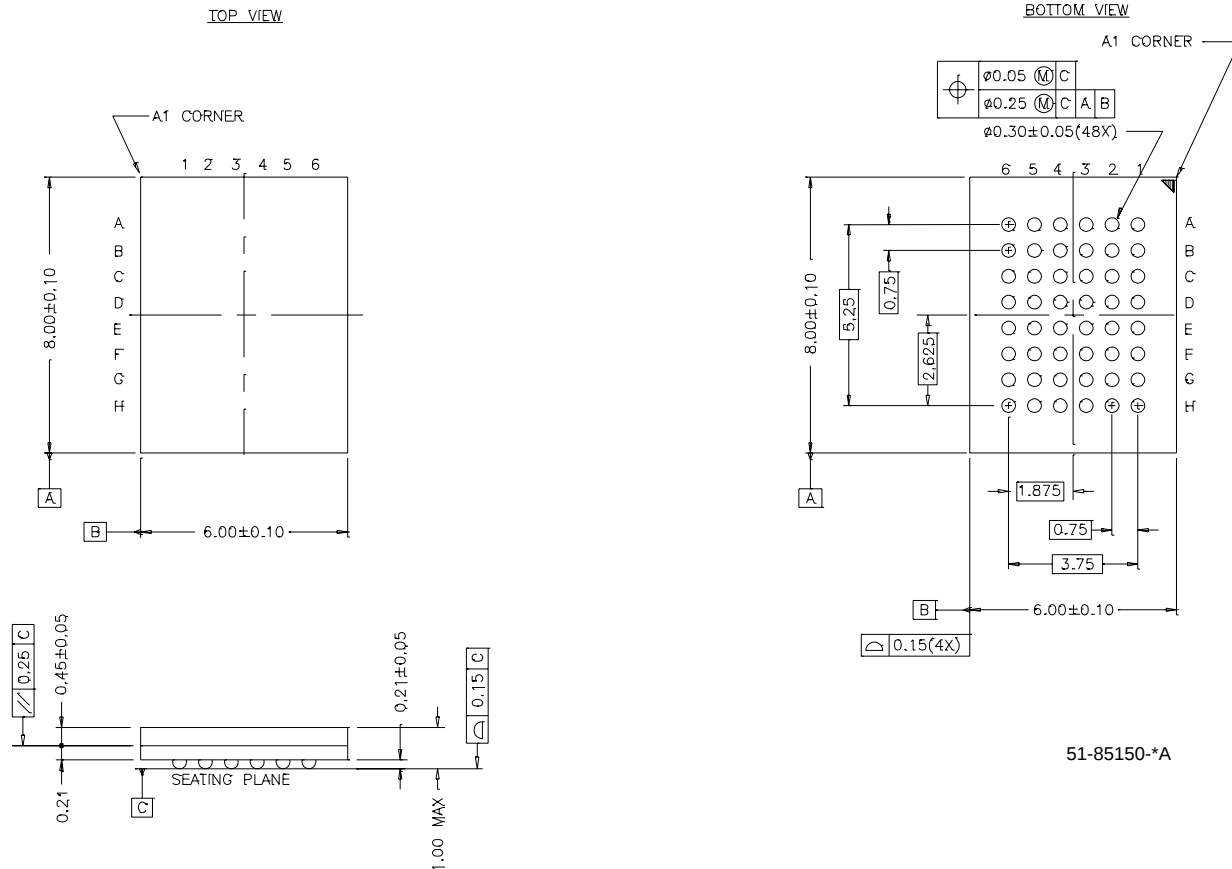
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62136CV18LL-70BAI	BA48A	48-Ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	Industrial
	CY62136CV18LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1mm)	
55	CY62136CV18LL-55BAI	BA48A	48-Ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm)	
	CY62136CV18LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1mm)	

Package Diagram

48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A



Package Diagram (continued)
48-Lead VFBGA (6 x 8 x 1 mm) BV48A


51-85150-*A

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Document Title: CY62136CV18 MoBL2™, 128K x 16 Static RAM Document Number: 38-05016				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106264	05/07/01	HRT/MGN	New Data Sheet
*A	107701	06/15/01	MGN	Delete data sheet. Not offering device.
*B	111522	11/06/01	GAV	Reactivate spec. Final data sheet.
*C	115865	09/04/02	MGN	Add BV pkg