

VCO + phase comparator IC for PLL system

BU2374FV

BU2374FV is a VCO+phase comparator IC used to construct PLL system. PLL system is constructed and low jitter clocks can be generated by adopting external LPF and divider. Through a mechanism incorporated in this IC the output could be switched into quarter. Another function can set in the center point of frequency by adjusting external resistance.

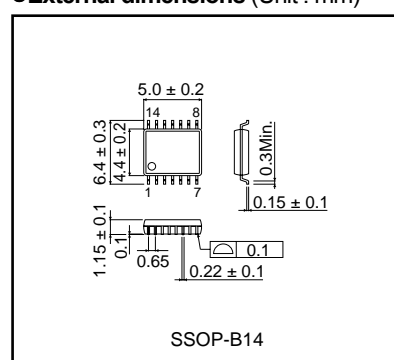
●Applications

TV

●Features

- 1) $V_{DD}=3.3V\pm 5\%$ operating guaranteed
- 2) Oscillating range of VCO is 37MHz~60MHz
- 3) High-speed edge trigger type phase comparator
- 4) VCO can be fine-adjusted by external resistor.
- 5) VCO and phase comparator can be controlled independently.
- 6) Small SSOP-B14 package

●External dimensions (Unit : mm)



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{DD}+0.5$	V
Power dissipation	P_d	400*	mW
Storage temperature	T_{stg}	-30 to +125	°C

*An operation is not guaranteed.

*In case it is used at $T_a=25^{\circ}\text{C}$ or more, 4.0mW is reduced at every 1°C.

*Radiation resistance design is not used.

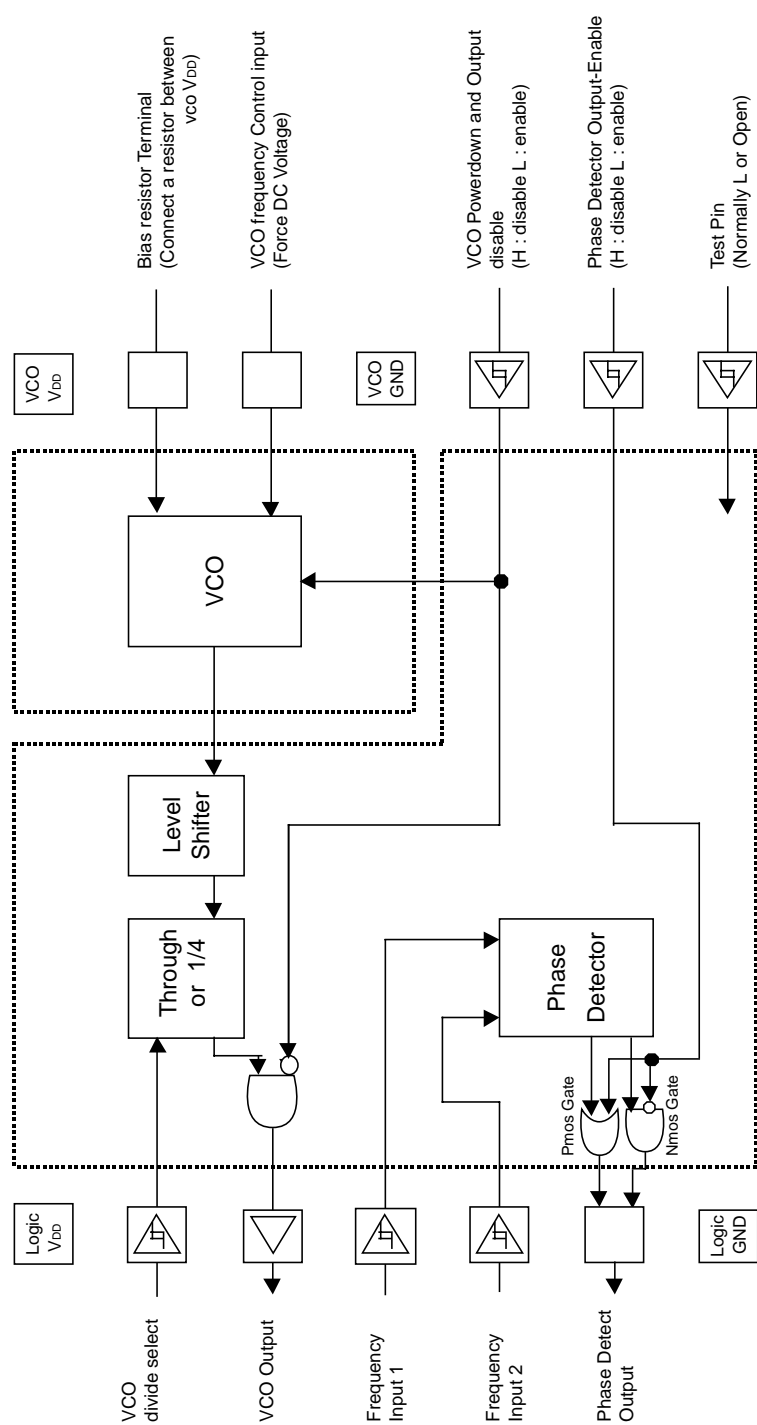
*Power dissipation is measured when BU2374FV is placed on the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.15	—	3.45	V
Input H voltage range	V_{IH}	$0.8V_{DD}$	—	V_{DD}	V
Input L voltage range	V_{IL}	0	—	$0.2V_{DD}$	V
Operating temperature	T_{opr}	-20	—	+75	°C
Output load	C_L	—	—	15	pF

Multimedia ICs

●Block diagram



Multimedia ICs

●Pin descriptions

Pin No.	Pin name	Functions
1	LOGIC V _{DD}	Digital V _{DD}
2	SELECT	VCO output frequency select (H:1/4 output, L:1/1 output)
3	VCO OUT	VCO output
4	FIN-A	Input reference frequency is applied to Fin A
5	FIN-B	Input for VCO external counter output frequency
6	PFD_OUT	PD output
7	LOGIC_GND	Digital GND
8	TEST	TEST input with Pull-down resistor (Normally OPEN or 'L')
9	PFD_INHIBIT	Control Pin for PD (H:PD disable (Hi impedance state), L:PD enable)
10	VCO_INHIBIT	VCO mode select (H:VCO OUT disable (L Fix), L:VCOOUT enable)
11	VCO_GND	GND for VCO (Analog GND)
12	VCO_IN	VCO control voltage input
13	BIAS	For adjusting VCO output frequency range (An external resistor connect between VCO_V _{DD} and BIAS)
14	VCO_V _{DD}	V _{DD} for VCO (Analog V _{DD})

Multimedia ICs

●Input / output circuits

Pin No.	Equivalent circuit
Output Pin (Pin3)	
Output Pin (Pin6)	
Input Pin (Schmitt trigger) (Pin2, 4, 5, 8, 9, 10) Pin8 : with pull-down resistance	
Input Pin (Pin12)	
Input Pin (Pin13)	

Multimedia ICs

●Electrical characteristics (Unless otherwise noted, Ta=25°C, Vcc=3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VCO section						
VCO_OUT Output H voltage	V _{OH}	3.0	—	—	V	I _{OH} =-2.0mA
VCO_OUT Output L voltage	V _{OL}	—	—	0.3	V	I _{OL} =2.0mA
input current (VCO_INHIBIT, SELECT)	I _{IH} , I _{IL}	—	—	±1	μA	
input impedance (VCO_IN)	Z _i	—	10	—	MΩ	
VCO current consumption (inhibit)	I _{DD} (INH)	—	—	1	μA	at VCO_INHIBIT=V _{DD} PFD_INHIBIT=V _{DD}
VCO current consumption (normal operation)	I _{DD} (vco)	—	12.5	—	mA	Output 50MHz
VCO control voltage	V _I (vco_in)	0.5	—	V _{DD} -0.5	V	
VCO frequency range	frange	37	—	60	MHz	
Bias Resistor range	R _{bias}	2.0	—	3.0	KΩ	* 1
Frequency sersibility	β ₁	—	23	—	MHz/V	* 2
Output duty	Duty	45	50	55	%	at 1/2 V _{DD} point
Output Rise-time	t _r	—	2.5	—	nsec	Time is from V _{DD} × 0.2 to v _{dd} × 0.8
Output Fall-time	t _f	—	2.5	—	nsec	Time is from V _{DD} × 0.8 to v _{dd} × 0.2

* 1 Value of design guarantee (all guarantee range)
 Bias R=2.0kΩ 37MHz to 54MHz
 Bias R=2.4kΩ 45MHz to 58MHz
 Bias R=3.0kΩ 53MHz to 60MHz

* 2 Frequency sersibility { f1(VCOIN=2.0V)-f2(VCOIN=1.0V) } / 1.0V

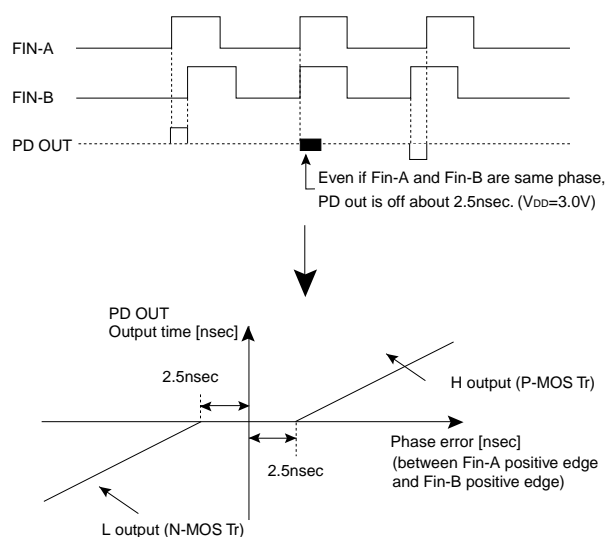
* 3 When FSEL is H and output frequency is 1/4, calculate

Multimedia ICs

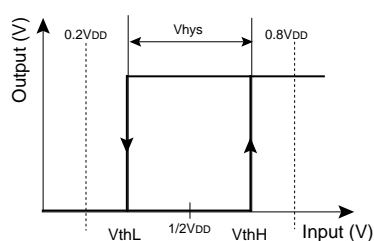
(Unless otherwise noted, $T_a=25^\circ\text{C}$, $V_{CC}=3.3\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
PFD section						
PFD_OUT Output H voltage	V_{OH}	3.0	—	—	V	$I_{OH}=-2.0\text{mA}$
PFD_OUT Output L voltage	V_{OL}	—	—	0.3	V	$I_{OL}=2.0\text{mA}$
input current (PFD_INHIBIT, FIN A, FIN B)	I_{IH}, I_{IL}	—	—	± 1	μA	
PFD current consumption (inhibit)	$I_{DD}(\text{INH})$	—	—	1	μA	at $V_{CO_INHIBIT}=V_{DD}$ $PFD_INHIBIT=V_{DD}$ FIN_A and $B=GND$
PFD current consumption (normal operation)	$I_{DD}(\text{VCO})$	—	0.5	—	mA	FIN_A and $FIN_B=1\text{MHz}$
PFD Function	—	—	—	—	—	*4

*4

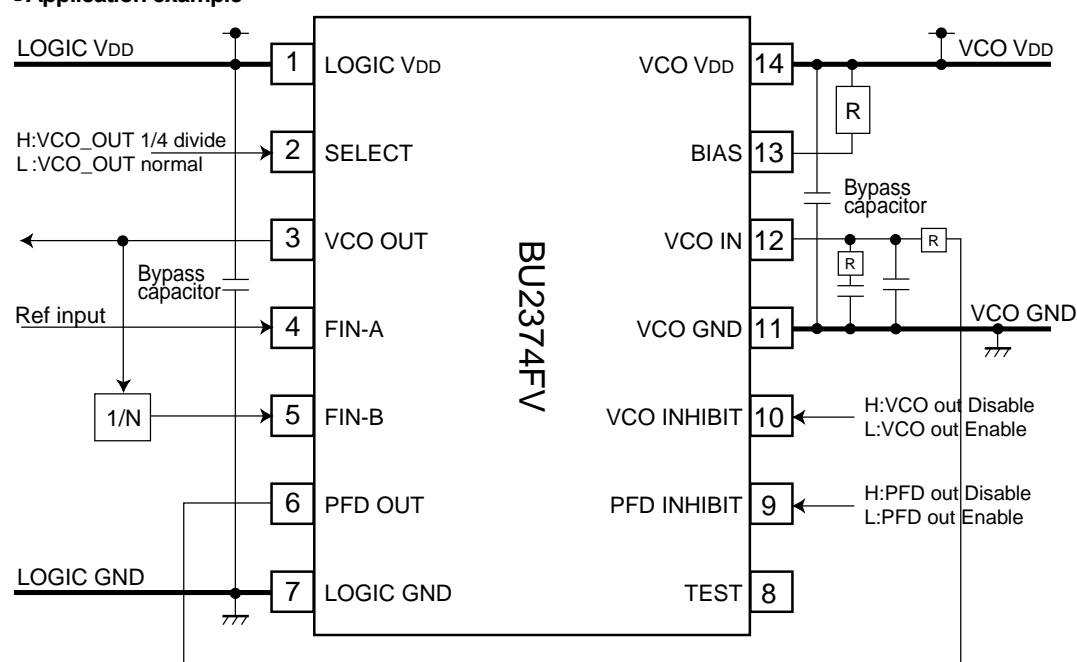


Input pin (FIN_A, FIN_B, VCO_INHIBIT, PFD_INHIBIT, SELECT)



Multimedia ICs

●Application example

VCO_V_{DD}, VCO_GND

Please take care this Power line. Because this line is most weak in digital noise.
So this line must be separated from LOGIC_V_{DD}, GND.
And place bypass capacitor (0.1μF) for power pin as close to BU2374FV as possible.

LOGIC_V_{DD}, LOGIC_GND

This line is noise source. So it should be separated from AV_{DD} (AGND).
And place bypass capacitor (0.1μF) for power pin as close to BU2374FV as possible.
And this line should be connected V_{DD} of external voc-out divide.

Bias

Please take care because the bias is weak in digital noise.
And place capacitor (0.1μF) close to BU2374FV.

*Recommend to use capacitor that is better to reduce high frequency noise.

*Recommend to control (SELECT, PFD_INHIBIT, VCO_INHIBIT) by power line (LOGIC_V_{DD}, LOGIC_GND).

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