



P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.015 @ $V_{GS} = -4.5$ V	-13.2
	0.020 @ $V_{GS} = -2.5$ V	-11.4
	0.029 @ $V_{GS} = -1.8$ V	-9.5

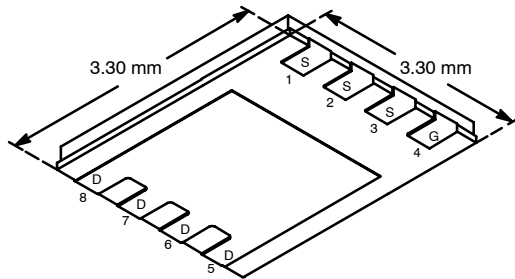
FEATURES

- TrenchFET® Power MOSFET
- New PowerPAK® Package
 - Low Thermal Resistance, R_{thJC}
 - Low 1.07-mm Profile

APPLICATIONS

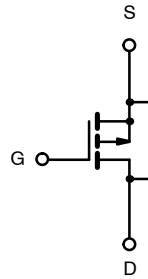
- Load Switch

PowerPAK 1212-8



Bottom View

Ordering Information: Si7413DN-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	−20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	−13.2	−8.4	A
	T _A = 85°C		−9.5	−6.1	
Pulsed Drain Current		I _{DM}	−30		
Continuous Source Current (Diode Conduction) ^a		I _S	−3.2	−1.3	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.8	1.5	W
	T _A = 85°C		2.0	0.8	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	26	33	$^\circ\text{C/W}$
	Steady State		65	81	
Maximum Junction-to-Case		R_{thJC}	1.9	2.4	

Notes

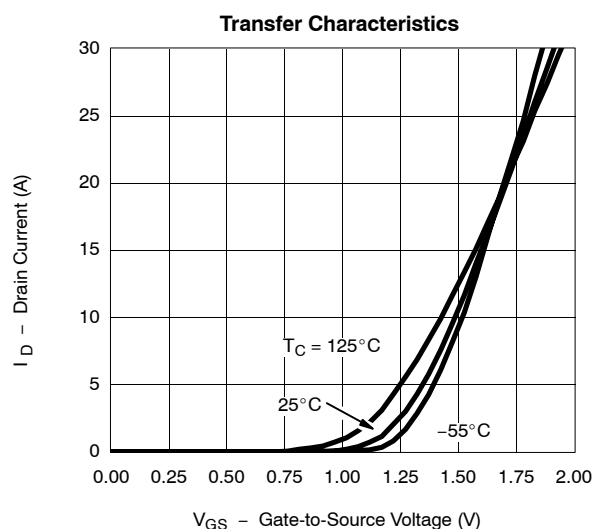
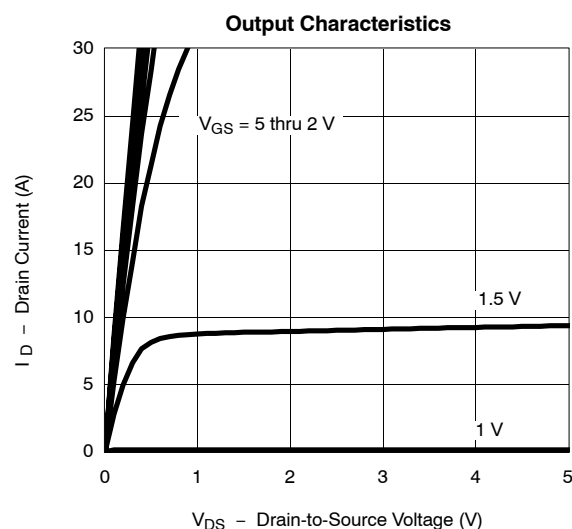
a. Surface Mounted on 1" x 1" FR4 Board.

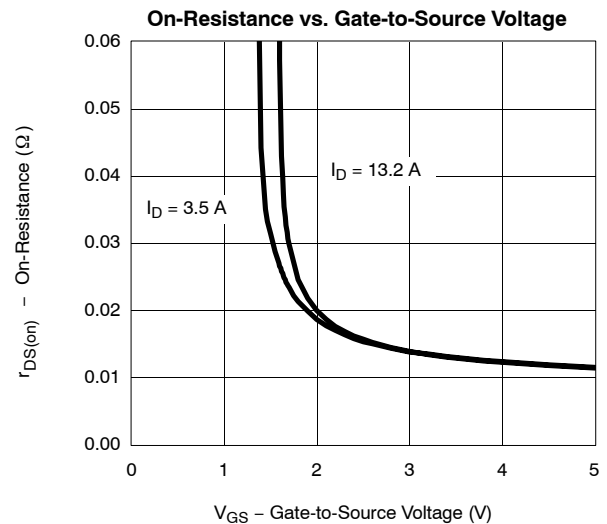
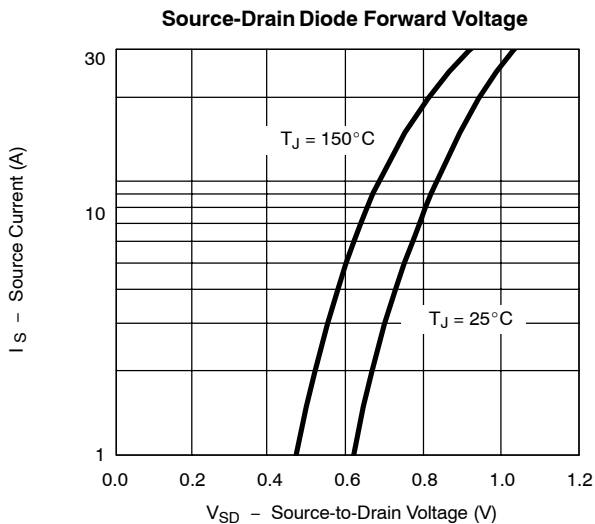
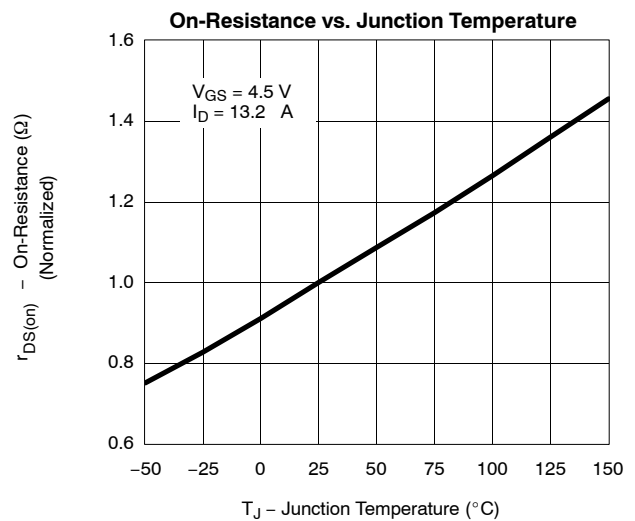
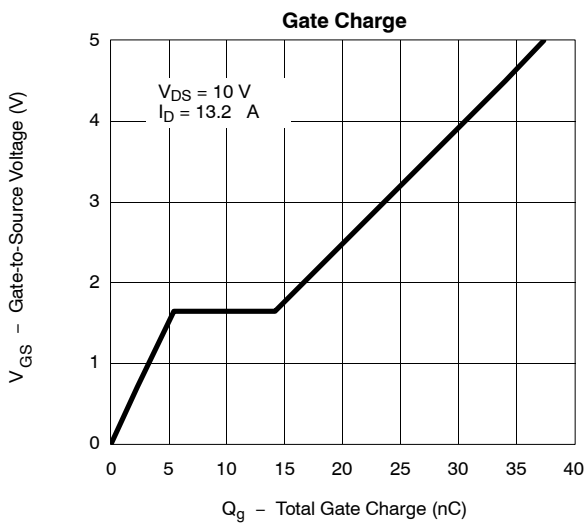
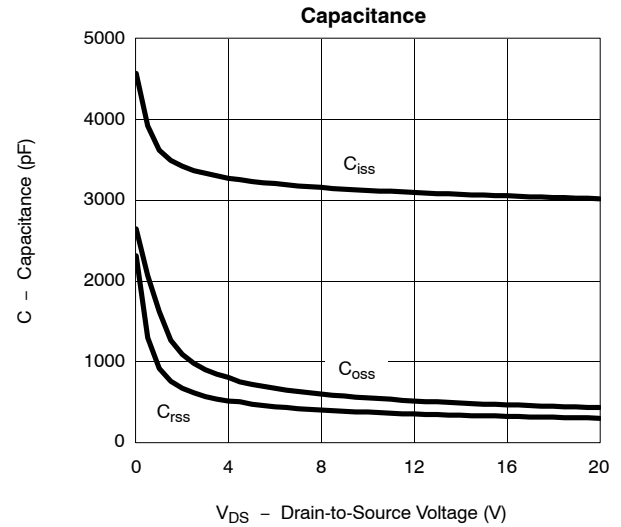
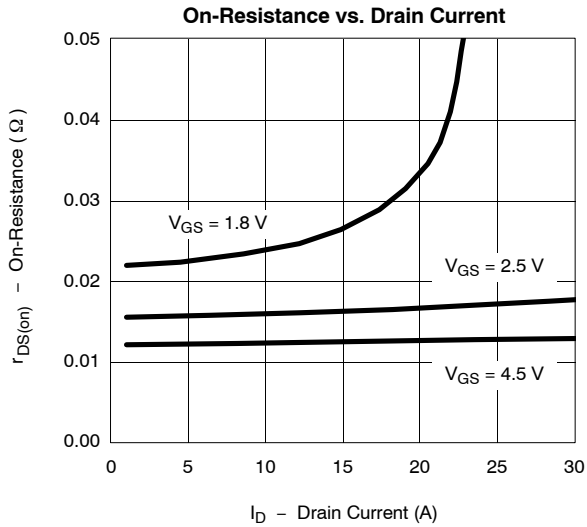
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

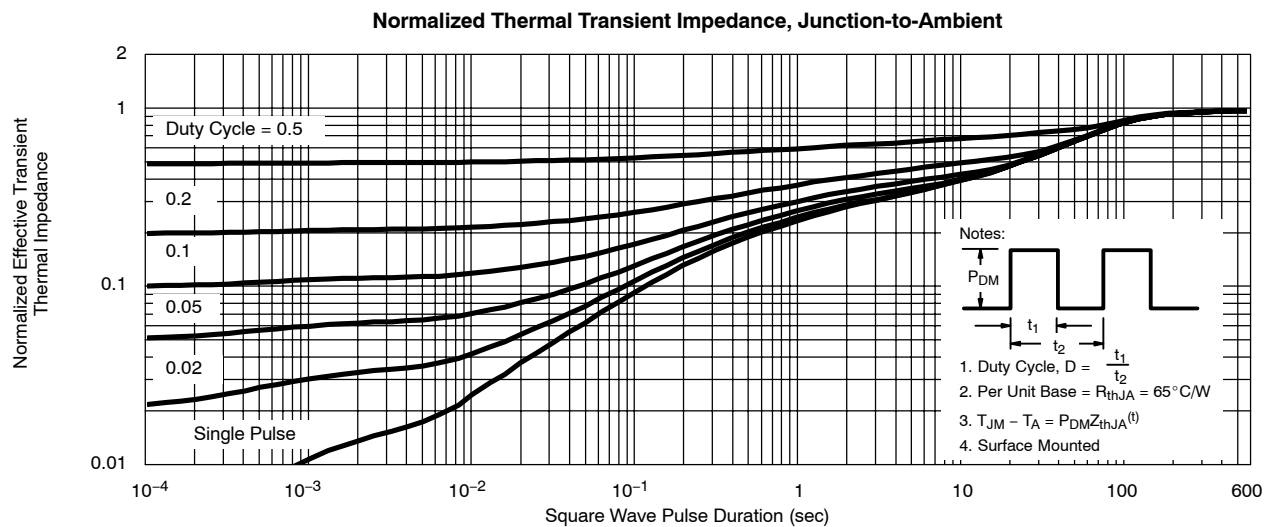
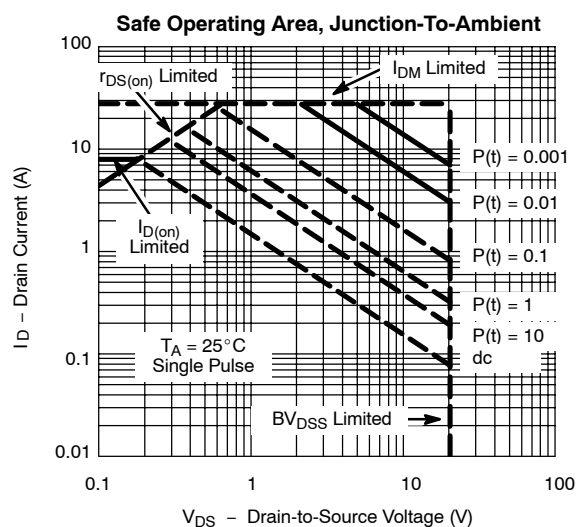
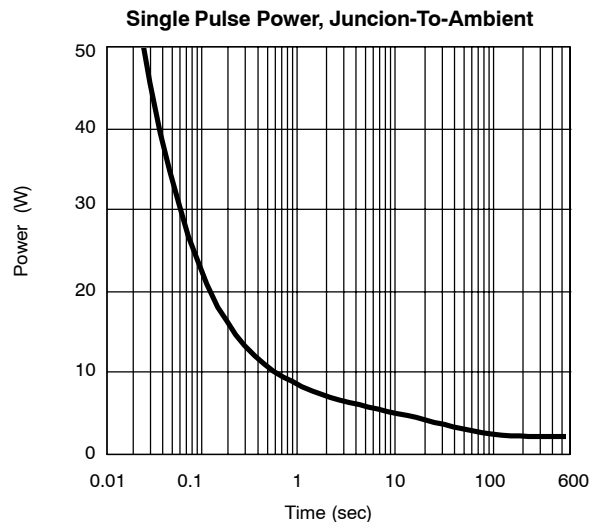
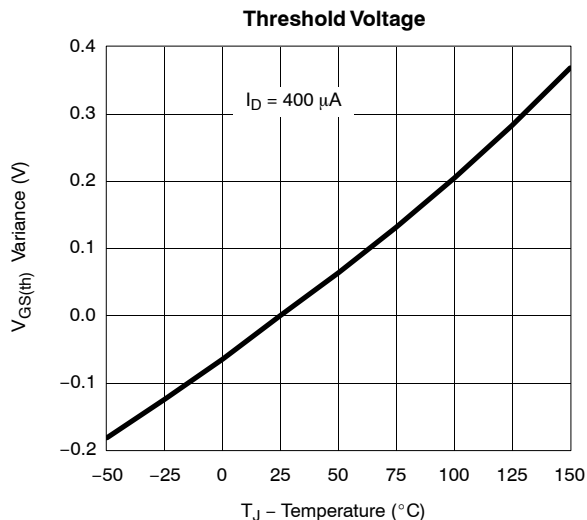
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -400\ \mu\text{A}$	-0.4		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -13.2\ \text{A}$		0.012	0.015	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -11.4\ \text{A}$		0.016	0.020	
		$V_{GS} = -1.8\ \text{V}, I_D = -3.5\ \text{A}$		0.023	0.029	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -13.2\ \text{A}$		47		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -3.2\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -13.2\ \text{A}$		34	51	nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			8.8		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_g = 6\ \Omega$		30	45	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			200	300	
Fall Time	t_f			95	140	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		35	55	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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