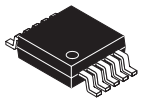
TEXAS INSTRUMENTS



SLUS600 − APRIL 2004

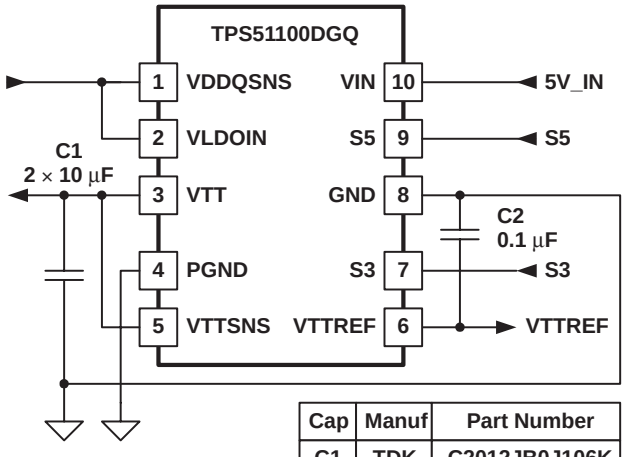
3-A SINK/SOURCE DDR TERMINATION REGULATOR

FEATURES

- **Input Voltage Range: 4.75 V to 5.25 V**
- **VLDOIN Voltage Range: 1.2 V to 3.6 V**
- **3-A Sink/Source Termination Regulator Includes Droop Compensation**
- **Requires Only 20-μF Ceramic Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S5**
- **1.2-V Input (VLDOIN) Helps Reduce Total Power Dissipation**
- **Integrated Divider Tracks $^1/_2$VDDQSNS for VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **± 20-mV Accuracy for VTT and VTTREF**
- **10-mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start, UVLO and OCL**
- **Thermal Shutdown**
- **Supports JEDEC Specifications**

APPLICATIONS

- **DDR I/II Memory Termination**
- **SSTL−2, SSTL−18 and HSTL Termination**



Cap	Manuf	Part Number
C1	TDK	C2012JB0J106K
C2	TDK	C1608JB1H104K

UDG−04015

DESCRIPTION

The TPS51100 is a 3-A sink/source tracking termination regulator. It is specifically designed for low-cost/low-external component count systems, where space is a premium.

The TPS51100 maintains fast transient response only requiring 20-μF (2 × 10μF) of ceramic output capacitance. The TPS51100 supports remote sensing functions and all features required to power the DDR/DDR II VTT bus termination according to the JEDEC specification. In addition, the TPS51100 includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (suspend to disk). The TPS51100 is available in the thermally efficient 10-pin MSOP PowerPAD™ and is specified from −40°C to 85°C.

ORDERING INFORMATION

T_A	PLASTIC MSOP POWER PAD (DGQ)(1)
−40°C to 85°C	TPS51100DGQ

(1) The DGQ package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS51100DGQR). See the application section of the data sheet for PowerPAD drawing and layout information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS51100	UNIT
Input voltage range(2)	VIN, VLDOIN, VTTSNS, VDDQSNS, S3, S5	−0.3 to 6	V
	PGND	−0.3 to 0.3	
Output voltage range(2)	VTT, VTTREF	−0.3 to 6	
Operating ambient temperature range, T_A		−40 to 85	°C
Storage temperature, T_{stg}		−55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		TBD	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

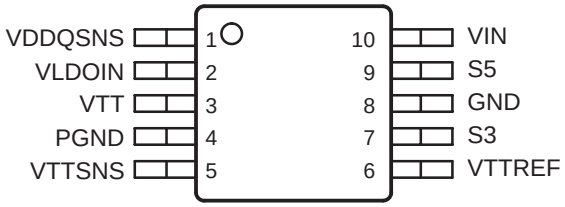
DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10-pin DGQ	1.73 W	17.3 mW/°C	0.694 W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{IN}		4.75	5.25	V
Voltage range	S3, S5	−0.10	5.25	
	VLDOIN, VDDQSNS, VTT, VTTSNS	−0.1	3.6	
	VTTREF	−0.1	1.8	
	PGND	−0.1	0.1	
Operating free-air temperature, T_A		−40	85	°C

(TOP VIEW)
DGQ Package



ACTUAL SIZE
3,05mm x 4,98mm

(4) For more information on the DGQ package, refer to TI Technical Brief, Literature No. SLMA002.
(5) PowerPAD™ heat slug must be connected to GND (pin 8) or electrically isolated from all other pins.

ELECTRICAL CHARACTERISTICS

T_A = −40°C to 85°C, V_{VIN} = 5 V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Supply current, VIN	T_A = 25°C, V_{VIN} = 5 V, no load; $V_{S3} = V_{S5}$ = 5 V	0.25	0.50	1.00	mA
I_{VINSTB}	Standby currrent, VIN	T_A = 25°C, V_{VIN} = 5 V, no load; V_{S3} = 0 V, V_{S5} = 5 V	25	50	80	µA
I_{VINSDN}	Shutdown current, VIN	T_A = 25°C, V_{VIN} = 5 V, no load; $V_{S3} = V_{S5}$ = 0 V, $V_{VLDOIN} = V_{VDDQSNS}$ = 0 V		0.3	1.0	
I_{VLDOIN}	Supply current, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load; $V_{S3} = V_{S5}$ = 5 V	0.7	1.2	2.0	mA
$I_{VLDOINSTB}$	Standby currrent, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load; V_{S3} = 0 V, V_{S5} = 5 V		6	10	µA
$I_{VLDOINSDN}$	Shutdown current, VLDOIN	T_A = 25°C, V_{VIN} = 5 V, no load; $V_{S3} = V_{S5}$ = 0 V		0.3	1.0	
INPUT CURRENT						
$I_{VDDQSNS}$	Input current, VDDQSNS	V_{VIN} = 5 V, $V_{S3} = V_{S5}$ = 5 V	1	3	5	µA
I_{VTTSNS}	Input current, VTTSNS	V_{VIN} = 5 V, $V_{S3} = V_{S5}$ = 5 V	−1.00	−0.25	1.00	
VTT OUTPUT						
V_{VTTSNS}	Output voltage, VTT	$V_{VLDOIN} = V_{VDDQSNS}$ = 2.5 V		1.25		V
		$V_{VLDOIN} = V_{VDDQSNS}$ = 1.8 V		0.9		
$V_{VTTTOL25}$	Output voltage tolerance to VTTREF, VTT	$V_{VLDOIN} = V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 0 A	−20		20	mV
		$V_{VLDOIN} = V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 1.5 A	−30		30	
		$V_{VLDOIN} = V_{VDDQSNS}$ = 2.5 V, $\|I_{VTT}\|$ = 3 A	−40		40	
$V_{VTTTOL18}$	Output voltage tolerance to VTTREF, VTT	$V_{VLDOIN} = V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 0 A	−20		20	
		$V_{VLDOIN} = V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 1 A	−30		30	
		$V_{VLDOIN} = V_{VDDQSNS}$ = 1.8 V, $\|I_{VTT}\|$ = 2 A	−40		40	
$I_{VTTOCLSRC}$	Source current limit, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 0.95$, PGOOD = High	3.0	3.8	6.0	A
		V_{VTT} = 0 V	1.5	2.2	3.0	
$I_{VTTOCLSNK}$	Sink current limit, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right) \times 1.05$, PGOOD = High	3.0	3.6	6.0	
		$V_{VTT} = V_{VDDQ}$	1.5	2.2	3.0	
I_{VTTLK}	Leakage current, VTT	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right)$ = 1.25 V, T_A = 25°C; V_{S3} = 0 V, V_{S5} = 5 V	−1.0	0.5	1.0	µA
$I_{VTTSNSLK}$	Leakage current, VTTSNS	$V_{TT} = \left(\frac{V_{VDDQSNS}}{2}\right)$ = 1.25 V, T_A = 25°C	−1.00	0.01	1.00	
I_{DSCHRG}	Discharge current, VTT	T_A = 25°C, $V_{S3} = V_{S5}$ = 0 V, $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V	10	17		mA

ELECTRICAL CHARACTERISTICS(continued)

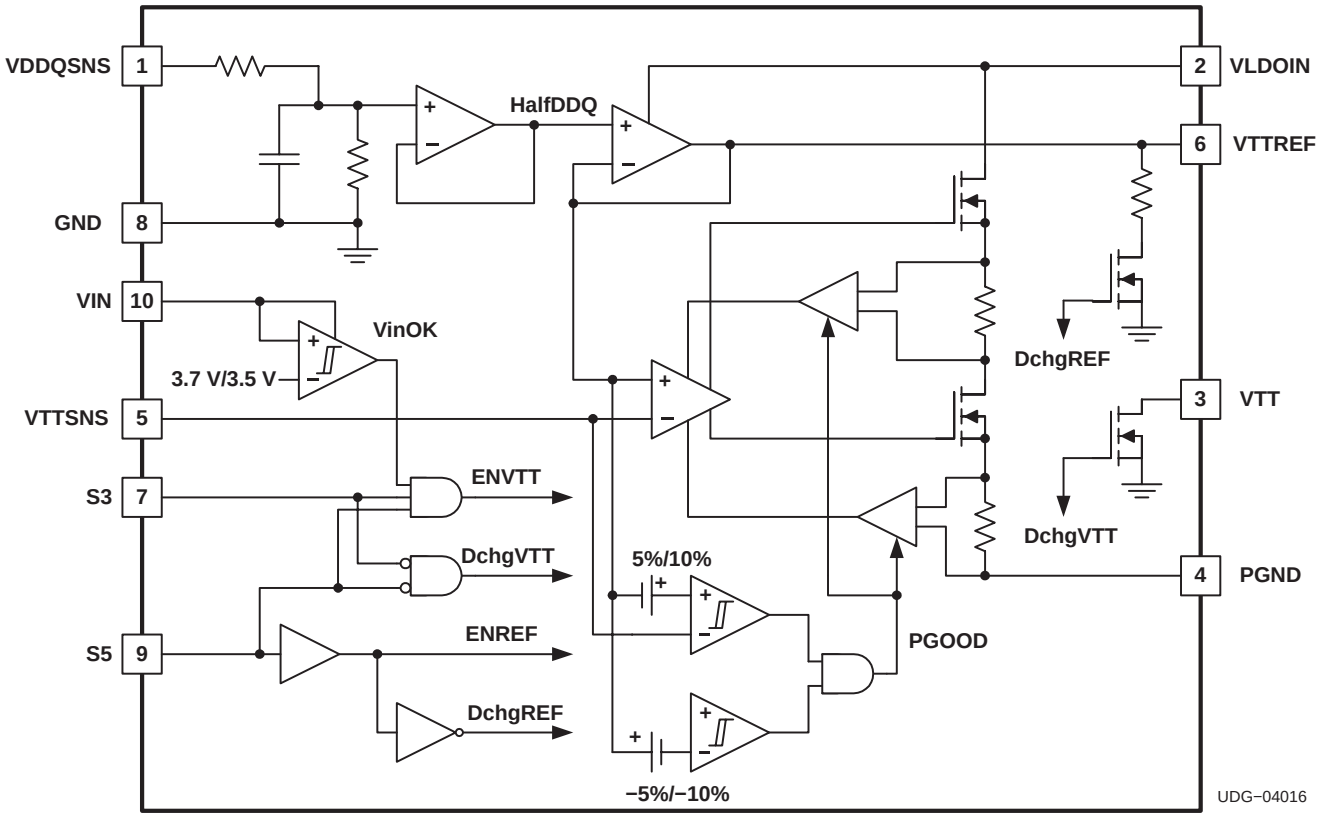
T_A = −40°C to 85°C, V_{VIN} = 5 V, VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VTTREF OUTPUT						
V_{VTTREF}	Output voltage, VTTREF		$V_{TTREF} = \left(\frac{V_{VDDQSNS}}{2}\right)$			V
$V_{VTTREFTOL}$	Output voltage tolerance to VDDQSNS/2	$V_{VLDOIN} = V_{VDDQSNS}$, I_{VTTREF} < 10 mA	−20		20	mV
$I_{VTTREFOCL}$	Source current limit, VTTREF	$V_{VVTTREF}$ = 0 V	10	20	30	mA
UVLO/LOGIC THRESHOLD						
V_{VINUV}	UVLO threshold voltage, VIN	Wake up	3.4	3.7	4.0	V
		Hysteresis	0.15	0.25	0.35	
V_{IH}	High-level input voltage	S3, S5	1.6			
V_{IL}	Low-level input voltage	S3, S5			0.3	
V_{IHYST}	Hysteresis voltage	S3, S5		0.2		
I_{ILEAK}	Logic input leakage current	S2, S5, T_A = 25°C	−1		1	µA
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold voltage	Shutdown temperature	TBD	160	TBD	°C
		Hysteresis		10		

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	8	−	Signal ground. Connect to negative terminal of the output capacitor
PGND	4	−	Power ground output for the VTT LDO
S3	7	I	S3 signal input
S5	9	I	S5 signal input
VDDQSNS	1	I	VDDQ sense input
VIN	10	I	5-V power supply
VLDOIN	2	I	Power supply for the VTT LDO and VTTREF output stage
VTT	3	O	Power output for the VTT LDO
VTTREF	6	O	VTT reference output. Connect to GND through 0.1-µF ceramic capacitor.
VTTSNS	5	I	Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor.

SIMPLIFIED BLOCK DIAGRAM



DETAILED DESCRIPTION

VTT SINK/SOURCE REGULATOR

The TPS51100 is a 3-A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. TPS51100 integrates high-performance low−dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within ±40 mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current line from VTT.

VTTREF REGULATOR

The VTTREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source current up to 10 mA. Bypass VTTREF to GND using a 0.1-µF ceramic capacitor to ensure stable operation.

Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2.2 A. When VTT rises above (VTTREF − 5%) or falls below (VTTREF + 5%) the current limit level switches to 3.8 A. The thresholds are typically VTTREF ±5% (from outside regulation to inside) and ±10% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VTTREF voltage, but also from VDDQ to VTTREF voltage. Note that the VTT output is in a high impedance state during the S3 state (S3 = low, S5 = high) and its voltage can be up to VDDQ voltage depending on the external condition. Note that VTT does not start under a full load condition.

S3, S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. Both VTTREF and VTT are turned on at S0 state (S3 = high, S5 = high). VTTREF is kept alive while VTT is turned off and left high impedance in S3 state (S3 = low, S5 = high). Both VTT and VTTREF outputs are turned off and discharged to the ground through internal MOSFETs during S4/S5 state (both S3 and S5 are low).

Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high−Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

(In case S3 is forced H and S5 to L, VTTREF is discharged and VTT is at High−Z state. This condition is NOT recommended.)

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 3.8 A. This trip point is reduced to 2.2 A before the output voltage comes within ±5% of the target voltage or goes outside of ±10% of the target voltage.

DETAILED DESCRIPTION

VIN UVLO Protection

For VIN undervoltage lockout (UVLO) protection, the TPS51100 monitors VIN voltage. When the VIN voltage is lower than UVLO threshold voltage, the VTT regulator is shut off. This is a non-latch protection.

Thermal Shutdown

TPS51100 monitors its temperature. If the temperature exceeds threshold value, typically 160°C, the VTT and VTTREF regulators are shut off. This is also a non-latch protection.

Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20-µF. Attach two 10-µF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same or slightly lower than the time constant of the output capacitor and its ESR.

Soft-start duration, T_{SS}, is also a function of this output capacitance. Where I_{TTOCL} = 2.2 A (typ), T_{SS} can be calculated as,

$$T_{SS} = \left(\frac{C_{OUT} \times V_{VTT}}{I_{VTTOCL}} \right) \quad (1)$$

Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the part, transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-µF (or more) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT. In general, use 1/2 C_{OUT} for input.

VIN Capacitor

Add a ceramic capacitor with a value between 1.0-µF and 4.7-µF placed close to the VIN pin, to stabilize 5-V from any parasitic impedance from the supply.

Thermal design

As the TPS51100 is a linear regulator, the VTT current flow in both source and sink directions generate power dissipation from the device. In the source phase, the potential difference between V_{VLDOIN} and V_{VTT} times VTT current becomes the power dissipation, W_{DSRC}.

$$W_{DSRC} = \left(V_{VLDOIN} - V_{VTT} \right) \times I_{VTT} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than V_{DDQ} voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, and W_{DSNK}, is calculated by:

$$W_{DSNK} = V_{VTT} \times I_{VTT} \quad (3)$$

Since the device does not sink and source the current at the same time and I_{VTT} varies rapidly with time, actual power dissipation need to be considered for thermal design is an average of above value over thermal relaxation duration of the system. Another power consumption is the current used for internal control circuitry from VIN supply and VLDOIN supply. This can be estimated as 20 mW or less at normal operational conditions. This power needs to be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by,

DETAILED DESCRIPTION

$$W_{PKG} = \frac{\left(T_{J(max)} - T_{A(max)}\right)}{\theta_{JA}} \quad (4)$$

where

- $T_{J(max)}$ is 125°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on the board layout. TPS51100 is assembled in a thermally enhanced PowerPAD™ package that has exposed die pad underneath the body. For improved thermal performance, this die pad needs to be attached to ground trace via thermal land on the PCB. This ground trace acts as a heat sink/spread. The typical thermal resistance, 57.7°C/W, is achieved based on a 3 mm × 2 mm thermal land with 2 vias without air flow. It can be improved by using larger thermal land and/or increasing vias number. For example, assuming 3 mm × 3 mm thermal land with 4 vias without air flow, it is 45.4°C/W. Further information about PowerPAD™ and its recommended board layout is described in the application note (SLMA002). This document is available at www.ti.com.

LAYOUT CONSIDERATIONS

Consider the following points before the layout of TPS51100 design begins.

- The input bypass capacitor for VLDOIN should be placed to the pin as close as possible with short and wide connection.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
- Consider adding LPF at VTTSNS in case ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- Negative node of VTT output capacitor(s) and VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
- GND (Signal GND) pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (Power GND) should be isolated, with a single point connection between them.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Wide trace of the component−side copper, connected to this thermal land, will help heat spreading. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder−side ground plane(s) should be used to help dissipation.

TYPICAL CHARACTERISTICS

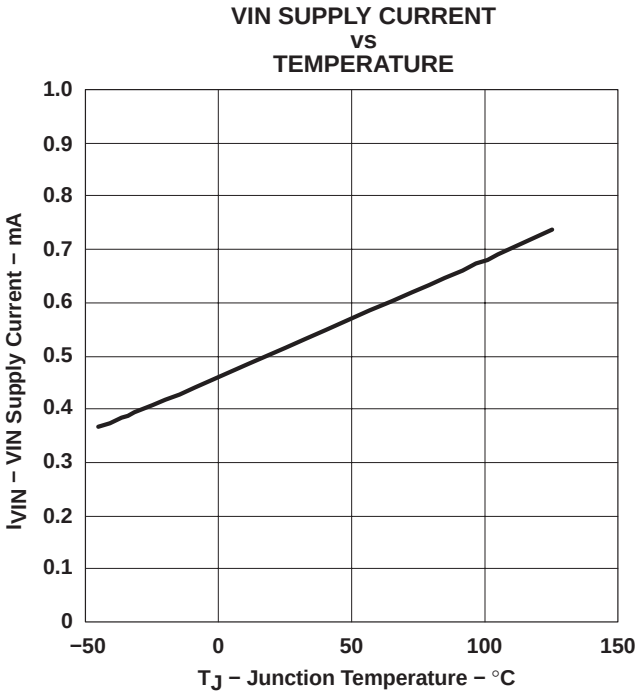


Figure 1

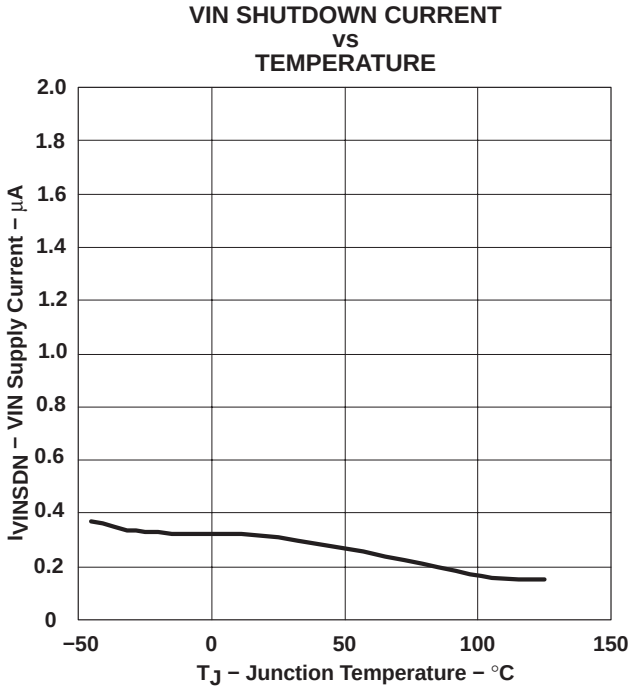


Figure 2

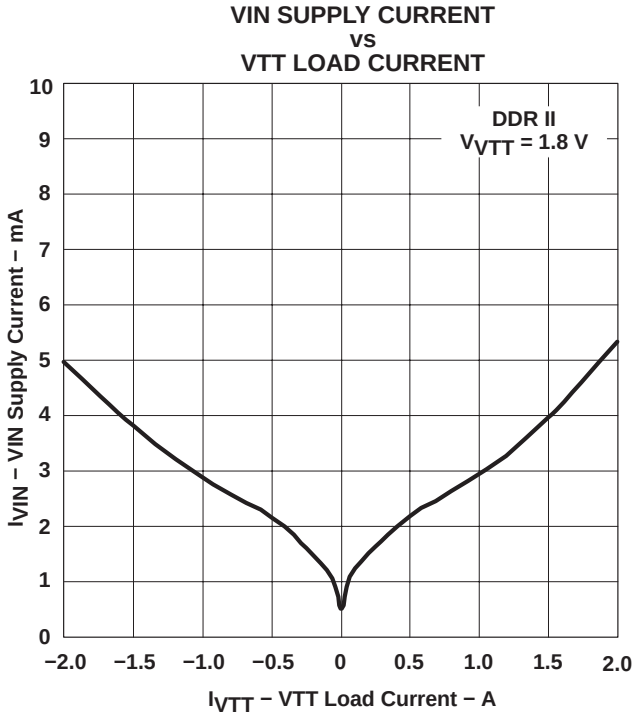


Figure 3

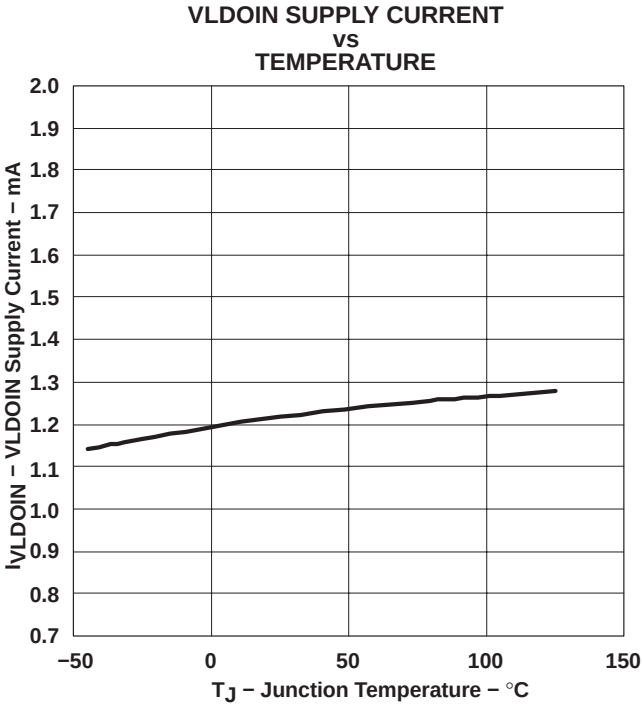


Figure 4

TYPICAL CHARACTERISTICS

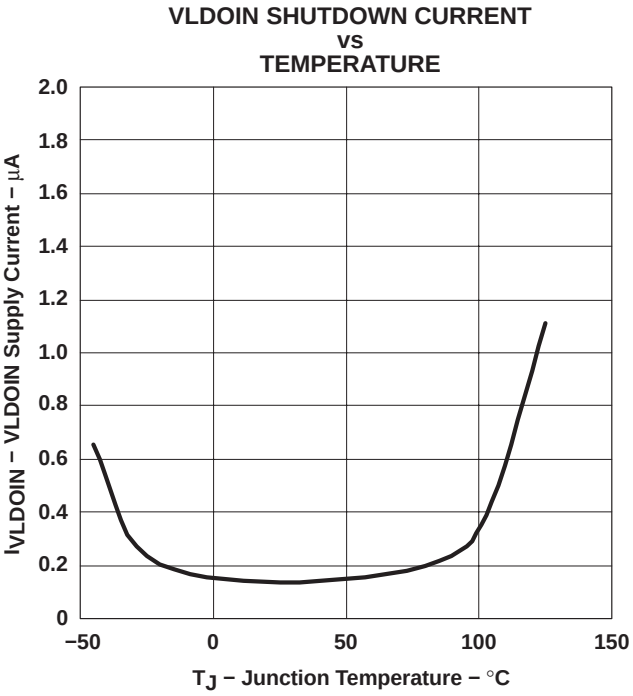


Figure 5

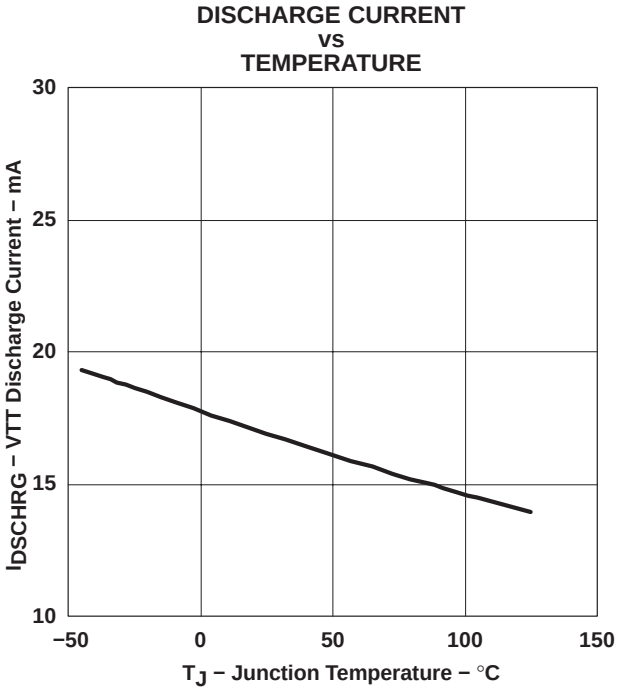


Figure 6

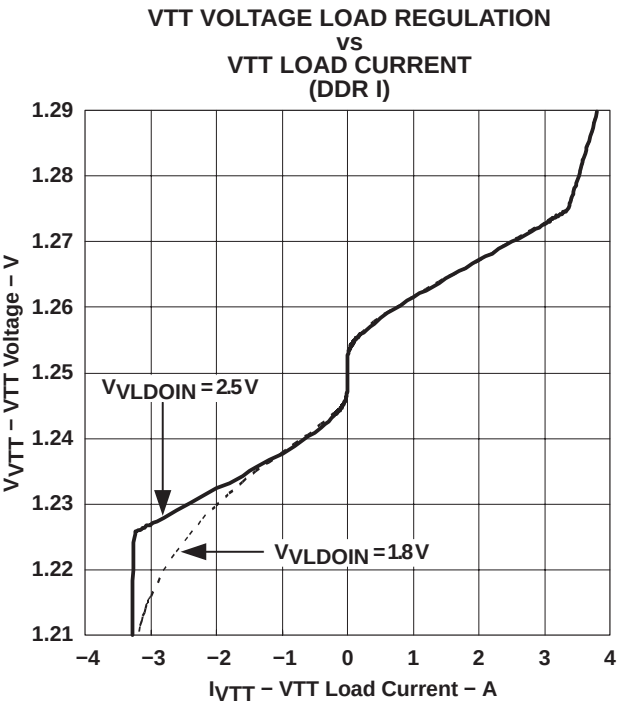


Figure 7

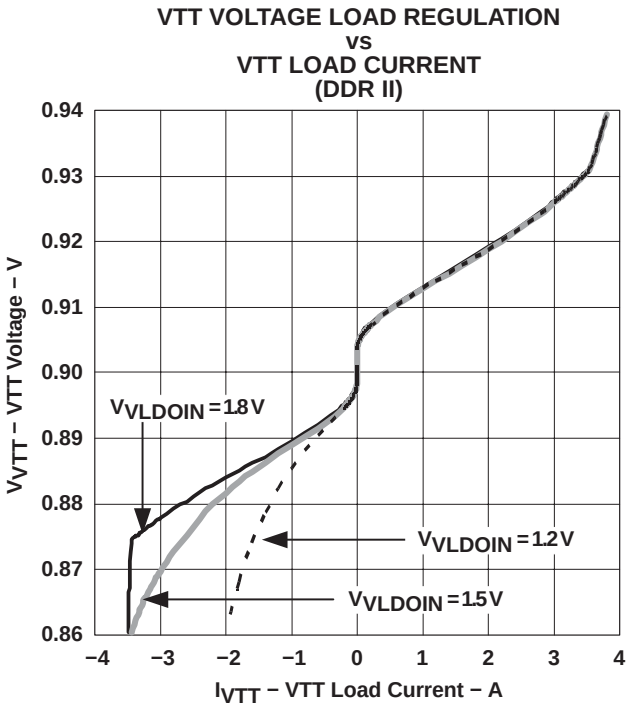


Figure 8

TYPICAL CHARACTERISTICS

VTTREF VOLTAGE LOAD REGULATION vs VTTREF LOAD CURRENT (DDR I)

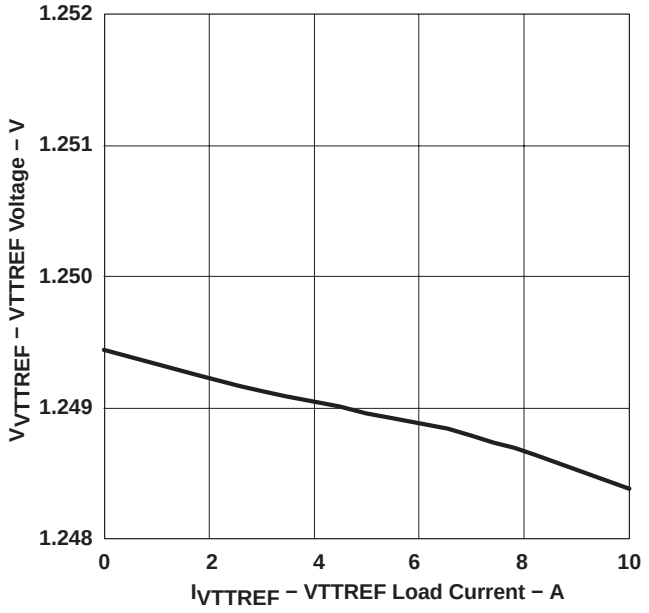


Figure 9

VTTREF VOLTAGE LOAD REGULATION vs VTTREF LOAD CURRENT (DDR II)

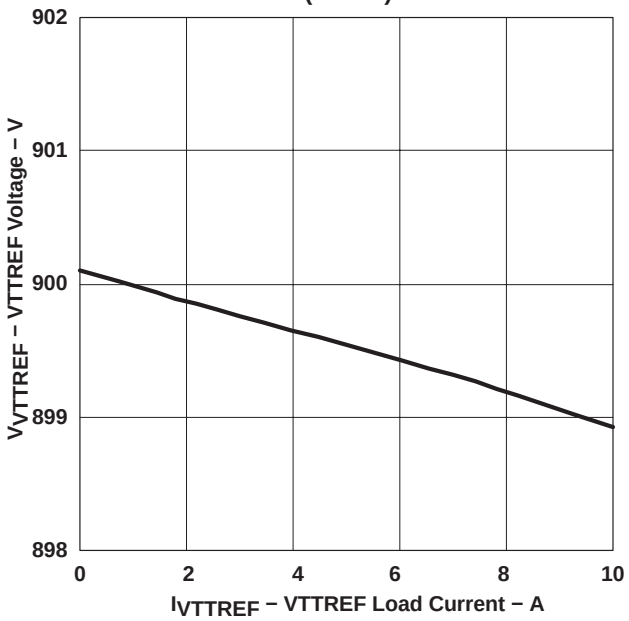


Figure 10

VTT VOLTAGE LOAD TRANSIENT RESPONSE

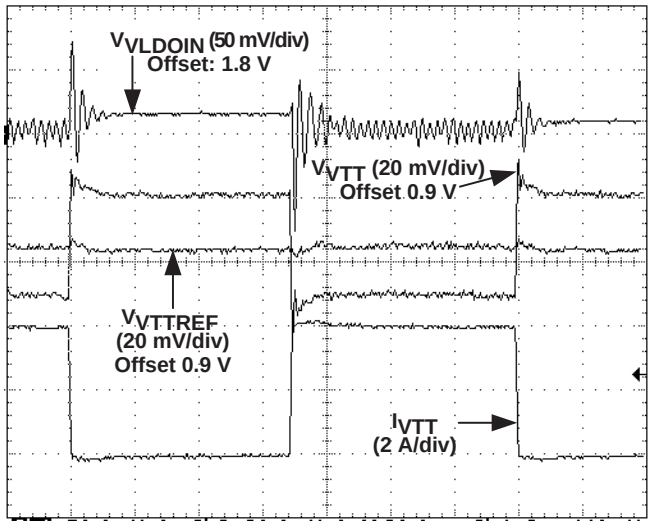
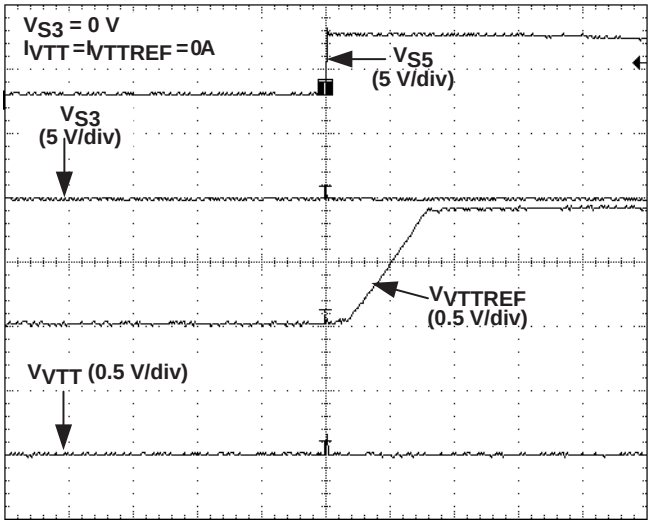


Figure 11

TYPICAL CHARACTERISTICS

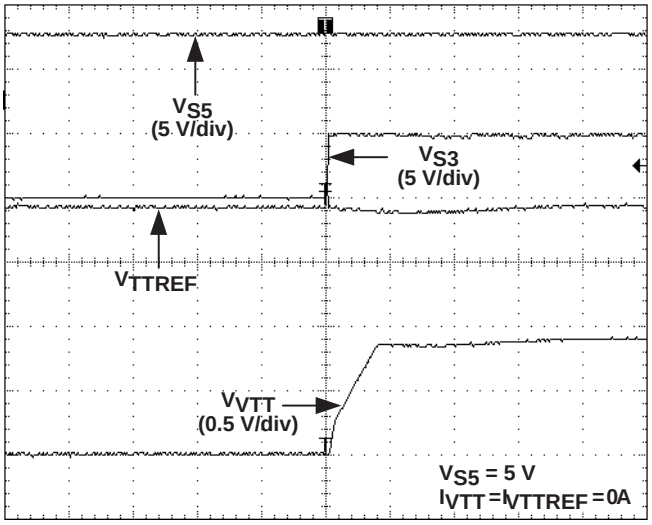
STARTUP WAVEFORMS
S5 LOW−TO−HIGH



t − Time − 10 μs/div

Figure 12

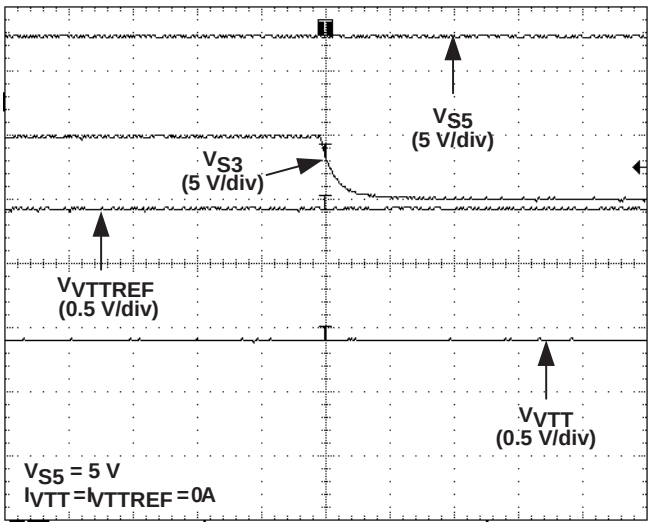
STARTUP WAVEFORMS
S3 LOW−TO−HIGH



t − Time − 10 μs/div

Figure 13

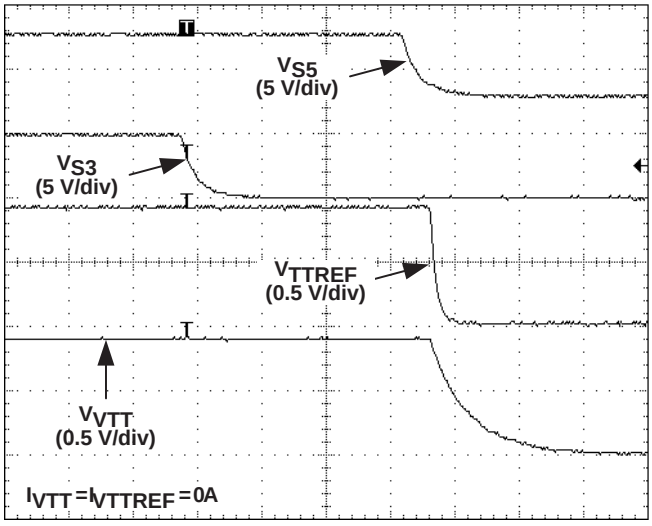
SHUTDOWN WAVEFORMS
S3 HIGH-TO-LOW



t − Time − 1 ms/div

Figure 14

SHUTDOWN WAVEFORMS
S3 AND S5 HIGH-TO-LOW



t − Time − 1 ms/div

Figure 15

TYPICAL CHARACTERISTICS

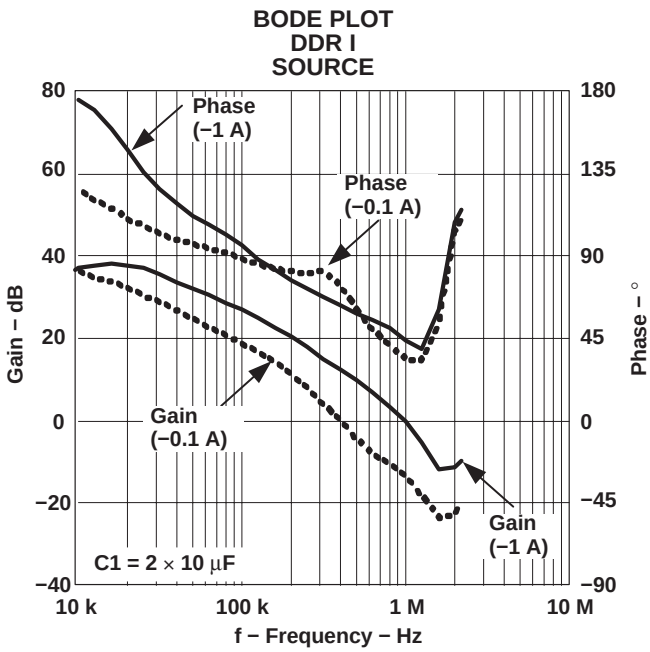


Figure 16

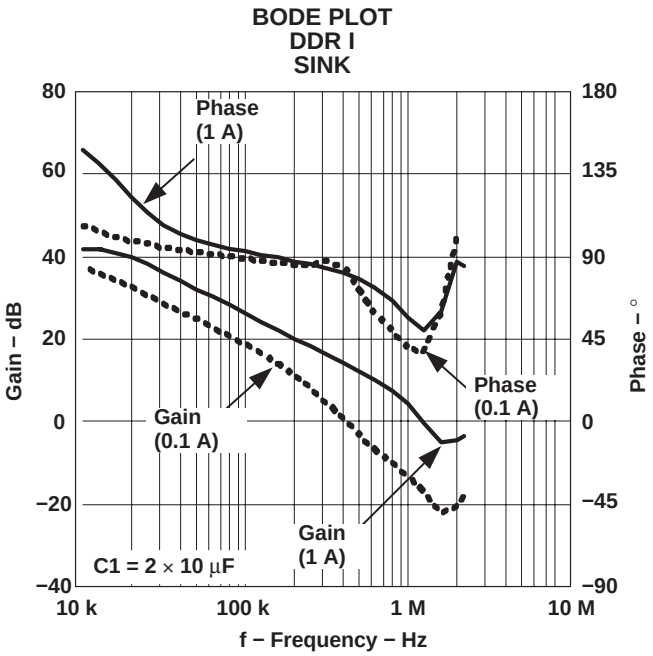


Figure 17

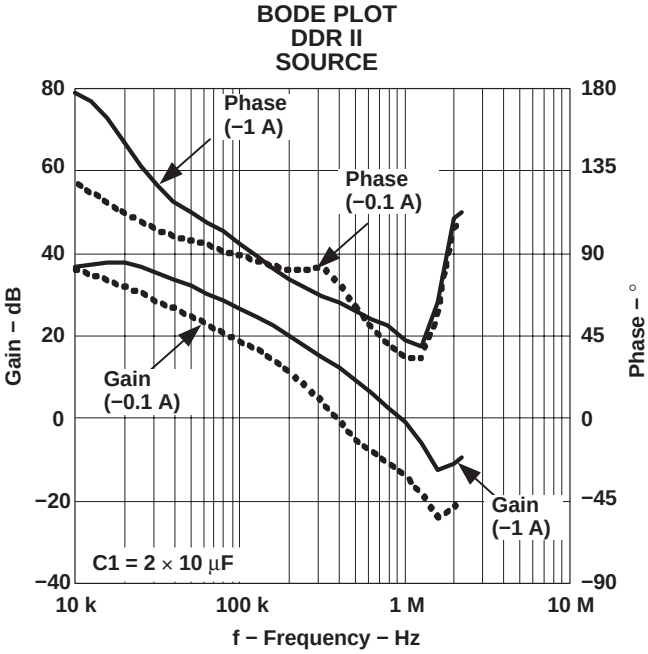


Figure 18

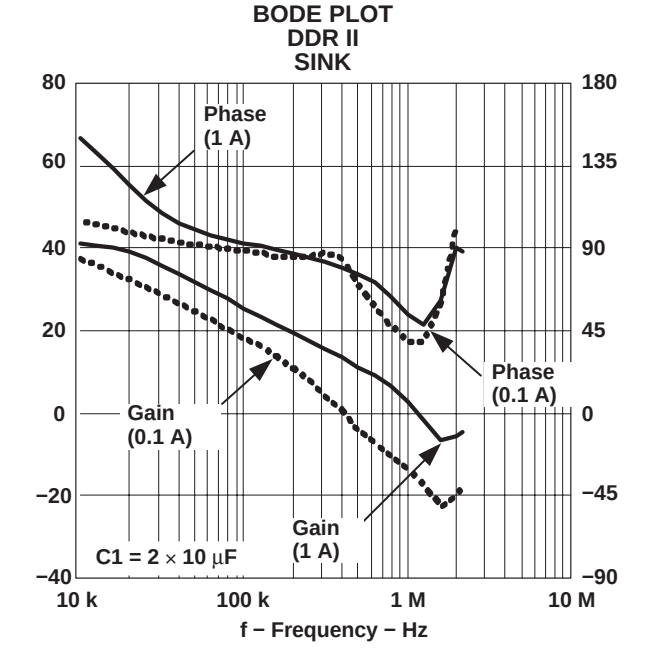
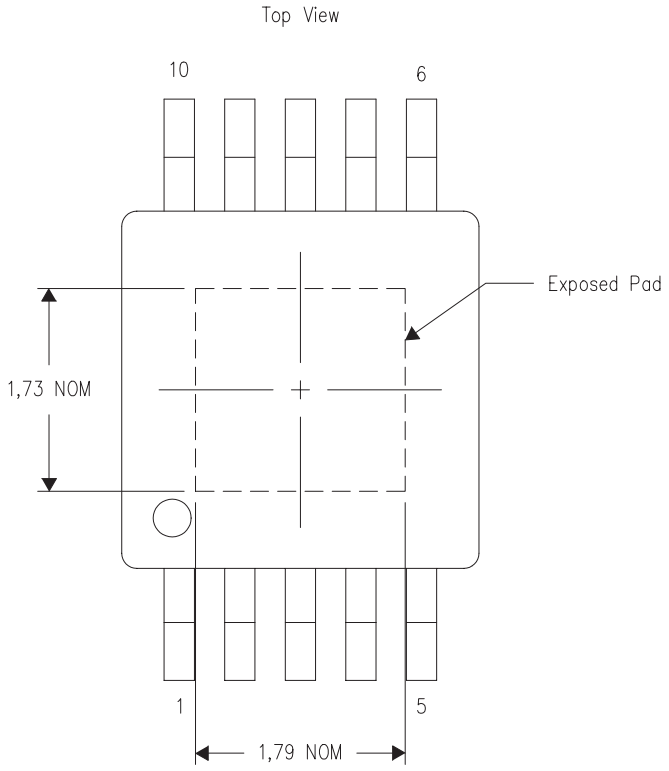


Figure 19

THERMAL PAD MECHANICAL DATA

DGQ (S–PDSO–G10) **PowerPAD™ PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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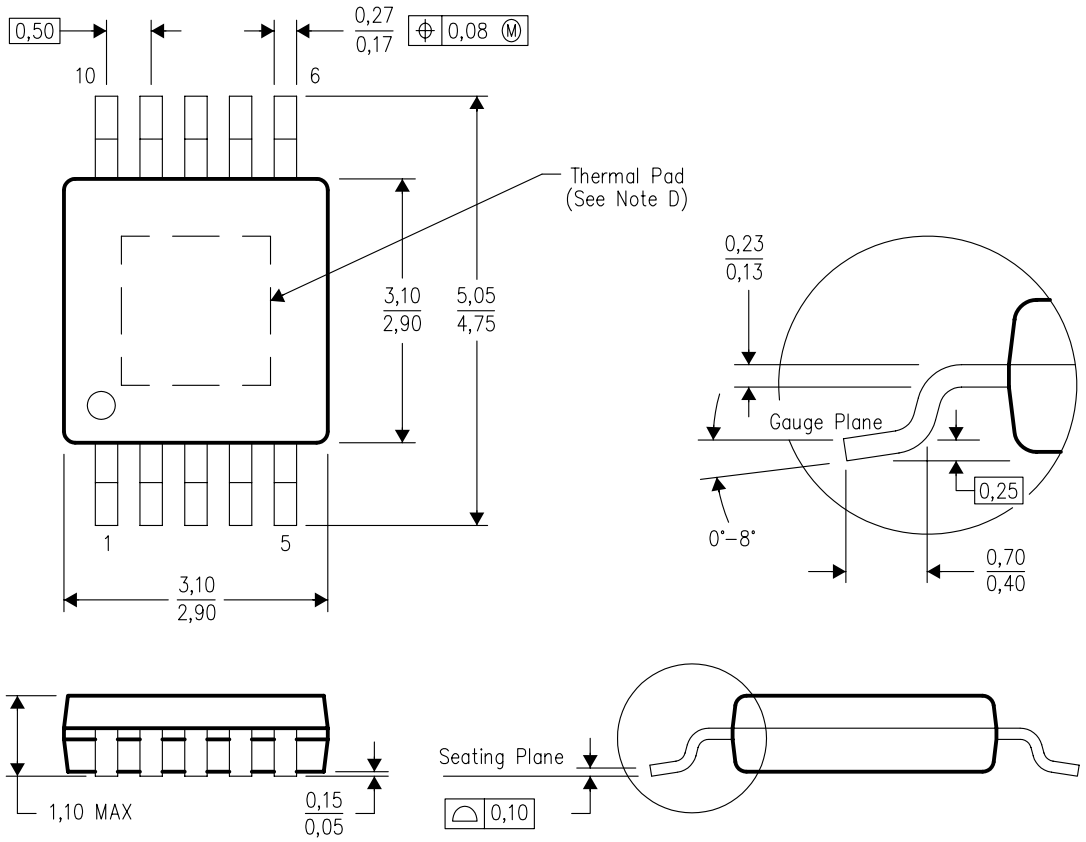
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073273/D 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

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