

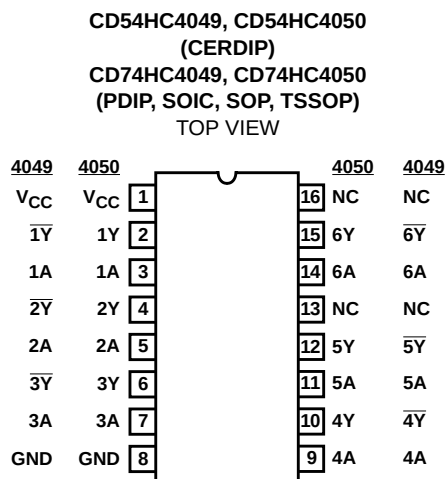
February 1998 - Revised February 2005

## High-Speed CMOS Logic Hex Buffers, Inverting and Non-Inverting

### Features

- Typical Propagation Delay: 6ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- High-to-Low Voltage Level Converter for up to  $V_I = 16V$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$

### Pinout



### Description

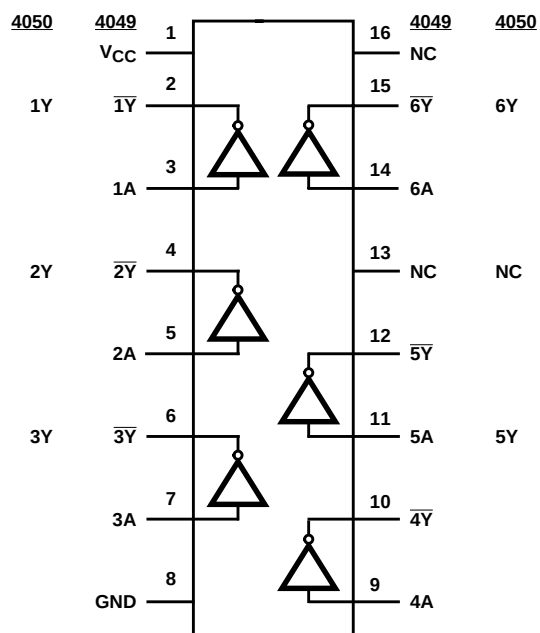
The 'HC4049 and 'HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15-V input pulse levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. These parts also can be used as simple buffers or inverters without level translation. The 'HC4049 and 'HC4050 are enhanced versions of equivalent CMOS types.

### Ordering Information

| PART NUMBER   | TEMP. RANGE<br>(°C) | PACKAGE      |
|---------------|---------------------|--------------|
| CD54HC4049F3A | -55 to 125          | 16 Ld CERDIP |
| CD54HC4050F3A | -55 to 125          | 16 Ld CERDIP |
| CD74HC4049E   | -55 to 125          | 16 Ld PDIP   |
| CD74HC4049M   | -55 to 125          | 16 Ld SOIC   |
| CD74HCT4050MT | -55 to 125          | 16 Ld SOIC   |
| CD74HC4049M96 | -55 to 125          | 16 Ld SOIC   |
| CD74HC4049NSR | -55 to 125          | 16 Ld SOP    |
| CD74HC4049PW  | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4049PWR | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4049PWT | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050E   | -55 to 125          | 16 Ld PDIP   |
| CD74HC4050M   | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050MT  | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050M96 | -55 to 125          | 16 Ld SOIC   |
| CD74HC4050NSR | -55 to 125          | 16 Ld SOP    |
| CD74HC4050PW  | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050PWR | -55 to 125          | 16 Ld TSSOP  |
| CD74HC4050PWT | -55 to 125          | 16 Ld TSSOP  |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

## Functional Diagram



## Logic Diagrams

HC4049



HC4050



# CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

## Absolute Maximum Ratings

|                                                        |              |
|--------------------------------------------------------|--------------|
| DC Supply Voltage, $V_{CC}$                            | −0.5V to 7V  |
| Input Voltage Range                                    | −0.5V to 16V |
| DC Input Diode Current, $I_{IK}$                       |              |
| For $V_I < -0.5V$                                      | −20mA        |
| DC Output Diode Current, $I_{OK}$                      |              |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | ±20mA        |
| DC Output Source or Sink Current per Output Pin, $I_O$ |              |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | ±25mA        |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$   | ±50mA        |

## Operating Conditions

|                                |                |
|--------------------------------|----------------|
| Temperature Range ( $T_A$ )    | −55°C to 125°C |
| Supply Voltage Range, $V_{CC}$ |                |
| HC Types                       | .2V to 6V      |
| HCT Types                      | 4.5V to 5.5V   |
| DC Input Voltage, $V_I$        | .0V to 15V     |
| DC Output Voltage, $V_O$       | 0V to $V_{CC}$ |
| Input Rise and Fall Time       |                |
| 2V                             | 1000ns (Max)   |
| 4.5V                           | 500ns (Max)    |
| 6V                             | 400ns (Max)    |

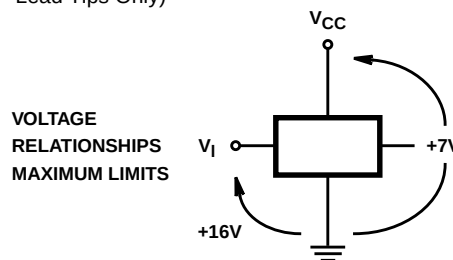
**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## Thermal Information

|                                                        |                |
|--------------------------------------------------------|----------------|
| Package Thermal Impedance, $\theta_{JA}$ (see Note 1): |                |
| E (PDIP) Package                                       | 67°C/W         |
| M (SOIC) Package                                       | 73°C/W         |
| NS (SOP) Package                                       | 64°C/W         |
| PW (TSSOP) Package                                     | 108°C/W        |
| Maximum Junction Temperature (Hermetic Package or Die) | 175°C          |
| Maximum Junction Temperature (Plastic Package)         | 150°C          |
| Maximum Storage Temperature Range                      | −65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s)               | 300°C          |
| (SOIC - Lead Tips Only)                                |                |



## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | −40°C TO 85°C |      | −55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | −0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | −0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | −0.02               | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  |                 |                                    | −4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                    | −5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   |                 |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |
|                                         |                 | 15                                 | -                   | 6                   | -    | -   | ±0.5 | -             | ±5   | -              | ±5   |       |

# CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

## DC Electrical Specifications (Continued)

| PARAMETER                | SYMBOL          | TEST CONDITIONS        |                     | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------|-----------------|------------------------|---------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                          |                 | V <sub>I</sub> (V)     | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Quiescent Device Current | I <sub>CC</sub> | V <sub>CC</sub> or GND | 0                   | 6                   | -    | -   | 2   | -             | 20  | -              | 40  | μA    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                                | SYMBOL                              | TEST<br>CONDITIONS    | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO<br>85°C |     | -55°C TO<br>125°C |     | UNITS |
|----------------------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|------------------|-----|-------------------|-----|-------|
|                                                          |                                     |                       |                     | MIN  | TYP | MAX | MIN              | MAX | MIN               | MAX |       |
| HC TYPES                                                 |                                     |                       |                     |      |     |     |                  |     |                   |     |       |
| Propagation Delay,<br>nA to nY HC4049<br>nA to nY HC4050 | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 85  | -                | 105 | -                 | 130 | ns    |
|                                                          |                                     |                       | 4.5                 | -    | -   | 17  | -                | 21  | -                 | 26  | ns    |
|                                                          |                                     |                       | 6                   | -    | -   | 14  | -                | 18  | -                 | 22  | ns    |
|                                                          |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 6   | -   | -                | -   | -                 | -   | ns    |
| Transition Times (Figure 1)                              | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -                | 95  | -                 | 110 | ns    |
|                                                          |                                     |                       | 4.5                 | -    | -   | 15  | -                | 19  | -                 | 22  | ns    |
|                                                          |                                     |                       | 6                   | -    | -   | 13  | -                | 16  | -                 | 19  | ns    |
| Input Capacitance                                        | C <sub>I</sub>                      | -                     | -                   | -    | -   | 10  | -                | 10  | -                 | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 2, 3)            | C <sub>PD</sub>                     | -                     | 5                   | -    | 35  | -   | -                | -   | -                 | -   | pF    |

### NOTES:

- C<sub>PD</sub> is used to determine the dynamic power consumption, per gate.
- P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

## Test Circuit and Waveform

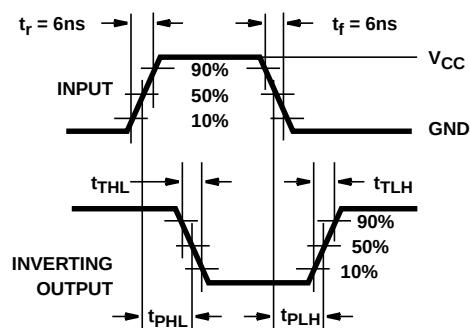


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8681901EA   | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| 5962-8682001EA   | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD54HC4049F3A    | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD54HC4050F3A    | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | Call TI          | Level-NC-NC-NC               |
| CD74HC4049E      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HC4049M      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049M96    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049M96E4  | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049ME4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049MT     | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049MTE4   | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049NSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049NSRE4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PW     | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PWE4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PWR    | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PWRE4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PWT    | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4049PWTE4  | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050E      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HC4050EE4    | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC               |
| CD74HC4050M      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050M96    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050M96E4  | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050ME4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050MT     | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050MTE4   | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| no Sb/Br)        |                       |              |                 |      |             |                         |                  |                              |
| CD74HC4050NSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050NSRE4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PW     | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PWG4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PWR    | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PWG4   | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PWT    | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC4050PWTG4  | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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| Logic            | <a href="http://logic.ti.com">logic.ti.com</a>                     | Military            | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt       | <a href="http://power.ti.com">power.ti.com</a>                     | Optical Networking  | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Microcontrollers | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> | Security            | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
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