

High Performance Pin Driver



The EL7155 high performance pin driver with 3-state is suited to many ATE and level-shifting applications.

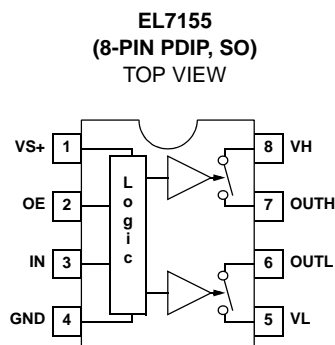
The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads.

Output pins OUT_H and OUT_L are connected to input pins V_H and V_L respectively, depending on the status of the IN pin. One of the output pins is always in tri-state, except when the OE pin is active low, in which case both outputs are in 3-state mode. The isolation of the output FETs from the power supplies enables V_H and V_L to be set independently, enabling level-shifting to be implemented.

This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and on-resistance characteristics.

Available in 8-Pin SO and 8-Pin PDIP packages, the EL7155 is specified for operation over the full -40°C to $+85^{\circ}\text{C}$ temperature range.

Pinout



Features

- Clocking speeds up to 40MHz
- 15ns tr/td at 2000pF C_{LOAD}
- 0.5ns rise and fall times mismatch
- 0.5ns $T_{ON}-T_{OFF}$ prop delay mismatch
- 3.5pF typical input capacitance
- 3.5A peak drive
- Low on resistance of 3.5Ω
- High capacitive drive capability
- Operates from 4.5V up to 18V

Applications

- ATE/burn-in testers
- Level shifting
- IGBT drivers
- CCD drivers

Ordering Information

| PART NUMBER | PACKAGE | TAPE & REEL | PKG. NO. |
|--------------|------------|-------------|----------|
| EL7155CN | 8-Pin PDIP | - | MDP0031 |
| EL7155CS | 8-Pin SO | - | MDP0027 |
| EL7155CS-T7 | 8-Pin SO | 7" | MDP0027 |
| EL7155CS-T13 | 8-Pin SO | 13" | MDP0027 |

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage (V_{S+} to V_L) +18V
 Input Voltage $V_L - 0.3\text{V}$, $V_L + 0.3\text{V}$
 Continuous Output Current 200mA
 Storage Temperature Range -65°C to $+150^\circ\text{C}$

Ambient Operating Temperature -40°C to $+85^\circ\text{C}$
 Operating Junction Temperature 125°C
 Power Dissipation see curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

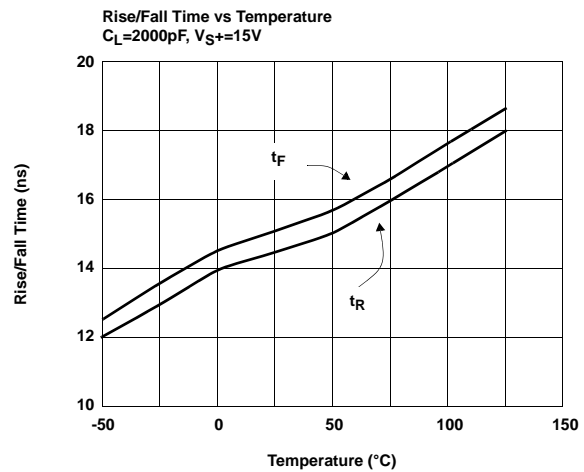
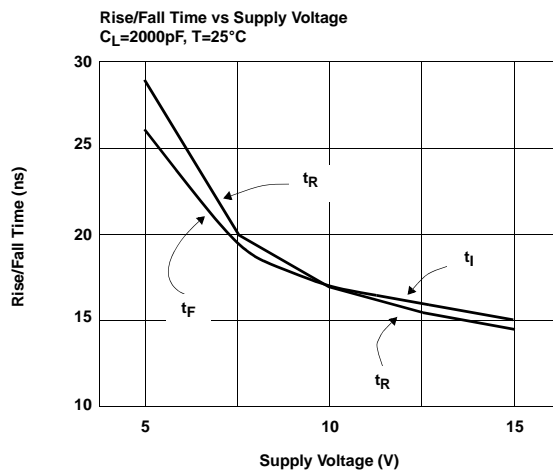
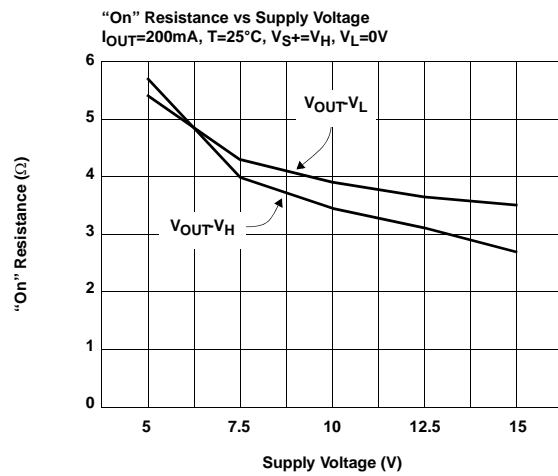
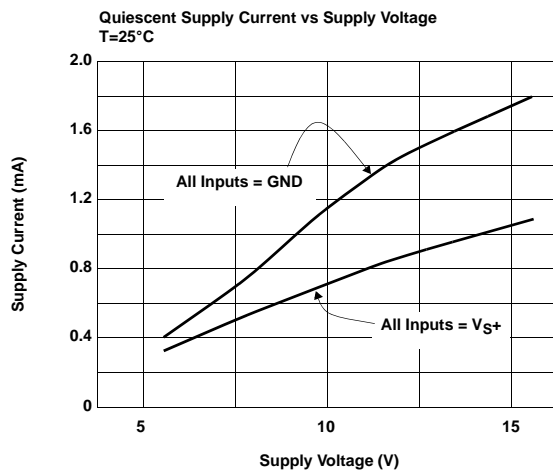
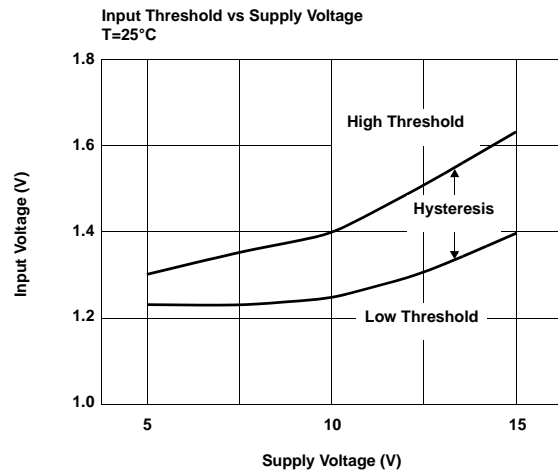
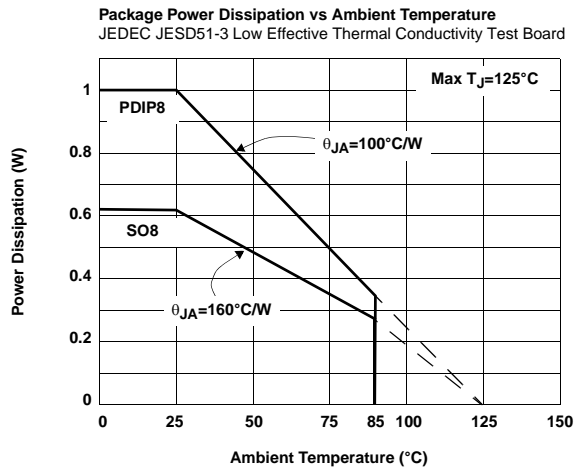
Electrical Specifications $V_{S+} = +15\text{V}$, $V_H = +15\text{V}$, $V_L = 0\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN | TYP | MAX | UNIT |
|----------------------------------|---|---|-----|------|-----|---------------|
| INPUT | | | | | | |
| V_{IH} | Logic '1' Input Voltage | | 2.4 | | | V |
| I_{IH} | Logic '1' Input Current | $V_{IH} = V_{S+}$ | | 0.1 | 10 | μA |
| V_{IL} | Logic '0' Input Voltage | | | | 0.8 | V |
| I_{IL} | Logic '0' Input Current | $V_{IL} = 0\text{V}$ | | 0.1 | 10 | μA |
| C_{IN} | Input Capacitance | | | 3.5 | | pF |
| R_{IN} | Input Resistance | | | 50 | | M Ω |
| OUTPUT | | | | | | |
| R_{OVH} | ON Resistance V_H to OUT_H | $I_{OUT} = -200\text{mA}$ | | 2.7 | 4.5 | Ω |
| R_{OVL} | ON Resistance V_L to OUT_L | $I_{OUT} = +200\text{mA}$ | | 3.5 | 5.5 | Ω |
| I_{OUT} | Output Leakage Current | $OE = 0\text{V}$, $OUT_H = V_L$, $OUT_L = V_{S+}$ | | 0.1 | 10 | μA |
| I_{PK} | Peak Output Current (linear resistive operation) | Source | | 3.5 | | A |
| | | Sink | | 3.5 | | A |
| I_{DC} | Continuous Output Current | Source/Sink | 200 | | | mA |
| POWER SUPPLY | | | | | | |
| I_S | Power Supply Current | Inputs = V_{S+} | | 1.3 | 3 | mA |
| I_{VH} | Off Leakage at V_H | $V_H = 0\text{V}$ | | 4 | 10 | μA |
| SWITCHING CHARACTERISTICS | | | | | | |
| t_R | Rise Time | $C_L = 2000\text{pF}$ | | 14.5 | | ns |
| t_F | Fall Time | $C_L = 2000\text{pF}$ | | 15 | | ns |
| $t_{R\Delta}$ | t_R , t_F Mismatch | $C_L = 2000\text{pF}$ | | 0.5 | | ns |
| t_{D-1} | Turn-Off Delay Time | $C_L = 2000\text{pF}$ | | 9.5 | | ns |
| t_{D-2} | Turn-On Delay Time | $C_L = 2000\text{pF}$ | | 10 | | ns |
| $t_{D\Delta}$ | t_{D-1} - t_{D-2} Mismatch | $C_L = 2000\text{pF}$ | | 0.5 | | ns |
| t_{D-3} | 3-state Delay Enable | | | 10 | | ns |
| t_{D-4} | 3-state Delay Disable | | | 10 | | ns |

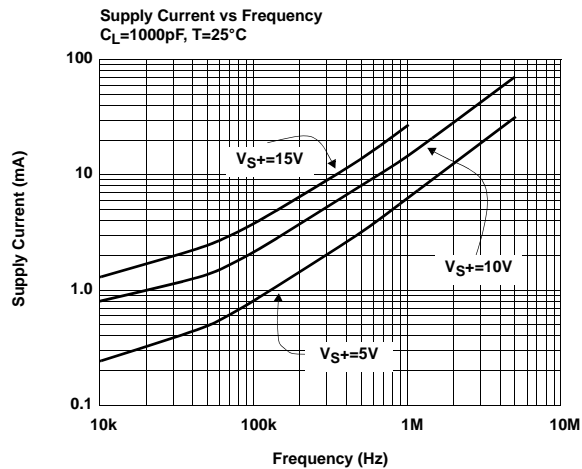
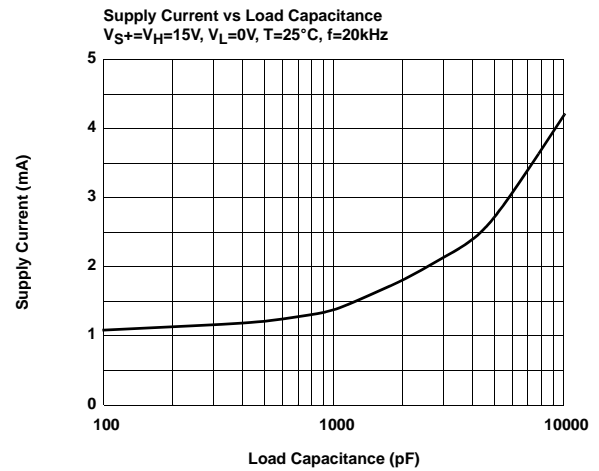
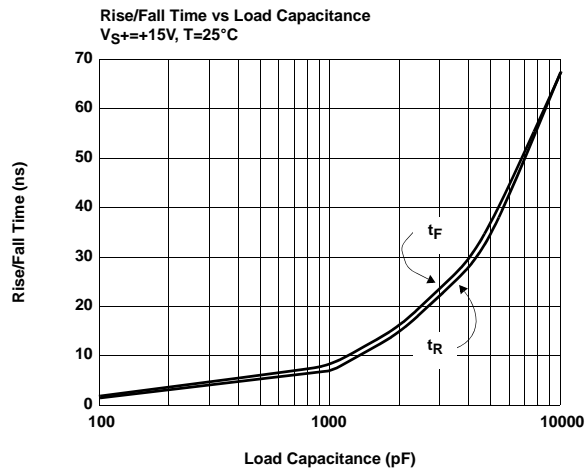
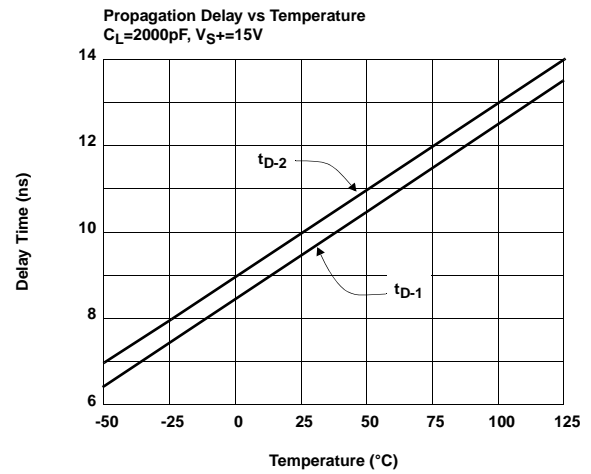
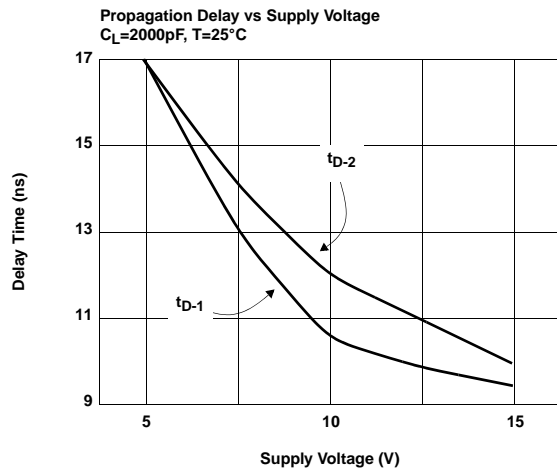
Electrical Specifications $V_{S+} = +5V$, $V_H = +5V$, $V_L = -5V$, $T_A = 25^\circ C$, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN | TYP | MAX | UNIT |
|----------------------------------|---|--|-----|------|-----|------------|
| INPUT | | | | | | |
| V_{IH} | Logic '1' Input Voltage | | 2.0 | | | V |
| I_{IH} | Logic '1' Input Current | $V_{IH} = V_{S+}$ | | 0.1 | 10 | μA |
| V_{IL} | Logic '0' Input Voltage | | | | 0.8 | V |
| I_{IL} | Logic '0' Input Current | $V_{IL} = 0V$ | | 0.1 | 10 | μA |
| C_{IN} | Input Capacitance | | | 3.5 | | pF |
| R_{IN} | Input Resistance | | | 50 | | M Ω |
| OUTPUT | | | | | | |
| R_{OVH} | ON Resistance V_H to OUT_H | $I_{OUT} = -200mA$ | | 3.4 | 5 | Ω |
| R_{OVL} | ON Resistance V_L to OUT_L | $I_{OUT} = +200mA$ | | 4 | 6 | Ω |
| I_{OUT} | Output Leakage Current | $OE = 0V$, $OUT_H = V_L$, $OUT_L = V_{S+}$ | | 0.1 | 10 | μA |
| I_{PK} | Peak Output Current (linear resistive operation) | Source | | 3.5 | | A |
| | | Sink | | 3.5 | | A |
| I_{DC} | Continuous Output Current | Source/Sink | 200 | | | mA |
| POWER SUPPLY | | | | | | |
| I_S | Power Supply Current | Inputs = V_{S+} | | 1 | 2.5 | mA |
| I_{VH} | Off Leakage at V_H | $V_H = 0V$ | | 4 | 10 | μA |
| SWITCHING CHARACTERISTICS | | | | | | |
| t_R | Rise Time | $C_L = 2000pF$ | | 17 | | ns |
| t_F | Fall Time | $C_L = 2000pF$ | | 17 | | ns |
| $t_{RF\Delta}$ | t_R , t_F Mismatch | $C_L = 2000pF$ | | 0 | | ns |
| t_{D-1} | Turn-Off Delay Time | $C_L = 2000pF$ | | 11.5 | | ns |
| t_{D-2} | Turn-On Delay Time | $C_L = 2000pF$ | | 12 | | ns |
| $t_{D\Delta}$ | t_{D-1} - t_{D-2} Mismatch | $C_L = 2000pF$ | | 0.5 | | ns |
| t_{D-3} | 3-state Delay Enable | | | 11 | | ns |
| t_{D-4} | 3-state Delay Disable | | | 11 | | ns |

Typical Performance Curves



Typical Performance Curves (Continued)



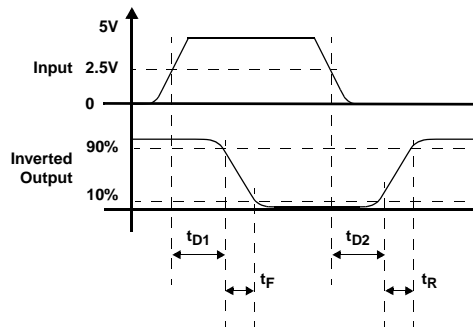
Truth Table

| OE | IN | V _H TO OUT _H | OUT _L TO V _{S-} |
|----|----|------------------------------------|-------------------------------------|
| 0 | 0 | Open | Open |
| 0 | 1 | Open | Open |
| 1 | 0 | Closed | Open |
| 1 | 1 | Open | Closed |

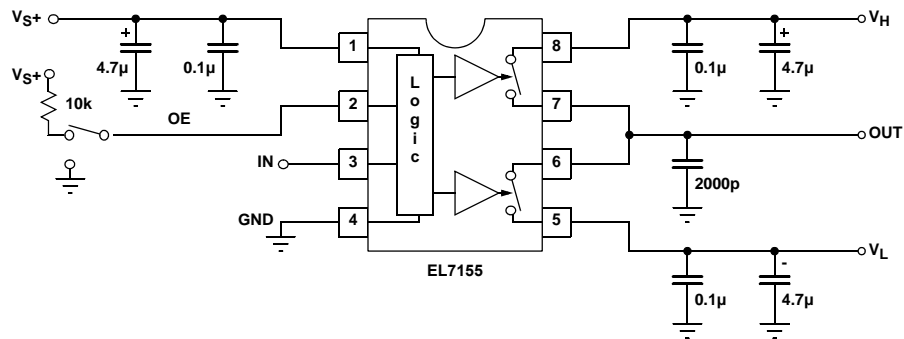
Operating Voltage Range

| PIN | MIN | MAX |
|----------------------------------|----------------|----------------|
| GND - V _L | -5 | 0 |
| V _{S+} - V _L | 5 | 18 |
| V _H - V _L | 0 | 18 |
| V _{S+} - V _H | 0 | 18 |
| V _{S+} - GND | 5 | 18 |
| 3-state Output | V _L | V _H |

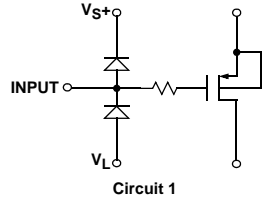
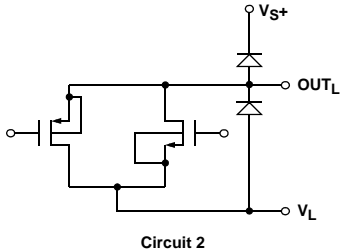
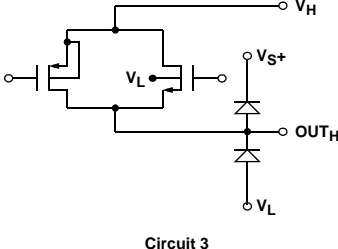
Timing Diagrams



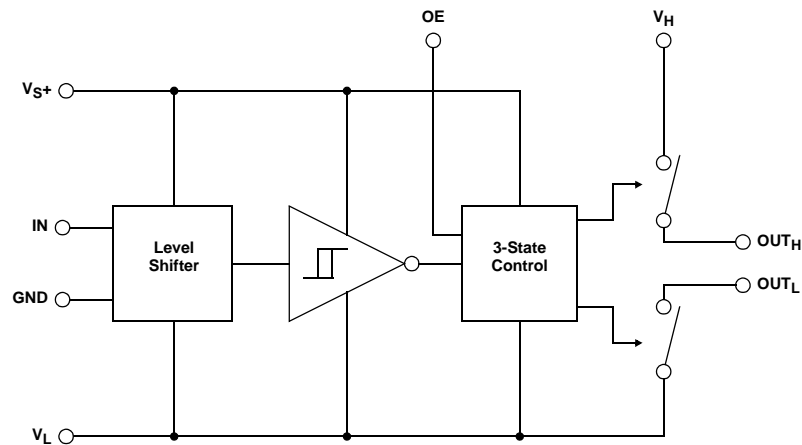
Standard Test Configuration



Pin Descriptions

| PIN | NAME | FUNCTION | EQUIVALENT CIRCUIT |
|-----|------|-------------------------|---|
| 1 | VS+ | Positive Supply Voltage | |
| 2 | OE | Output Enable |  <p>Circuit 1</p> |
| 3 | IN | Input | Reference Circuit 1 |
| 4 | GND | Ground | |
| 5 | VL | Negative Supply Voltage | |
| 6 | OUTL | Lower Switch Output |  <p>Circuit 2</p> |
| 7 | OUTH | Upper Switch Output |  <p>Circuit 3</p> |
| 8 | VH | Upper Output Voltage | |

Block Diagram



Applications Information

Product Description

The EL7155 is a high performance 40MHz pin driver. It contains two analog switches connecting V_H to OUT_H and V_L to OUT_L . Depending on the value of the IN pin, one of the two switches will be closed and the other switch open. An output enable (OE) is also supplied which opens both switches simultaneously.

Due to the topology of the EL7155, V_L should always be connected to a voltage equal to, or lower than GND. V_H can be connected to any voltage between V_L and the positive supply, V_{S+} .

The EL7155 is available in both the 8-pin SO and the 8-pin PDIP packages. The relevant package should be chosen depending on the calculated power dissipation.

3-state Operation

When the OE pin is low, the output is 3-state (floating.) The output voltage is the parasitic capacitance's voltage. It can be any voltage between V_H and V_L , depending on the previous state. At 3-state, the output voltage can be pushed to any voltage between V_H and V_L . The output voltage can't be pushed higher than V_H or lower than V_L since the body diode at the output stage will turn on.

Supply Voltage Range and Input Compatibility

The EL7155 is designed for operation on supplies from 5V to 15V (4.5V to 18V maximum). The table on page 6 shows the specifications for the relationship between the V_{S+} , V_H , V_L , and GND pins.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V_{S+}) of 5V, the EL7155 is also compatible with TTL inputs.

Power Supply Bypassing

When using the EL7155, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7155 necessitate the use of a bypass capacitor between the V_{S+} and GND pins. It is recommended that a 2.2 μ F tantalum capacitor be used in parallel with a 0.1 μ F low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the V_H and V_L pins have some level of bypassing, especially if the EL7155 is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7155 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

V_S is the total power supply to the EL7155 (from V_{S+} to GND)

V_{OUT} is the swing on the output ($V_H - V_L$)

C_L is the load capacitance

C_{INT} is the internal load capacitance (100pF max)

I_S is the quiescent supply current (3mA max)

f is frequency

Having obtained the application's power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T_{JMAX} :

$$\theta_{JA} = \frac{(T_{JMAX} - T_{MAX})}{PD}$$

where:

T_{JMAX} is the maximum junction temperature (125°C)

T_{MAX} is the maximum operating temperature

PD is the power dissipation calculated above

θ_{JA} thermal resistance on junction to ambient

θ_{JA} is 160°C/W for the SO8 package and 100°C/W for the PDIP8 package when using a standard JEDEC JESD51-3 single-layer test board. If T_{JMAX} is greater than 125°C when calculated using the equation above, then one of the following actions must be taken:

Reduce θ_{JA} the system by designing more heat-sinking into the PCB (as compared to the standard JEDEC JESD51-3)

Use the PDIP8 instead of the SO8 package

De-rate the application either by reducing the switching frequency, the capacitive load, or the maximum operating (ambient) temperature (T_{MAX})

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com