

TC74HC165AP, TC74HC165AF, TC74HC165AFN**8 – BIT SHIFT REGISTER (P – IN, S – OUT)**

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74HC165A is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

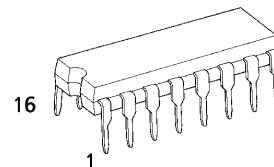
It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock inputs. When the $\overline{\text{SHIFT/LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When the $\overline{\text{SHIFT/LOAD}}$ input is held low, the parallel data is loaded asynchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

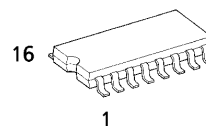
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

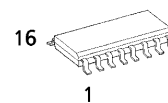
- High Speed..... $f_{\text{MAX}} = 56\text{MHz}(\text{typ.})$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}(\text{Min.})$
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..... $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide Operating Voltage Range..... $V_{\text{CC}}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS165



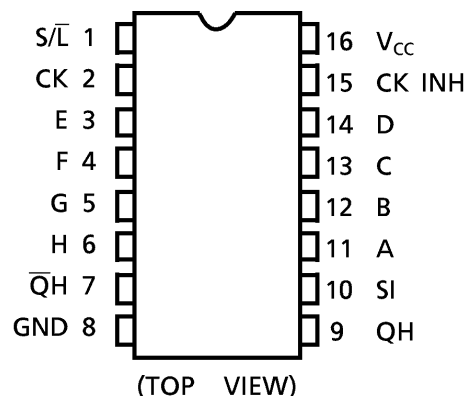
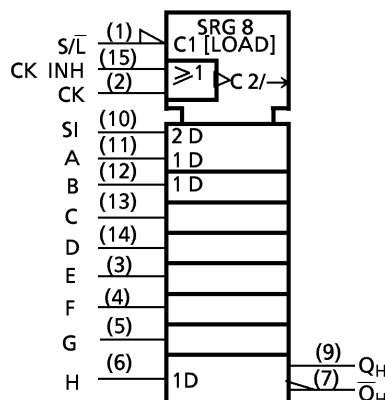
P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

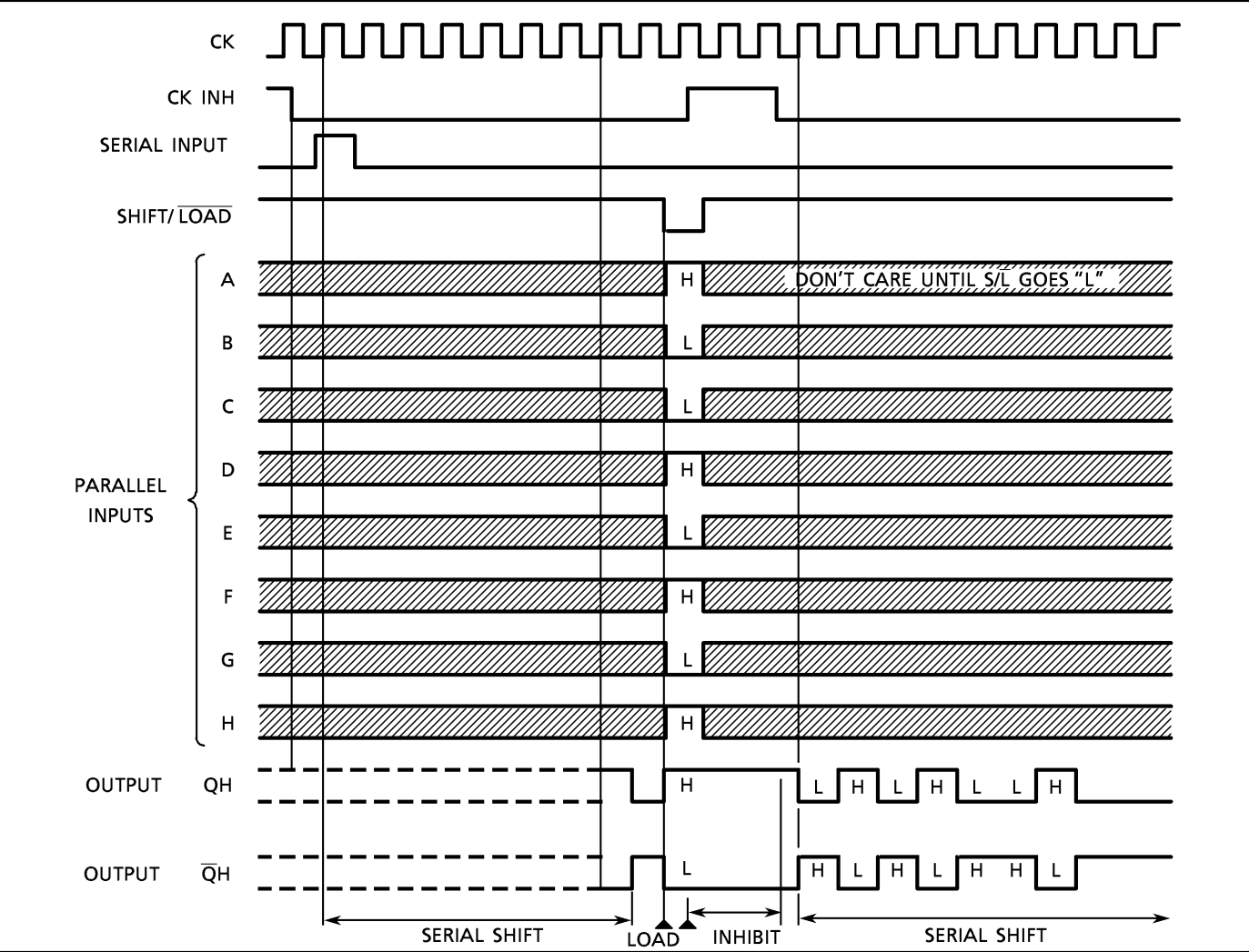
PIN ASSIGNMENT**IEC LOGIC SYMBOL**

TRUTH TABLE

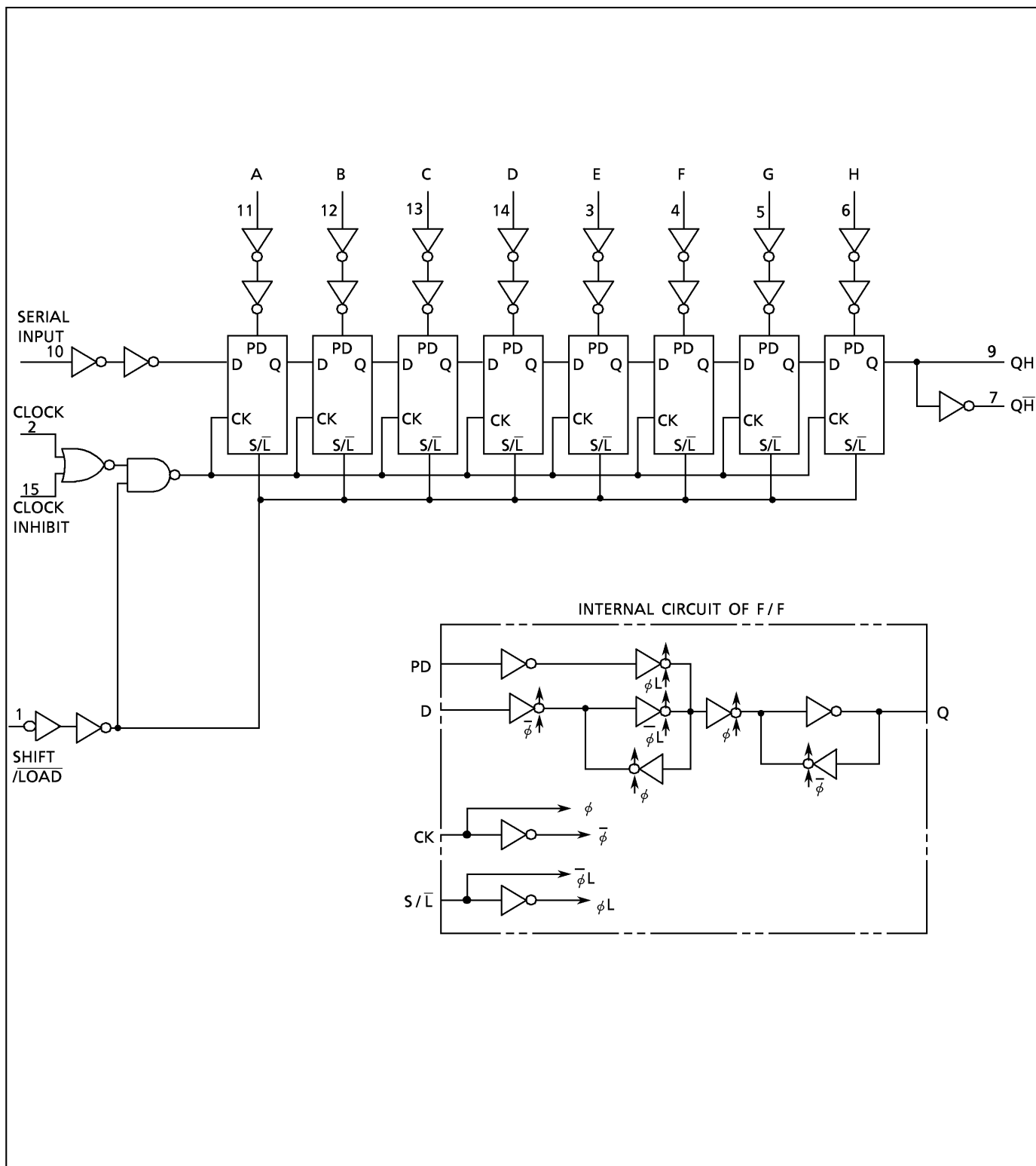
INPUTS					INTERNAL OUTPUTS		OUTPUT	
SHIFT/LOAD	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a h	a	b	h	$\overline{h}$
H	L		H	X	H	QAn	QGn	$\overline{QGn}$
H	L		L	X	L	QAn	QGn	$\overline{QGn}$
H		L	H	X	H	QAn	QGn	$\overline{QGn}$
H		L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	NO CHANGE			
H	H	X	X	X	NO CHANGE			

X : Don't Care
a h : The level of steady state input voltage at inputs A through H respectively
QAn~QGn : The level of QA~QG, respectively, before the most recent positive transition of the CK.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ ($V_{CC} = 2.0\text{V}$) $0 \sim 500$ ($V_{CC} = 4.5\text{V}$) $0 \sim 400$ ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$							V
		$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	V
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$							V
		$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	
		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS OPERATING CONDITIONS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK, CK INH)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (S/ $\bar{L}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (PI—S/ $\bar{L}$)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (SI—CK, CK INH)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (S/ $\bar{L}$ —CK, CK INH)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (PI—S/ $\bar{L}$)	t_h		2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (SI—CK, CK INH)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (S/ $\bar{L}$ —CK, CK INH)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (CK INH—CK) (CK—CK INH)	t_{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Clock Frequency	f		2.0	—	7	6	MHz
			4.5	—	30	24	
			6.0	—	41	28	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK, CK INH—QH, $\overline{QH}$)	t_{pLH} t_{pHL}		—	15	25	
Propagation Delay Time (S/L—QH, $\overline{QH}$)	t_{pLH} t_{pHL}		—	15	25	
Propagation Delay Time (H—QH, $\overline{QH}$)	t_{pLH} t_{pHL}		—	14	26	
Maximum Clock Frequency	f_{MAX}		35	56	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	25	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (CK, CK INH—QH, $\overline{\text{QH}}$)	t_{pLH} t_{pHL}		2.0	—	55	150	—	190
			4.5	—	18	30	—	38
			6.0	—	15	26	—	33
Propagation Delay Time (S/ $\overline{\text{L}}$ —QH, $\overline{\text{QH}}$)	t_{pLH} t_{pHL}		2.0	—	60	165	—	205
			4.5	—	19	33	—	41
			6.0	—	16	28	—	35
Propagation Delay Time (H—QH, $\overline{\text{QH}}$)	t_{pHL}		2.0	—	52	135	—	170
			4.5	—	17	27	—	34
			6.0	—	14	23	—	29
Maximum Clock Frequency Frequency	f_{MAX}		2.0	7	14	—	6	—
			4.5	30	46	—	24	—
			6.0	41	65	—	28	—
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	$C_{\text{PD}} (1)$			—	55	—	—	—

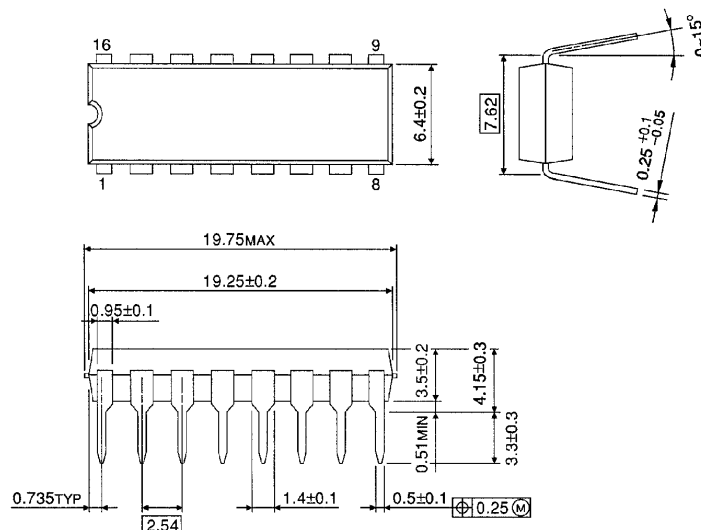
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

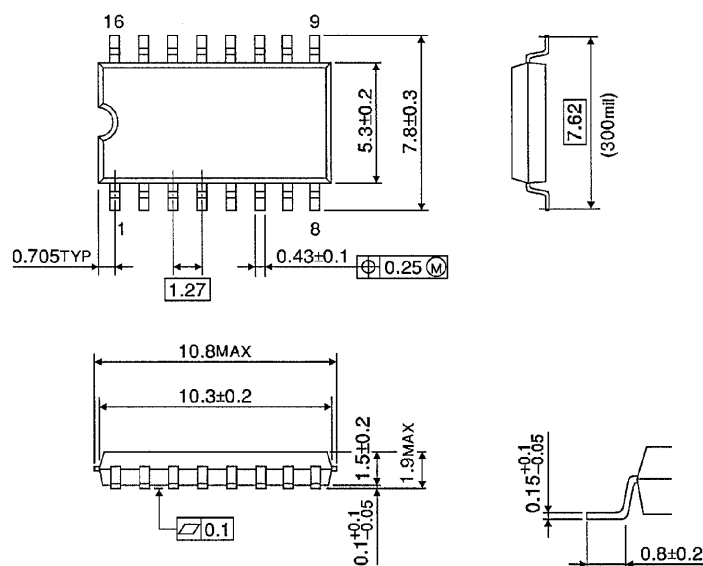
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

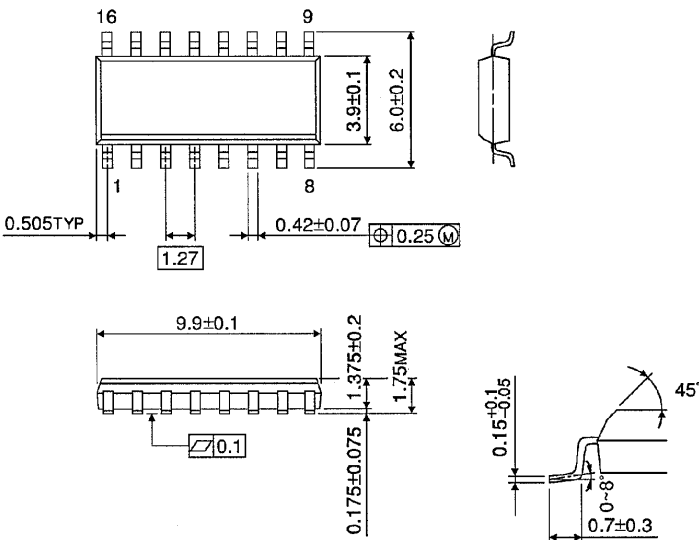


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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